Quad-SHARC®
DSP Multiprocessor Family

AD14060/AD14060L

PERFORMANCE FEATURES

ADSP-21060 core processor (× 4)
480 MFLOPS peak, 320 MFLOPS sustained
25 ns instruction rate, single-cycle instruction execution—each of four processors
16 Mbit shared SRAM (internal to SHARCs)
4 gigawords addressable off-module memory
Twelve 40 Mbyte/s link ports (3 per SHARC)
Four 40 Mbit/s independent serial ports (one from each SHARC)
One 40 Mbit/s common serial port
5 V and 3.3 V operation
32-bit single precision and 40-bit extended precision IEEE floating point data formats, or 32-bit fixed point data format
IEEE JTAG Standard 1149.1 test access port and on-chip emulation

PACKAGING FEATURES

308-lead ceramic quad flatpack (CQFP)
2.05" (52 mm) body size
Cavity up or down, configurable
Low profile, 0.160" height
Hermetic
25 Mil (0.65 mm) lead pitch
29 grams (typical)
θ_{JC} = 0.36°C/W

FUNCTIONAL BLOCK DIAGRAM

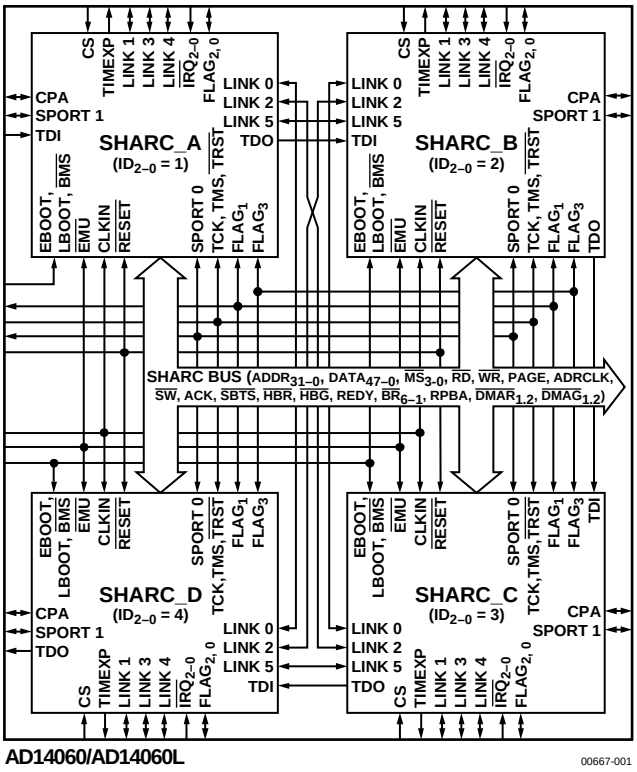

Figure 1.

GENERAL DESCRIPTION

The AD14060/AD14060L Quad-SHARC is the first in a family of high performance DSP multiprocessor modules. The core of the multiprocessor is the ADSP-21060 DSP microcomputer. The AD14060/AD14060L has the highest performance-to-density and lowest cost-to-performance ratios of any in its class. It is ideal for applications requiring higher levels of performance and/or functionality per unit area.

The AD14060/AD14060L takes advantage of the built-in multiprocessing features of the ADSP-21060 to achieve 480 peak MFLOPS with a single chip type in a single package. The on-chip SRAM of the DSPs provides 16 Mbits of on-module shared SRAM. The complete shared bus (48 data, 32 address) is also brought off-module for interfacing with expansion memory or other peripherals.

The ADSP-21060 link ports are interconnected to provide direct communication among the four SHARCs, as well as high speed off-module access. Internally, each SHARC has a direct link port connection. Externally, each SHARC has a total of 120 Mbytes/s link port bandwidth.

Multiprocessor performance is enhanced with embedded power and ground planes, matched impedance interconnect, and optimized signal routing lengths and separation. The fully tested and ready-to-insert multiprocessor also significantly reduces board space.

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

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REVISION HISTORY

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10/97—Rev. 0 to Rev. A

4/97—Revision 0: Initial Version

SPECIFICATIONS

Table 1. Recommended Operating Conditions

Parameter		B Grade Min	B Grade Max	K Grade Min	K Grade Max	Unit
V_{DD}	Supply Voltage (5 V)	4.75	5.25	4.75	5.25	V
	Supply Voltage (3.3 V)	3.15	3.6	3.15	3.6	V
T_{CASE}	Case Operating Temperature	−40	+100	0	+85	°C

ELECTRICAL CHARACTERISTICS (3.3 V, 5 V SUPPLY)

Table 2.

Parameter		Case Temp	Test Level	Test Condition	5 V Min	5 V Typ	5 V Max	3.3 V Min	3.3 V Typ	3.3 V Max	Unit
V_{IH1}	High Level Input Voltage[1]	Full	I	@ V_{DD} = max	2.0		V_{DD} + 0.5	2.0		V_{DD} + 0.5	V
V_{IH2}	High Level Input Voltage[2]	Full	I	@ V_{DD} = max	2.2		V_{DD} + 0.5	2.2		V_{DD} + 0.5	V
V_{IL}	Low Level Input Voltage[1, 2]	Full	I	@ V_{DD} = min			0.8			0.8	V
V_{OH}	High Level Output Voltage[3, 4]	Full	I	@ V_{DD} = min, I_{OH} = −2.0 mA	4.1			2.4			V
V_{OL}	Low Level Output Voltage[3, 4]	Full	I	@ V_{DD} = min, I_{OL} = 4.0 mA			0.4			0.4	V
I_{IH}	High Level Input Current[5, 6, 7]	Full	I	@ V_{DD} = max, V_{IN} = V_{DD} max			10			10	µA
I_{IL}	Low Level Input Current[5]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			10			10	µA
I_{ILP}	Low Level Input Current[6]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			150			150	µA
I_{ILPX4}	Low Level Input Current[7]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			600			600	µA
I_{OZH}	Three-State Leakage Current[8, 9, 10, 11]	Full	I	@ V_{DD} = max, V_{IN} = V_{DD} max			10			10	µA
I_{OZL}	Three-State Leakage Current[8, 12]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			10			10	µA
I_{OZHP}	Three-State Leakage Current[12]	Full	I	@ V_{DD} = max, V_{IN} = V_{DD} max			350			350	µA
I_{OZLC}	Three-State Leakage Current[13]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			1.5			1.5	mA
I_{OZLA}	Three-State Leakage Current[14]	Full	I	@ V_{DD} = max, V_{IN} = 1.5 V (5 V), 2 V (3.3 V)			350			350	µA
I_{OZLAR}	Three-State Leakage Current[10]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			4.2			4.2	mA
I_{OZLS}	Three-State Leakage Current[9]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			150			150	µA
I_{OZLSX4}	Three-State Leakage Current[11]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			600			600	µA
I_{DDIN}	Supply Current (Internal)[15]	Full	IV	t_{CK} = 25 ns, V_{DD} = max		1.4	2.92		1.0	2.2	A
I_{DDIDLE}	Supply Current (Idle)[16]	Full	I	V_{DD} = max			800			760	mA
C_{IN}	Input Capacitance[17, 18]	25°C	V			15			15		pF

[1] Applies to input and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{STBS}$, $\overline{IRQy_{2-0}}$, FLAGy0, FLAG1, FLAGy2, $\overline{HBG}$, CSy, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR_{6-1}}$, RPBA, $\overline{CPAy}$, TFS0, TFSy1, RFS0, RFSy1, $LyxDAT_{3-0}$, LyxCLK, LyxACK, EBOOTA, LBOOTA, EBOOTBCD, LBOOTBCD, $\overline{BMSA}$, $\overline{BMSBCD}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DRy1, TCLK0, TCLKy1, RCLK0, RCLKy1.

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

[3] Applies to output and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS_{3-0}}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAGy0, FLAG1, FLAGy2, TIMEXPy, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR_{6-1}}$, $\overline{CPAy}$, DTO, DTy1, TCLK0, TCLKy1, RCLK0, RCLKy1, TFS0, TFSy1, RFS0, RFSy1, $LyxDAT_{3-0}$, LyxCLK, LyxACK, $\overline{BMSA}$, $\overline{BMSBCD}$, TDO, $\overline{EMU}$.

[4] See the Output Drive Currents section for typical drive current capabilities.

[5] Applies to input pins: $\overline{STBS}$, $\overline{IRQy_{2-0}}$, $\overline{HBR}$, $\overline{CSy}$, $\overline{DMAR1}$, $\overline{DMAR2}$, RPBA, EBOOTA, LBOOTA, EBOOTBCD, LBOOTBCD, CLKIN, $\overline{RESET}$, TCK.

[6] Applies to input pins with internal pull-ups: DR0, $\overline{DRy1}$, TDI.

[7] Applies to bused input pins with internal pull-ups: $\overline{TRST}$, TMS.

[8] Applies to three-statable pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS_{3-0}}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAGy0, FLAG1, FLAGy2, REDY, $\overline{HBG}$, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMSA}$, $\overline{BMSBCD}$, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{2-0} = 001 and another ADSP-2106x is not requesting bus mastership. $\overline{HBG}$ and $\overline{EMU}$ are not tested for leakage current.)

[9] Applies to three-statable pins with internal pull-ups: DTy1, TCLKy1, RCLKy1.

[10] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{2-0} = 001 and another ADSP-2106x is not requesting bus mastership.)

[11] Applies to bused three-statable pins with internal pull-ups: DT0, TCLK0, RCLK0.

[12] Applies to three-statable pins with internal pull-downs: $LyxDAT_{3-0}$, LyxCLK, LyxACK.

[13] Applies to $\overline{CPAy}$ pin.

[14] Applies to ACK pin, when the keeper latch is enabled.

[15] Applies to V_{DD} pins. Conditions of operation: each processor is executing radix-2 FFT butterfly with instruction in cache, one data operand is fetched from each internal memory block, and one DMA transfer is occurring from/to internal memory at t_{CK} = 25 ns.

[16] Applies to V_{DD} pins. Idle denotes AD14060/AD14060L state during execution of IDLE instruction.

[17] Applies to all signal pins.

[18] Guaranteed, but not tested.

EXPLANATION OF TEST LEVELS

Test	Level
I	100% production tested.[1]
II	100% production tested at 25°C, and sample tested at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and analysis, and characterization testing on discrete SHARCs.
V	Parameter is typical value only.
VI	All devices are 100% production tested at 25°C, and sample tested at temperature extremes.

[1] Link and serial ports: All are 100% tested at die level prior to assembly. All are 100% ac tested at module level; Link 4 and Serial 0 are also dc tested at the module level. See the Timing Specifications section.

TIMING SPECIFICATIONS

This data sheet represents production-released specifications for the AD14060 (5 V), and for the AD14060L (3.3 V). The ADSP-21060 die components are 100% tested, and the assembled AD14060/AD14060L units are again extensively tested at speed and across temperature. Parametric limits were established from the ADSP-21060 characterization followed by further design and analysis of the AD14060/AD14060L package characteristics.

The specifications are based on a CLKIN frequency of 40 MHz (t_{CK} = 25 ns). The DT derating allows specifications at other CLKIN frequencies (within the minimum to maximum range of the t_{CK} specification; see Table 3). DT is the difference between the actual CLKIN period and a CLKIN period of 25 ns:

$$DT = t_{CK} - 25 \text{ ns}$$

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, one cannot meaningfully add parameters to derive longer times.

Switching Characteristics specify how the processor changes its signals. The user has no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics specify what the processor does in a given circumstance. The user can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

(O/D) = Open Drain

(A/D) = Active Drive

Table 3. Clock Input

Parameter		40 MHz (5 V) Min	40 MHz (5 V) Max	40 MHz (3.3 V) Min	40 MHz (3.3 V) Max	Unit
Clock Input						
Timing Requirements:						
t_{CK}	CLKIN Period	25	100	25	100	ns
t_{CKL}	CLKIN Width Low	7		9.5		ns
t_{CKH}	CLKIN Width High	5		5		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3	ns

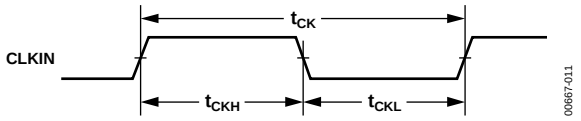


Figure 2. Clock Input

Table 4. Reset

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Reset						
Timing Requirements:						
t_{WRST}	$\overline{RESET}$ Pulse Width Low[1]	4 t_{CK}		4 t_{CK}		ns
t_{SRST}	$\overline{RESET}$ Setup before CLKIN High[2]	14 + DT/2	t_{CK}	14 + DT/2	t_{CK}	ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 2000 CLKIN cycles while $\overline{RESET}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of the external clock oscillator).
[2] Only required if multiple ADSP-2106xs must come out of reset synchronous to CLKIN with program counters (PC) equal (that is, for a SIMD system). Not required for multiple ADSP-2106xs communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

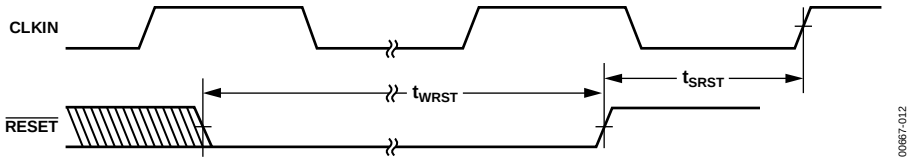


Figure 3. Reset

Table 5. Interrupts

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Interrupts						
Timing Requirements:						
t_{SIR}	$\overline{IRQ}$2-0 Setup before CLKIN High[1]	18 + 3 DT/4		18 + 3 DT/4		ns
t_{HIR}	$\overline{IRQ}$2-0 Hold before CLKIN High[1]		11.5 + 3 DT/4		11.5 + 3 DT/4	ns
t_{IPW}	$\overline{IRQ}$2-0 Pulse Width[2]	2 + t_{CK}		2 + t_{CK}		ns

[1] Only required for $\overline{IRQ}$x recognition in the following cycle.
[2] Applies only if t_{SIR} and t_{HIR} requirements are not met.

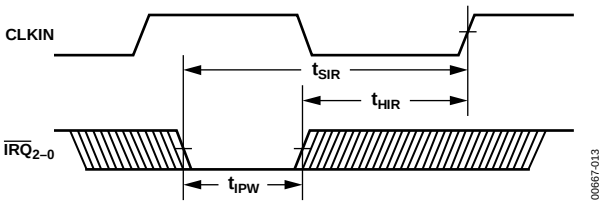


Figure 4. Interrupts

Table 6. Timer

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timer						
Switching Characteristic:						
t_{DTEX}	CLKIN High to TIMEXP		16		16	ns

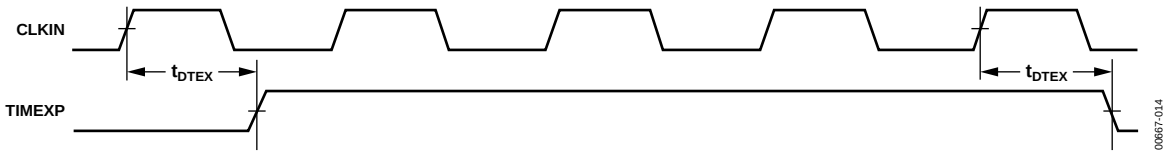


Figure 5. Timer

Table 7. Flags

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Flags						
Timing Requirements:						
t_{SFI}	FLAG2-0$_{IN}$ Setup before CLKIN High[1]	8 + 5 DT/16		8 + 5 DT/16		ns
t_{HFI}	FLAG2-0$_{IN}$ Hold after CLKIN High[1]	0.5 − 5 DT/16		0.5 − 5 DT/16		ns
t_{DWRFI}	FLAG2-0$_{IN}$ Delay after $\overline{RD}$/$\overline{WR}$ Low[1]		4.5 + 7 DT/16		4.5 + 7 DT/16	ns
t_{HFIWR}	FLAG2-0$_{IN}$ Hold after $\overline{RD}$/$\overline{WR}$ De-asserted[1]	0.5		0.5		ns
Switching Characteristics:						
t_{DFO}	FLAG2-0$_{OUT}$ Delay after CLKIN High		17		17	ns
t_{HFO}	FLAG2-0$_{OUT}$ Hold after CLKIN High	4		4		ns
t_{DFOE}	CLKIN High to FLAG2-0$_{OUT}$ Enable	3		3		ns
t_{DFOD}	CLKIN High to FLAG2-0$_{OUT}$ Disable		15		15	ns

[1] Flag inputs that meet these setup and hold times affect conditional instructions in the following instruction cycle.

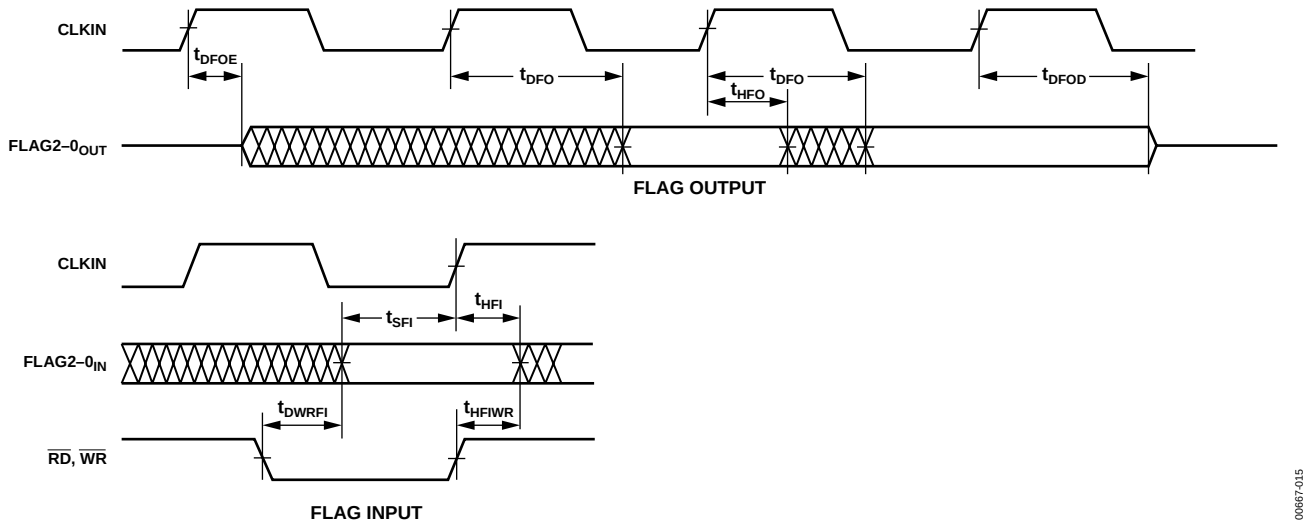


Figure 6. Flags

MEMORY READ—BUS MASTER

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the AD14060/AD14060L is the bus master accessing external memory space.

These switching characteristics also apply for bus master synchronous read/write timing (see the Synchronous Read/Write—Bus Master section). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa).

Table 8. Specifications

Parameter		5 V		3.3 V		Unit
		Min	Max	Min	Max	
Timing Requirements:						
t_{DAD}	Address, Delay to Data Valid[1, 2]		17.5 + DT + W		17.5 + DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		11.5 + 5 DT/8 + W		11.5 + 5 DT/8 + W	ns
t_{HDA}	Data Hold from Address[3]	1		1		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3]	2.5		2.5		ns
t_{DAAK}	ACK Delay from Address[2, 4]		13.5 + 7 DT/8 + W		13.5 + 7 DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[4]		7.5 + DT/2 + W		7.5 + DT/2 + W	ns
Switching Characteristics:						
t_{DRHA}	Address Hold after $\overline{RD}$ High	−0.5 + H		−0.5 + H		ns
t_{DARL}	Address to $\overline{RD}$ Low[2]	1.5 + 3 DT/8		1.5 + 3 DT/8		ns
t_{RW}	$\overline{RD}$ Pulse Width	12.5 + 5 DT/8 + W		12.5 + 5 DT/8 + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAG}$x Low	8 + 3 DT/8 + HI		8 + 3 DT/8 + HI		ns
t_{SADADC}	Address Setup before ADRCLK High[2]	−0.5 + DT/4		−0.5 + DT/4		ns

W = number of wait states specified in WAIT register × t_{CK}.
HI = t_{CK}, if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise, HI = 0.
H = t_{CK}, if an address hold cycle occurs as specified in WAIT register; otherwise, H = 0.

[1] Data delay/setup: User must meet t_{DAD}, t_{DRLD}, or synchronous specification, t_{SSDATI}.
[2] For $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$, the falling edge is referenced.
[3] Data hold: User must meet t_{HDA}, t_{HDRH}, or synchronous specification, t_{HDATI}. See the System Hold Time Calculation Example section for the calculation of hold times given capacitive and dc loads.
[4] ACK delay/setup: User must meet t_{DSAK}, t_{DAAK}, or synchronous specification, t_{SACKC}.

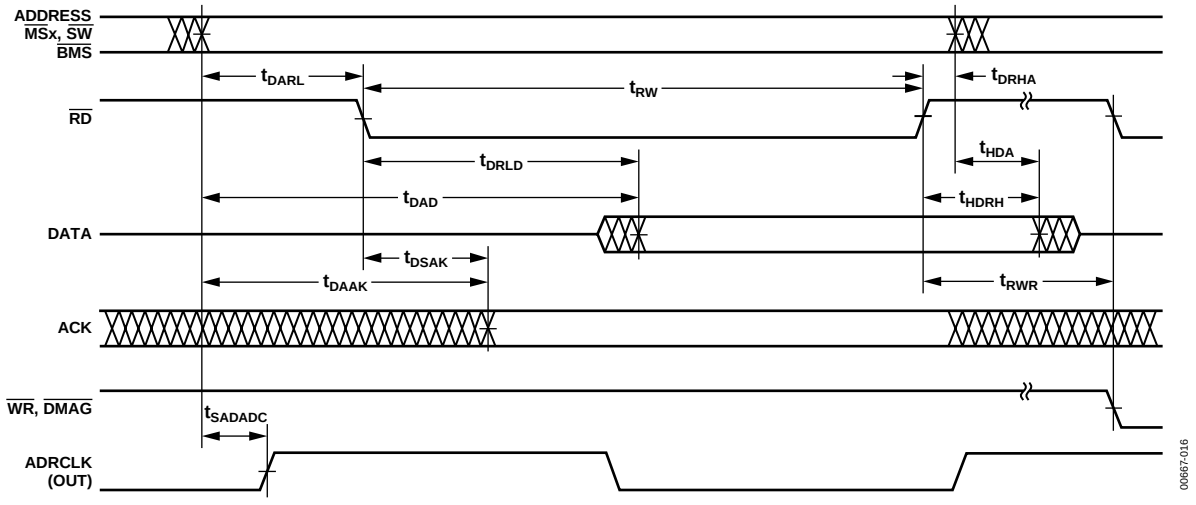


Figure 7. Memory Read—Bus Master

MEMORY WRITE—BUS MASTER

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the AD14060/AD14060L is the bus master accessing external memory space.

These switching characteristics also apply for bus master synchronous read/write timing (see the Synchronous Read/Write—Bus Master section). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa).

Table 9. Specifications

Parameter		5 V		3.3 V		Unit
		Min	Max	Min	Max	
Timing Requirements:						
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		13.5 + 7 DT/8 + W		13.5 + 7 DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		8 + DT/2 + W		8 + DT/2 + W	ns
Switching Characteristics:						
t_{DAWH}	Address, Selects to $\overline{WR}$ De-asserted[2]	16.5 + 15 DT/16 + W		16.5 + 15 DT/16 + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	2.5 + 3 DT/8		2.5 + 3 DT/8		ns
t_{WW}	$\overline{WR}$ Pulse Width	12 + 9 DT/16 + W		12 + 9 DT/16 + W		ns
t_{DDWH}	Data Setup before $\overline{WR}$ High	6.5 + DT/2 + W		6.5 + DT/2 + W		ns
t_{DWHA}	Address Hold after $\overline{WR}$ De-asserted	0 + DT/16 + H		0 + DT/16 + H		ns
t_{DATRWH}	Data Disable after $\overline{WR}$ De-asserted[3]	0.5 + DT/16 + H	6.5 + DT/16 + H	0.5 + DT/16 + H	6.5 + DT/16 + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAG}$x Low	8 + 7 DT/16 + H		8 + 7 DT/16 + H		ns
t_{DDWR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	4.5 + 3 DT/8 + 1		4.5 + 3 DT/8 + 1		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	−1.5 + DT/16		−1.5 + DT/16		ns
t_{SADADC}	Address, Selects to ADRCLK High[2]	−0.5 + DT/4		−0.5 + DT/4		ns

W = number of wait states specified in WAIT register × t_{CK}.
H = t_{CK}, if an address hold cycle occurs, as specified in WAIT register; otherwise, H = 0.
I = t_{CK}, if a bus idle cycle occurs, as specified in WAIT register; otherwise, I = 0.

[1] ACK delay/setup: User must meet t_{DAAK}, t_{DSAK}, or synchronous specification, t_{SACKC}.
[2] For $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$, the falling edge is referenced.
[3] See the System Hold Time Calculation Example section for the calculation of hold times given capacitive and dc loads.

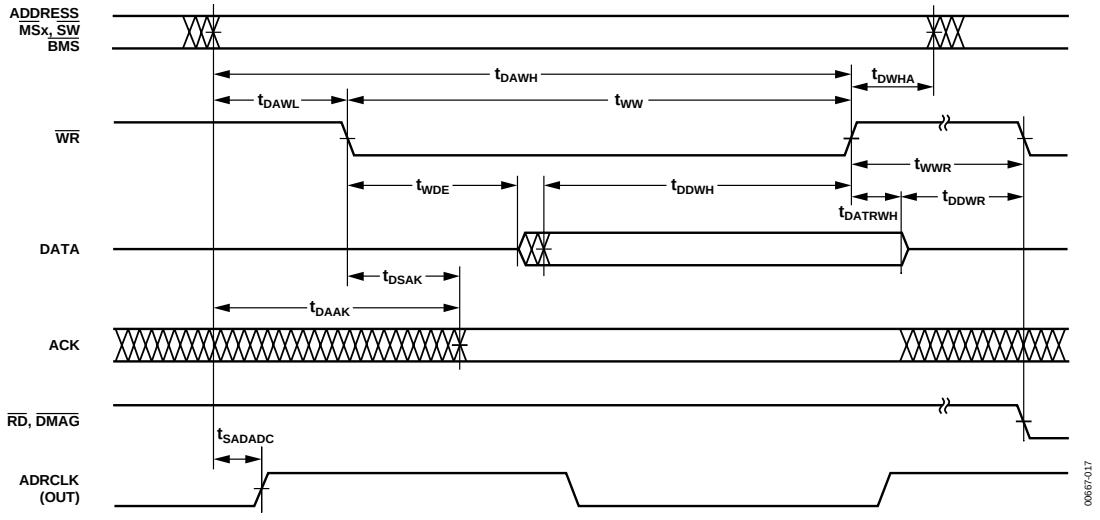


Figure 8. Memory Write—Bus Master

SYNCHRONOUS READ/WRITE—BUS MASTER

Use these specifications for interfacing to external memory systems that require CLKIN—relative timing or for accessing a slave ADSP 2106x in multiprocessor memory space. These synchronous switching characteristics are also valid during asynchronous memory reads and writes (see the Memory Read—Bus Master and Memory Write—Bus Master sections).

When accessing a slave ADSP-2106x, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see the Synchronous Read/Write—Bus Slave section). The slave ADSP-2106x must also meet these bus master timing requirements for data and acknowledge setup and hold times.

Table 10. Specifications

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements:						
t_{SSDATI}	Data Setup before CLKIN	3 + DT/8		3 + DT/8		ns
t_{HSDATI}	Data Hold after CLKIN	4 – DT/8		4 – DT/8		ns
t_{DAAK}	ACK Delay after Address, $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$[1, 2]		13.5 + 7 DT/8 + W		13.5 + 7 DT/8 + W	ns
t_{SACKC}	ACK Setup before CLKIN[2]	6.5 + DT/4		6.5 + DT/4		ns
t_{HACKC}	ACK Hold after CLKIN	–0.5 – DT/4		–0.5 – DT/4		ns
Switching Characteristics:						
t_{DADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$, Delay after CLKIN[1]		8 – DT/8		8 – DT/8	ns
t_{HADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$, Hold after CLKIN	–1 – DT/8		–1 – DT/8		ns
t_{DPGC}	PAGE Delay after CLKIN	9 + DT/8	17 + DT/8	9 + DT/8	17 + DT/8	ns
t_{DRDO}	$\overline{RD}$ High Delay after CLKIN	–2 – DT/8	+5 – DT/8	–2 – DT/8	+5 – DT/8	ns
t_{DWRO}	$\overline{WR}$ High Delay after CLKIN	–3 – 3 DT/16	+5 – 3 DT/16	–3 – 3 DT/16	+5 – 3 DT/16	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay after CLKIN	8 + DT/4	13.5 + DT/4	8 + DT/4	13.5 + DT/4	ns
t_{SDDATO}	Data Delay after CLKIN		20 + 5 DT/16		20.25 + 5 DT/16	ns
t_{DATTR}	Data Disable after CLKIN[3]	0 – DT/8	8 – DT/8	0 – DT/8	8 – DT/8	ns
t_{DADCCK}	ADRCLK Delay after CLKIN	4 + DT/8	11 + DT/8	4 + DT/8	11 + DT/8	ns
t_{ADRCK}	ADRCLK Period	t_{CK}		t_{CK}		ns
t_{ADRCKH}	ADRCLK Width High	(t_{CK}/2 – 2)		(t_{CK}/2 – 2)		ns
t_{ADRCKL}	ADRCLK Width Low	(t_{CK}/2 – 2)		(t_{CK}/2 – 2)		ns

W = number of wait states specified in WAIT register × t_{CK}.

[1] For $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$, the falling edge is referenced.
[2] ACK delay/setup: User must meet t_{DAAK}, t_{DSAK}, or synchronous specification, t_{SACKC}.
[3] See the System Hold Time Calculation Example section for the calculation of hold times given capacitive and dc loads.

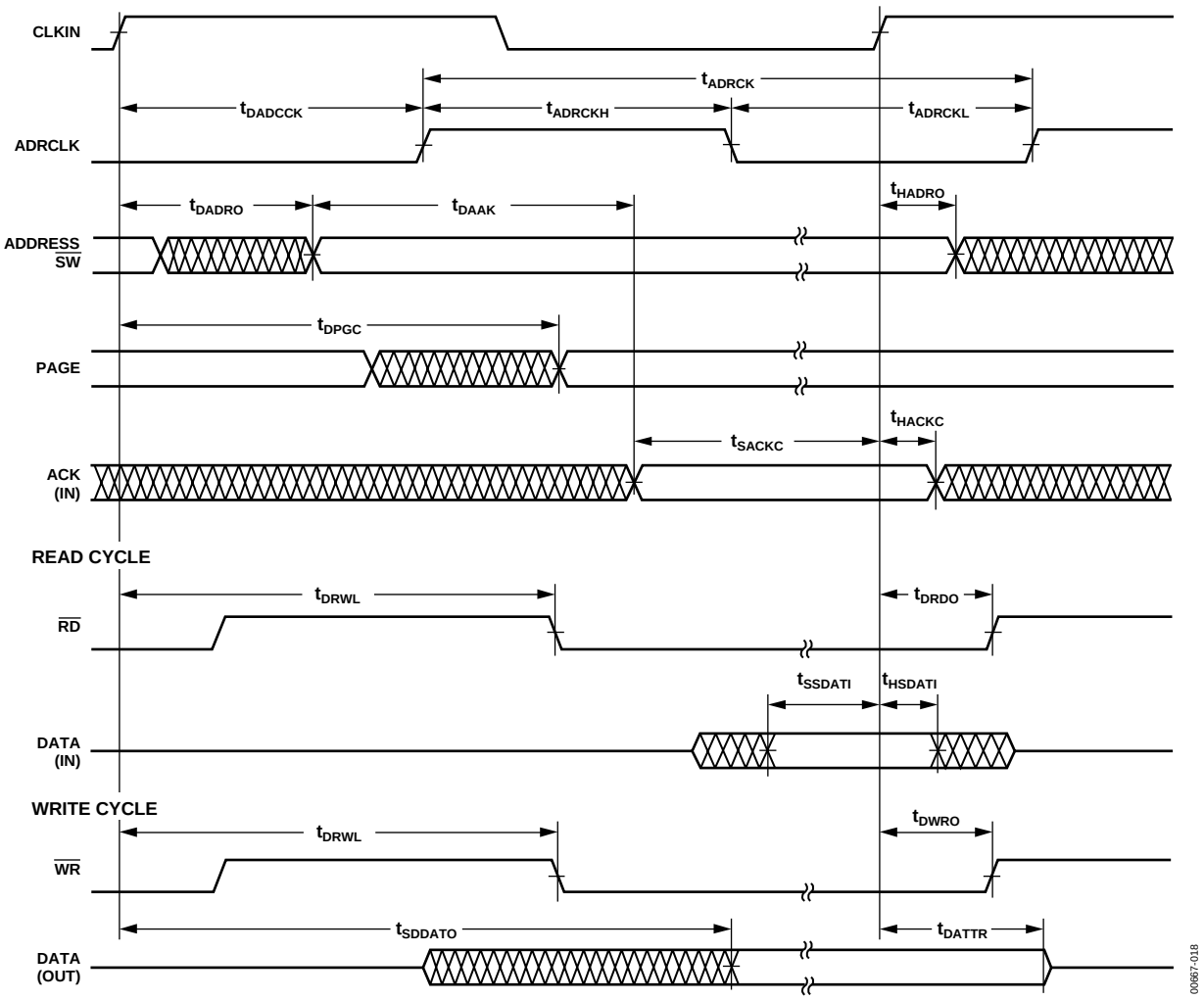


Figure 9. Synchronous Read/Write—Bus Master

SYNCHRONOUS READ/WRITE—BUS SLAVE

Use these specifications for bus master access to a slave's IOP registers or internal memory in multiprocessor memory space. The bus master must meet these bus slave timing requirements.

Table 11. Specifications

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements:						
t_{SADRI}	Address, $\overline{SW}$ Setup before CLKIN	15.5 + DT/2		15.5 + DT/2		ns
t_{HADRI}	Address, $\overline{SW}$ Hold before CLKIN		4.5 + DT/2		4.5 + DT/2	ns
t_{SRWLI}	$\overline{RD}/\overline{WR}$ Low Setup before CLKIN[1]	9.5 + 5 DT/16		9.5 + 5 DT/16		ns
t_{HRWLI}	$\overline{RD}/\overline{WR}$ Low Hold after CLKIN	−3.5 − 5 DT/16	+8 + 7 DT/16	−3.25 − 5 DT/16	+8 + 7 DT/16	ns
t_{RWHPI}	$\overline{RD}/\overline{WR}$ Pulse High	3		3		ns
t_{SDATWH}	Data Setup before $\overline{WR}$ High	5.5		5.5		ns
t_{HDATWH}	Data Hold after $\overline{WR}$ High	1.5		1.5		ns
Switching Characteristics:						
t_{SDDATO}	Data Delay after CLKIN		20 + 5 DT/16		20.25 + 5 DT/16	ns
t_{DATTR}	Data Disable after CLKIN[2]	0 − DT/8	8 − DT/8	0 − DT/8	8 − DT/8	ns
t_{DACKAD}	ACK Delay after Address, $\overline{SW}$[3]		10		10	ns
t_{ACKTR}	ACK Disable after CLKIN[3]	−1 − DT/8	+7 − DT/8	−1 − DT/8	+7 − DT/8	ns

[1] t_{SRWLI} (min) = 9.5 + 5 DT/16 when the multiprocessor memory space wait state (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min) = 4 + DT/8.

[2] See the System Hold Time Calculation Example section for the calculation of hold times given capacitive and dc loads.

[3] t_{DACKAD} is true only if the address and $\overline{SW}$ inputs have setup times (before CLKIN) greater than 10.5 + DT/8 and less than 18.5 + 3 DT/4. If the address and $\overline{SW}$ inputs have setup times greater than 19 + 3 DT/4, then ACK is valid 15 + DT/4 (max) after CLKIN. A slave that sees an address with an M field match responds with ACK regardless of the state of MMSWS or strobes. A slave three-states ACK every cycle with t_{ACKTR}.

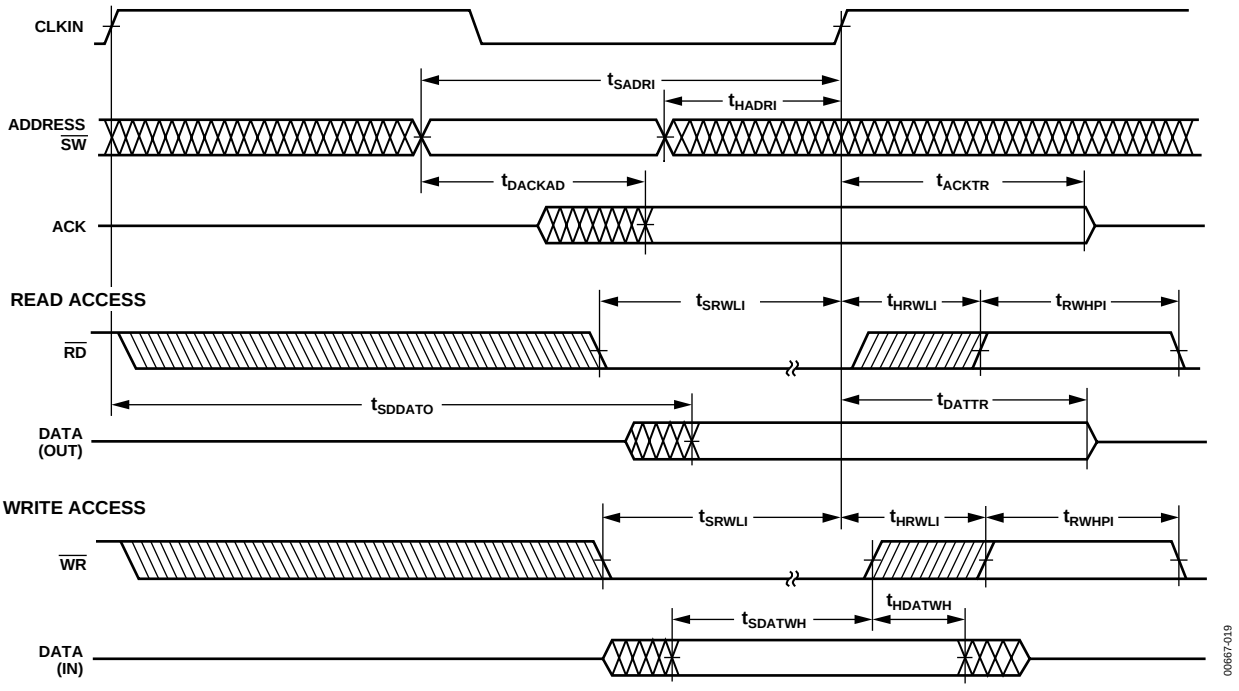


Figure 10. Synchronous Read/Write—Bus Slave

MULTIPROCESSOR BUS REQUEST AND HOST BUS REQUEST

Use these specifications for passing of the bus mastership among multiprocessing ADSP-2106xs ($\overline{BR}$x) or a host processor ($\overline{HBR}$, $\overline{HBG}$).

Table 12. Specifications

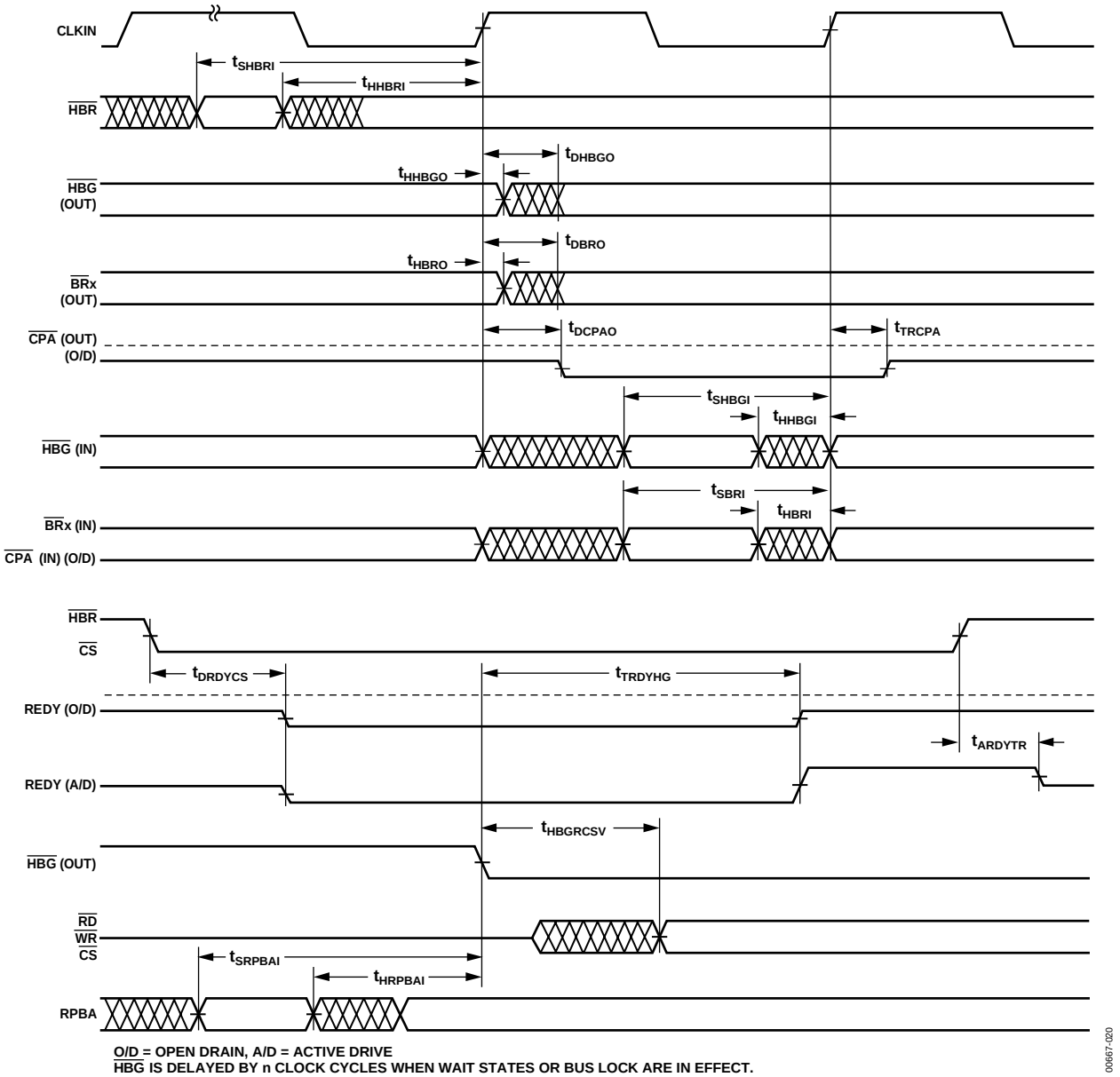
Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements:						
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$ Valid[1]		19.5 + 5 DT/4		19.5 + 5 DT/4	ns
t_{SHBRI}	$\overline{HBR}$ Setup before CLKIN[2]	20 + 3 DT/4		20 + 3 DT/4		ns
t_{HHBRI}	$\overline{HBR}$ Hold before CLKIN[2]		13.5 + 3 DT/4		13.5 + 3 DT/4	ns
t_{SHBGI}	$\overline{HBG}$ Setup before CLKIN	13 + DT/2		13 + DT/2		ns
t_{HHBGI}	$\overline{HBG}$ Hold before CLKIN High		5.5 + DT/2		5.5 + DT/2	ns
t_{SBRI}	$\overline{BR}$x, $\overline{CPA}$ Setup before CLKIN[3]	13 + DT/2		13 + DT/2		ns
t_{HBRI}	$\overline{BR}$x, $\overline{CPA}$ Hold before CLKIN High		5.5 + DT/2		5.5 + DT/2	ns
t_{SRPBAI}	RPBA Setup before CLKIN	21 + 3 DT/4		21 + 3 DT/4		ns
t_{HRPBAI}	RPBA Hold before CLKIN		11.5 + 3 DT/4		11.5 + 3 DT/4	ns
Switching Characteristics:						
t_{DHBGO}	$\overline{HBG}$ Delay after CLKIN		8 – DT/8		8 – DT/8	ns
t_{HHBGO}	$\overline{HBG}$ Hold after CLKIN	–2 – DT/8		–2 – DT/8		ns
t_{DBRO}	$\overline{BR}$x Delay after CLKIN		8 – DT/8		8 – DT/8	ns
t_{HBRO}	$\overline{BR}$x Hold after CLKIN	–2 – DT/8		–2 – DT/8		ns
t_{DCPAO}	$\overline{CPA}$ Low Delay after CLKIN		9 – DT/8		9.5 – DT/8	ns
t_{TRCPA}	$\overline{CPA}$ Disable after CLKIN	–2 – DT/8	+5.5 – DT/8	–2 – DT/8	+5.5 – DT/8	ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{CS}$ and $\overline{HBR}$ Low[4]		9.5		12	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{HBG}$[4]	40 + 27 DT/16		40 + 27 DT/16		ns
t_{ARDYTR}	REDY (A/D) Disable from $\overline{CS}$ or $\overline{HBR}$ High[4]		11		11	ns

[1] For first asynchronous access after $\overline{HBR}$ and $\overline{CS}$ asserted, $ADDR_{31-0}$ must be a non-MMS value 1/2 t_{CK} before $\overline{RD}$ or $\overline{WR}$ goes low, or by $t_{HBGRCSV}$ after HBG goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted.

[2] Required only for recognition in the current cycle.

[3] $\overline{CPA}$ assertion must meet the setup to CLKIN; de-assertion does not need to meet the setup to CLKIN.

[4] (O/D) = open drain; (A/D) = active drive.



O/D = OPEN DRAIN, A/D = ACTIVE DRIVE
HBG IS DELAYED BY n CLOCK CYCLES WHEN WAIT STATES OR BUS LOCK ARE IN EFFECT.

Figure 11. Multiprocessor Bus Request and Host Bus Request

ASYNCHRONOUS READ/WRITE—HOST TO AD14060/AD14060L

Use these specifications for asynchronous host processor access to an AD14060/AD14060L, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the AD14060/AD14060L, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the AD14060/AD14060L's internal memory or IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing.

Table 13. Specifications

		5 V		3.3 V		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Read Cycle						
Timing Requirements:						
t_{SADRDL}	Address Setup/$\overline{CS}$ Low before $\overline{RD}$ Low[1]	0.5		0.5		ns
t_{HADRDH}	Address Hold/$\overline{CS}$ Hold Low after $\overline{RD}$	0.5		0.5		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6		6		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay after REDY (O/D) Disable	0		0		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay after REDY (A/D) Disable	0		0		ns
Switching Characteristics:						
$t_{SDATRDY}$	Data Valid before REDY Disable from Low	1.5		1.5		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay after $\overline{RD}$ Low		11		13.5	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulse Width for Read	45 + DT		45 + DT		ns
t_{HDARWH}	Data Disable after $\overline{RD}$ High	1.5	9	1.5	9.5	ns
Write Cycle						
Timing Requirements:						
t_{SCSWRL}	$\overline{CS}$ Low Setup before $\overline{WR}$ Low	0.5		0.5		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold after $\overline{WR}$ High	0.5		0.5		ns
t_{SADWRH}	Address Setup before $\overline{WR}$ High	5.5		5.5		ns
t_{HADWRH}	Address Hold after $\overline{WR}$ High	2.5		2.5		ns
t_{WWRL}	$\overline{WR}$ Low Width	7		7		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6		6		ns
$t_{DWRHRDY}$	$\overline{WR}$ High Delay after REDY (O/D) or (A/D) Disable	0.5		0.5		ns
t_{SDATWH}	Data Setup before $\overline{WR}$ High	5.5		5.5		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1.5		1.5		ns
Switching Characteristics:						
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay after $\overline{WR}$/$\overline{CS}$ Low		11		13.5	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulse Width for Write	15		15		ns
t_{SRDYCK}	REDY (O/D) or (A/D) Disable to CLKIN	0 + 7 DT/16	8 + 7 DT/16	0 + 7 DT/16	8 + 7 DT/16	ns

[1] Not required, if $\overline{RD}$ and address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. For first access after $\overline{HBR}$ is asserted, $ADDR_{31-0}$ must be a non-MMS value 1/2 t_{CLK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. For address bits to be driven during asynchronous host accesses, see the *ADSP-2106x SHARC User's Manual.*

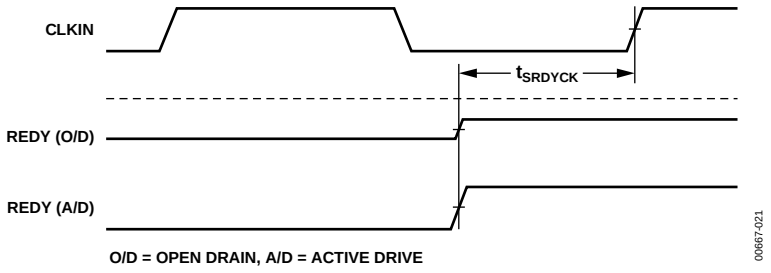


Figure 12. Synchronous REDY Timing

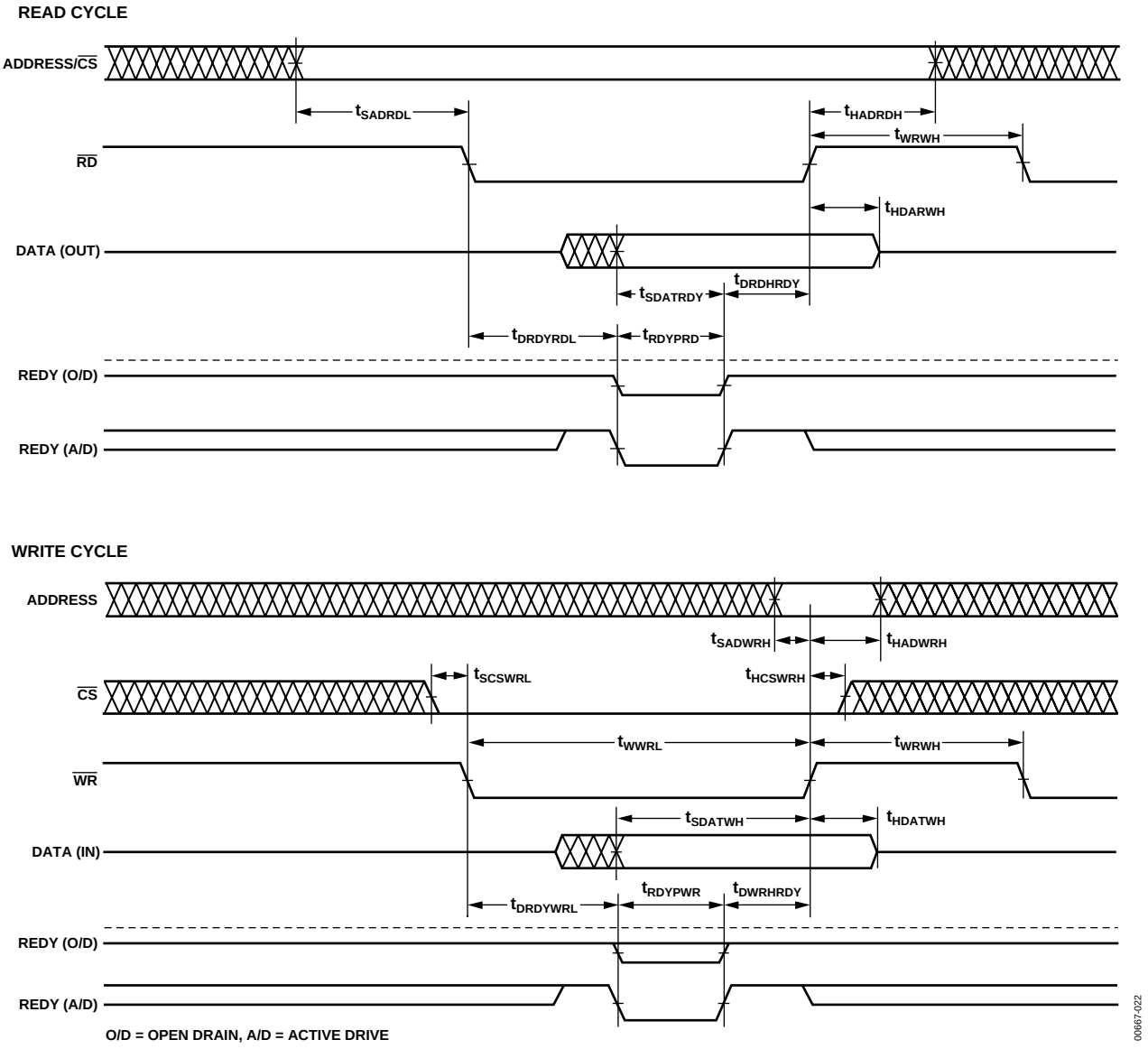


Figure 13. Asynchronous Read/Write—Host to ADSP-2106x

THREE-STATE TIMING—BUS MASTER, BUS SLAVE, $\overline{\text{HBR}}$, $\overline{\text{SBTS}}$

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{\text{SBTS}}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{\text{SBTS}}$ pin.

Table 14. Specifications

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements:						
t_{STSCK}	$\overline{\text{SBTS}}$ Setup before CLKIN	12.5 + DT/2		12.5 + DT/2		ns
t_{HTSCK}	$\overline{\text{SBTS}}$ Hold before CLKIN		5.5 + DT/2		5.5 + DT/2	ns
Switching Characteristics:						
t_{MIENA}	Address/Select Enable after CLKIN	−1.5 − DT/8		−1.25 − DT/8		ns
t_{MIENS}	Strobes Enable after CLKIN[1]	−1.5 − DT/8		−1.5 − DT/8		ns
t_{MIENHG}	$\overline{\text{HBG}}$ Enable after CLKIN	−1.5 − DT/8		−1.5 − DT/8		ns
t_{MITRA}	Address/Select Disable after CLKIN		1 − DT/4		1.25 − DT/4	ns
t_{MITRS}	Strobes Disable after CLKIN[1]		2.5 − DT/4		2.5 − DT/4	ns
t_{MITRHG}	$\overline{\text{HBG}}$ Disable after CLKIN		3 − DT/4		3 − DT/4	ns
t_{DATEN}	Data Enable after CLKIN[2]	9 + 5 DT/16		9 + 5 DT/16		ns
t_{DATTR}	Data Disable after CLKIN[2]	0 − DT/8	8 − DT/8	0 − DT/8	8 − DT/8	ns
t_{ACKEN}	ACK Enable after CLKIN[2]	7.5 + DT/4		7.5 + DT/4		ns
t_{ACKTR}	ACK Disable after CLKIN[2]	−1 − DT/8	+7 − DT/8	−1 − DT/8	+7 − DT/8	ns
t_{ADCEN}	ADRCLK Enable after CLKIN	−2 − DT/8		−2 − DT/8		ns
t_{ADCTR}	ADRCLK Disable after CLKIN		9 − DT/4		9 − DT/4	ns
t_{MTRHBG}	Memory Interface Disable before $\overline{\text{HBG}}$ Low[3]	−1 + DT/8		−1 + DT/8		ns
t_{MENHBG}	Memory Interface Enable after $\overline{\text{HBG}}$ High[3]	18.5 + DT		18.5 + DT		ns

[1] Strobes = $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, PAGE, $\overline{\text{DMAG}}$.
[2] In addition to bus master transition cycles, these specifications also apply to bus master and bus slave synchronous read/write.
[3] Memory interface = address, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}$x, $\overline{\text{SW}}$, $\overline{\text{HBG}}$, PAGE,$\overline{\text{DMAG}}$x, $\overline{\text{BMS}}$ (in EPROM boot mode).

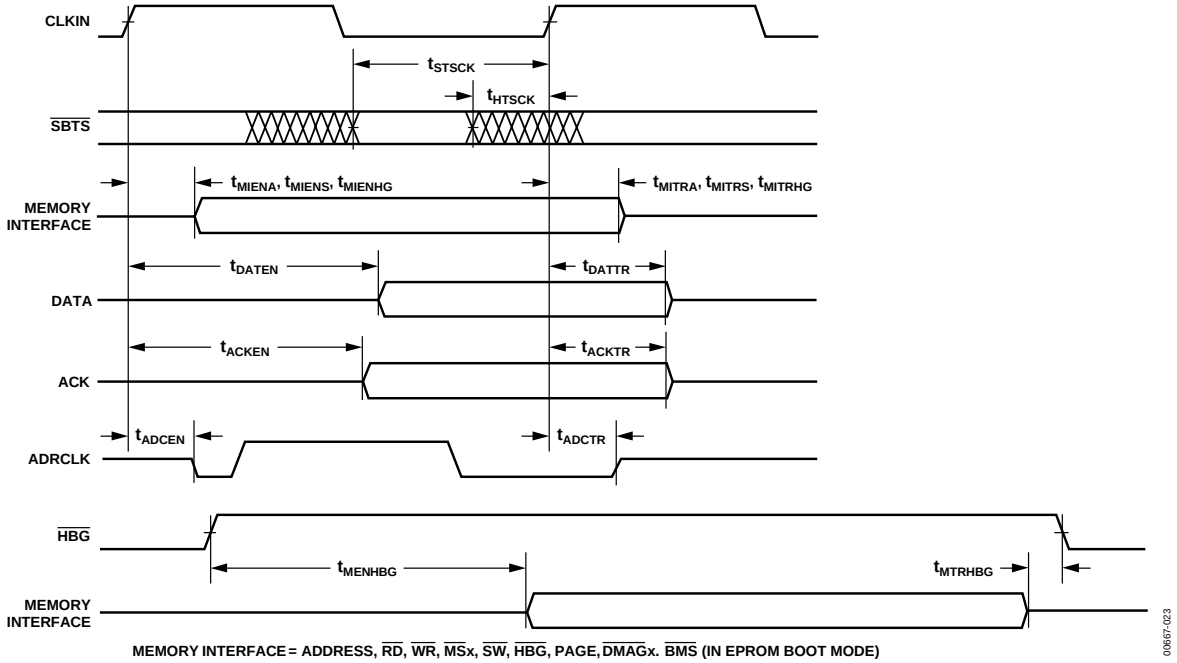


Figure 14. Three-State Timing

DMA HANDSHAKE

These specifications describe the three DMA handshake modes. In all three modes, $\overline{\text{DMAR}}$ is used to initiate transfers. For handshake mode, $\overline{\text{DMAG}}$ controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the $\text{ADDR}_{31\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, PAGE, $\overline{\text{MS}}_{3\text{-}0}$, ACK, and $\overline{\text{DMAG}}$ signals. For paced master mode, the data transfer is controlled by $\text{ADDR}_{31\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}_{3\text{-}0}$, and ACK (not $\overline{\text{DMAG}}$). For paced master mode, the memory read—bus master, memory write—bus master, and synchronous read/write—bus master timing specifications for $\text{ADDR}_{31\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}_{3\text{-}0}$, $\overline{\text{SW}}$, PAGE, $\text{DATA}_{47\text{-}0}$, and ACK also apply.

Table 15. Specifications

		5 V		3.3 V		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements:						
t_{SDRLC}	$\overline{\text{DMAR}}$x Low Setup before CLKIN[1]	5		5		ns
t_{SDRHC}	$\overline{\text{DMAR}}$x High Setup before CLKIN[1]	5		5		ns
t_{WDR}	$\overline{\text{DMAR}}$x Width Low (Nonsynchronous)	6		6		ns
$t_{SDATDGL}$	Data Setup after $\overline{\text{DMAG}}$x Low[2]		9 + 5 DT/8		9 + 5 DT/8	ns
$t_{HDATIDG}$	Data Hold after $\overline{\text{DMAG}}$x High	2		2		ns
t_{DATDRH}	Data Valid after $\overline{\text{DMAG}}$x High[2]		15.5 + 7 DT/8		15.5 + 7 DT/8	ns
t_{DMARLL}	$\overline{\text{DMAG}}$x Low Edge to Low Edge	23 + 7 DT/8		23 + 7 DT/8		ns
t_{DMARH}	$\overline{\text{DMAG}}$x Width High	6		6		ns
Switching Characteristics:						
t_{DDGL}	$\overline{\text{DMAG}}$x Low Delay after CLKIN	9 + DT/4	16 + DT/4	9 + DT/4	16 + DT/4	ns
t_{WDGH}	$\overline{\text{DMAG}}$x High Width	6 + 3 DT/8		6 + 3 DT/8		ns
t_{WDGL}	$\overline{\text{DMAG}}$x Low Width	12 + 5 DT/8		12 + 5 DT/8		ns
t_{HDGC}	$\overline{\text{DMAG}}$x High Delay after CLKIN	−2 − DT/8	+7 − DT/8	−2 − DT/8	+7 − DT/8	ns
$t_{VDATDGH}$	Data Valid before $\overline{\text{DMAG}}$x High[3]	7.5 + 9 DT/16		7.5 + 9 DT/16		ns
$t_{DATRDGH}$	Data Disable after $\overline{\text{DMAG}}$x High[4]	−1	+7.5	−1	+7.5	ns
t_{DGWRL}	$\overline{\text{WR}}$ Low before $\overline{\text{DMAG}}$x Low	−0.5	+2.5	−0.75	+2.5	ns
t_{DGWRH}	$\overline{\text{DMAG}}$x Low before $\overline{\text{WR}}$ High	9.5 + 5 DT/8 + W		9.5 + 5 DT/8 + W		ns
t_{DGWRR}	$\overline{\text{WR}}$ High before $\overline{\text{DMAG}}$x High	0.5 + DT/16	3.5 + DT/16	0.5 + DT/16	3.5 + DT/16	ns
t_{DGRDL}	$\overline{\text{RD}}$ Low before $\overline{\text{DMAG}}$x Low	−0.25	+2.5	0	2.5	ns
t_{DRDGH}	$\overline{\text{RD}}$ Low before $\overline{\text{DMAG}}$x High	11 + 9 DT/16 + W		11 + 9 DT/16 + W		ns
t_{DGRDR}	$\overline{\text{RD}}$ High before $\overline{\text{DMAG}}$x High	0	3.5	0	3.5	ns
t_{DGWR}	$\overline{\text{DMAG}}$x High to $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{DMAG}}$x Low	4.5 + 3 DT/8 + HI		4.5 + 3 DT/8 + HI		ns
t_{DADGH}	Address/Select Valid to $\overline{\text{DMAG}}$x High	16 + DT		16 + DT		ns
t_{DDGHA}	Address/Select Hold after $\overline{\text{DMAG}}$x High	−1.5		−1.5		ns

W = number of wait states specified in WAIT register × t_{CK}.
HI = t_{CK}, if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise, HI = 0.

[1] Required only for recognition in the current cycle.
[2] $t_{SDATDGL}$ is the data setup requirement, if $\overline{\text{DMAR}}$x is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMAR}}$x low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMAR}}$x is brought high.
[3] $t_{VDATDGH}$ is valid, if $\overline{\text{DMAR}}$x is not being used to hold off completion of a read. If $\overline{\text{DMAR}}$x is used to prolong the read, then $t_{VDATDGH}$ = 7.5 + 9 DT/16 + ($n \times t_{CK}$), where n equals the number of extra cycles that the access is prolonged.
[4] See the System Hold Time Calculation Example section for the calculation of hold times given capacitive and dc loads.

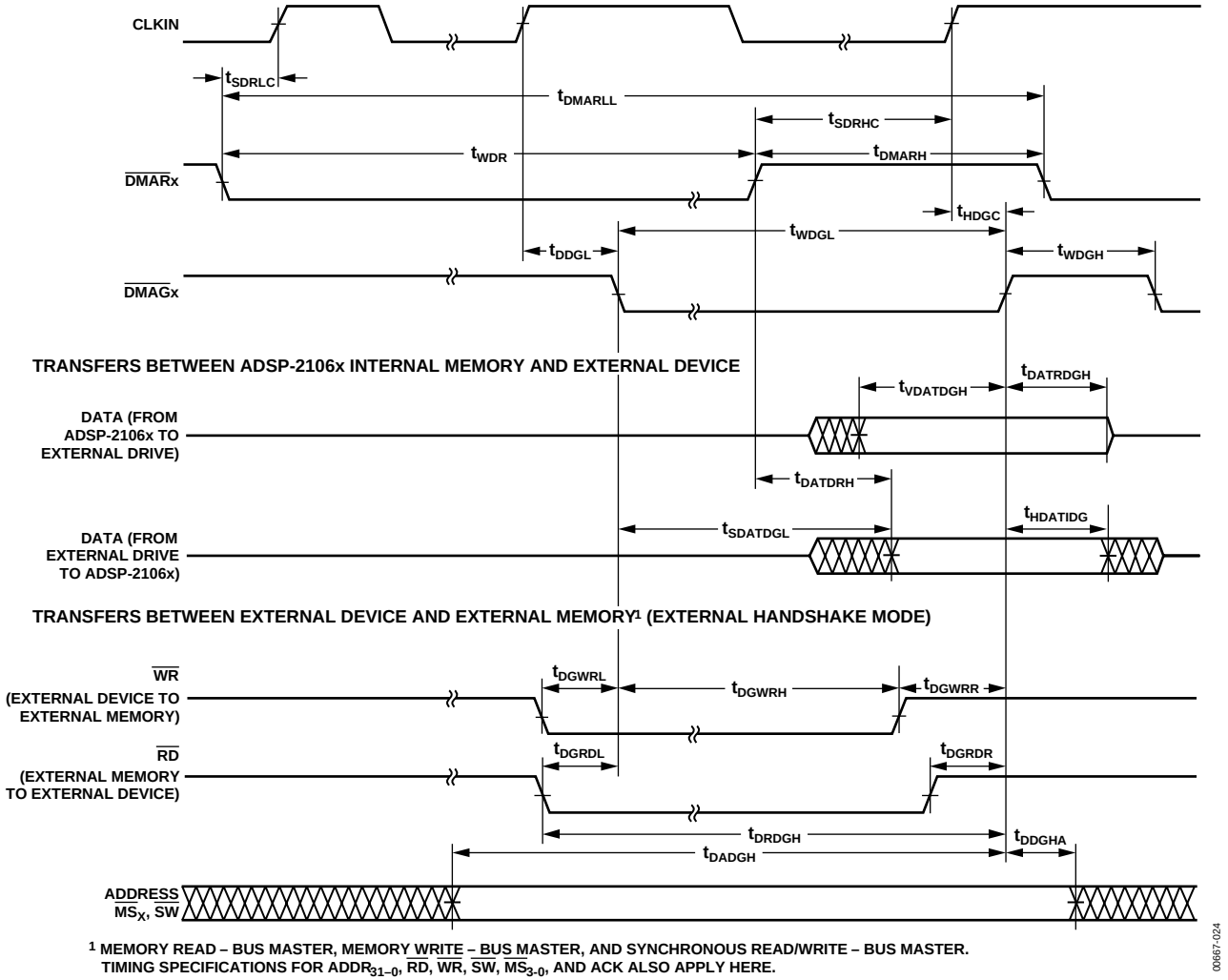


Figure 15. DMA Handshake Timing

Table 16. 1× CLK Speed Operation

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Receive						
Timing Requirements:						
t_{SLDCL}	Data Setup before LCLK Low	3.5		3		ns
t_{HLDCL}	Data Hold after LCLK Low	3		3		ns
t_{LCLKIW}	LCLK Period (1× Operation)	t_{CK}		t_{CK}		ns
$t_{LCLKRWL}$	LCLK Width Low	6		6		ns
$t_{LCLKRWH}$	LCLK Width High	5		5		ns
Switching Characteristics:						
t_{DLAHC}	LACK High Delay after CLKIN High	18 + DT/2	29.5 + DT/2	18 + DT/2	30 + DT/2	ns
t_{DLALC}	LACK Low Delay after LCLK High[1]	−3	+13.5	−3	+13.5	ns
t_{ENDLK}	LACK Enable from CLKIN	5 + DT/2		5 + DT/2		ns
t_{TDLK}	LACK Disable from CLKIN		21 + DT/2		21 + DT/2	ns
Transmit						
Timing Requirements:						
t_{SLACH}	LACK Setup before LCLK High	18		20		ns
t_{HLACH}	LACK Hold after LCLK High	−7		−7		ns
Switching Characteristics:						
t_{DLCLK}	LCLK Delay after CLKIN (1× Operation)		16.5		17.5	ns
t_{DLDCH}	Data Delay after LCLK High		3.5		3	ns
t_{HLDCH}	Data Hold after LCLK High	−3		−3		ns
$t_{LCLKTWL}$	LCLK Width Low	$(t_{CK}/2) - 2$	$(t_{CK}/2) + 2$	$(t_{CK}/2) - 1$	$(t_{CK}/2) + 2.25$	ns
$t_{LCLKTWH}$	LCLK Width High	$(t_{CK}/2) - 2$	$(t_{CK}/2) + 2$	$(t_{CK}/2) - 2.25$	$(t_{CK}/2) + 1$	ns
t_{DLACLK}	LCLK Low Delay after LACK High	$(t_{CK}/2) + 8.5$	$(3 \times t_{CK}/2) + 17.5$	$(t_{CK}/2) + 8$	$(3 \times t_{CK}/2) + 18.25$	ns
t_{ENDLK}	LDAT, LCLK Enable after CLKIN	5 + DT/2		5 + DT/2		ns
t_{TDLK}	LDAT, LCLK Disable after CLKIN		21 + DT/2		21 + DT/2	ns
Link Port Service Request Interrupts: 1× and 2× Speed Operations						
Timing Requirements:						
t_{SLCK}	LACK/LCLK Setup before CLKIN Low[2]	10		10		ns
t_{HLCK}	LACK/LCLK Hold after CLKIN Low[2]	2.5		2.5		ns

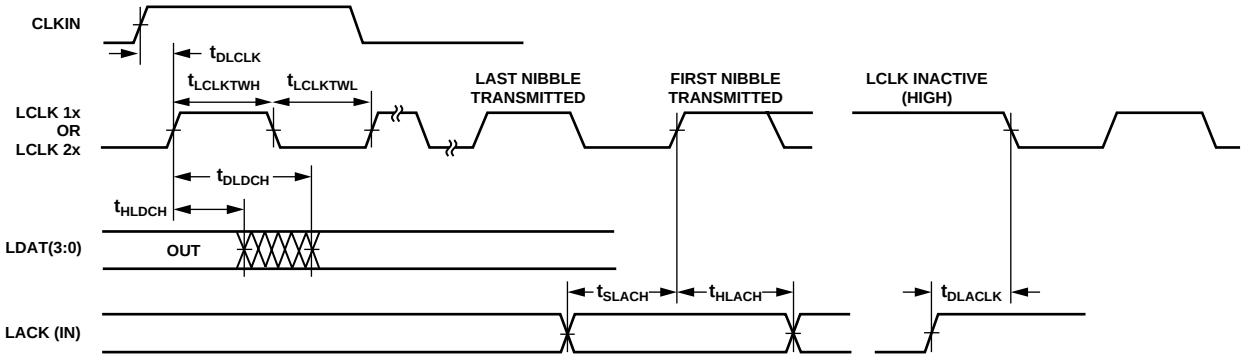
[1] LACK goes low with t_{DLALC} relative to the rising edge of LCLK after the first nibble is received. LACK does not go low, if the receiver's link buffer is not about to fill.
[2] Required only for interrupt recognition in the current cycle.

Table 17. 2× CLK Speed Operation

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Receive						
Timing Requirements:						
t_{SLDCL}	Data Setup before LCLK Low	2.75		2.25		ns
t_{HLDCL}	Data Hold after LCLK Low	2.25		2.25		ns
t_{LCLKIW}	LCLK Period (2× Operation)	$t_{CK}/2$		$t_{CK}/2$		ns
$t_{LCLKRWL}$	LCLK Width Low	4.6		5.25		ns
$t_{LCLKRWH}$	LCLK Width High	4.25		4.5		ns
Switching Characteristics:						
t_{DLAHC}	LACK High Delay after CLKIN High	18 + DT/2	31.5 + DT/2	18 + DT/2	30.5 + DT/2	ns
t_{DLALC}	LACK Low Delay after LCLK High[1]	6	17.8	6	19	ns
Transmit						
Timing Requirements:						
t_{SLACH}	LACK Setup before LCLK High	20.25		19		ns
t_{HLACH}	LACK Hold after LCLK High	−6.5		−6.5		ns
Switching Characteristics:						
t_{DLCLK}	LCLK Delay after CLKIN		9		9	ns
t_{DLDCH}	Data Delay after LCLK High		3.25		2.75	ns
t_{HLDCH}	Data Hold after LCLK High	−2		−2		ns
$t_{LCLKTWL}$	LCLK Width Low	$(t_{CK}/4) - 1$	$(t_{CK}/4) + 1.5$	$(t_{CK}/4) - 0.75$	$(t_{CK}/4) + 1.5$	ns
$t_{LCLKTWH}$	LCLK Width High	$(t_{CK}/4) - 1.5$	$(t_{CK}/4) + 1$	$(t_{CK}/4) - 1.5$	$(t_{CK}/4) + 1$	ns
t_{DLACLK}	LCLK Low Delay after LACK High	$(t_{CK}/4) + 9$	$(3 \times t_{CL}/4) + 17$	$(t_{CK}/4) + 9$	$(3 \times t_{CL}/4) + 17$	ns

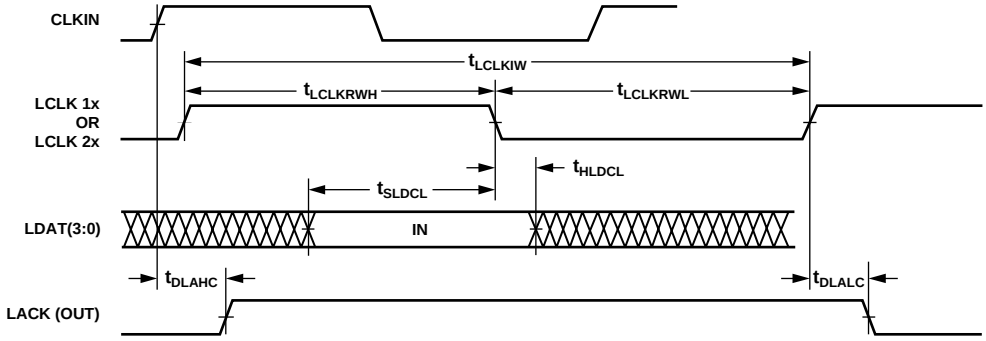
[1] LACK goes low with t_{DLALC} relative to the rising edge of LCLK after the first nibble is received. LACK does not go low, if the receiver's link buffer is not about to fill.

TRANSMIT



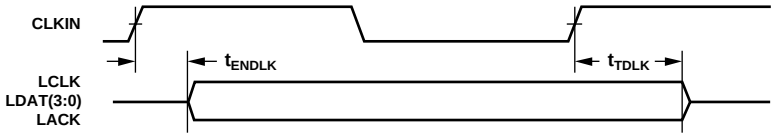
THE t_{SLACH} REQUIREMENT APPLIES TO THE RISING EDGE OF LCLK ONLY FOR THE FIRST NIBBLE TRANSMITTED.

RECEIVE



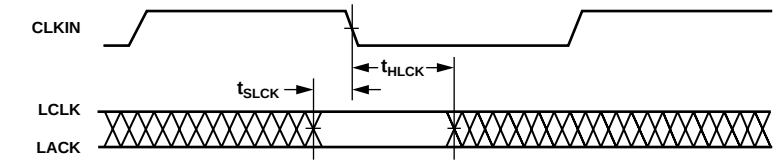
LACK GOES LOW ONLY AFTER THE SECOND NIBBLE IS RECEIVED.

LINK PORT ENABLE/THREE-STATE DELAY FROM INSTRUCTION



LINK PORT ENABLE OR THREE-STATE TAKES EFFECT 2 CYCLES AFTER A WRITE TO A LINK PORT CONTROL REGISTER.

LINK PORT INTERRUPT SETUP TIME



00667-025

Figure 16. Link Ports

Table 18. Serial Ports

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
External Clock						
Timing Requirements:						
t_{SFSE}	TFS/RFS Setup before TCLK/RCLK[1]	4		4		ns
t_{HFSE}	TFS/RFS Hold after TCLK/RCLK[1, 2]	4.5		4.5		ns
t_{SDRE}	Receive Data Setup before RCLK[1]	2		2		ns
t_{HDRE}	Receive Data Hold after RCLK[1]	4.5		4.5		ns
t_{SCLKW}	TCLK/RCLK Width	9.5		9.5		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		t_{CK}		ns
Internal Clock						
Timing Requirements:						
t_{SFSI}	TFS Setup before TCLK[1]; RFS Setup before RCLK[1]	9.5		9.5		ns
t_{HFSI}	TFS/RFS Hold after TCLK/RCLK[1, 2]	1		1		ns
t_{SDRI}	Receive Data Setup before RCLK[1]	4.5		4.5		ns
t_{HDRI}	Receive Data Hold after RCLK[1]	3		3		ns
External or Internal Clock						
Switching Characteristics:						
t_{DFSE}	RFS Delay after RCLK (Internally Generated RFS)[3]		14.5		14.5	ns
t_{HFSE}	RFS Hold after RCLK (Internally Generated RFS)[3]	2.5		2.5		ns
External Clock						
Switching Characteristics:						
t_{DFSE}	TFS Delay after TCLK (Internally Generated TFS)[3]		14.5		14.5	ns
t_{HFSE}	TFS Hold after TCLK (Internally Generated TFS)[3]	3		3		ns
t_{DDTE}	Transmit Data Delay after TCLK[3]		17.5		17.5	ns
t_{HDTE}	Transmit Data Hold after TCLK[3]	5		5		ns
Internal Clock						
Switching Characteristics:						
t_{DFSI}	TFS Delay after TCLK (Internally Generated TFS)[3]		5		5	ns
t_{HFSI}	TFS Hold after TCLK (Internally Generated TFS)[3]	−1.5		−1.5		ns
t_{DDTI}	Transmit Data Delay after TCLK[3]		7.5		7.5	ns
t_{HDTI}	Transmit Data Hold after TCLK[3]	−0.5		−0.5		ns
t_{SCLKIW}	TCLK/RCLK Width	(SCLK/2) − 2	(SCLK/2) + 2	(SCLK/2) − 2.5	(SCLK/2) + 2.5	ns
Enable and Three-State						
Switching Characteristics:						
t_{DDTEN}	Data Enable from External TCLK[3]	3.5		4		ns
t_{DDTTE}	Data Disable from External TCLK[3]		12		12	ns
t_{DDTIN}	Data Enable from Internal TCLK[3]	−0.5		−0.5		ns
t_{DDTTI}	Data Disable from Internal TCLK[3]		3		3	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		23.5 + 3 DT/8		23.5 + 3 DT/8	ns
t_{DPTR}	SPORT Disable after CLKIN		18.5		18.5	ns
Gated SCLK with External TFS (Mesh Multiprocessing)						
Timing Requirements:						
t_{STFSCK}	TFS Setup before CLKIN	5.5		5.5		ns
t_{HTFSCK}	TFS Hold after CLKIN	(TCK/2) + 0.5		(TCK/2) + 0.5		ns

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
External Late Frame Sync						
Switching Characteristics:						
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[4]		14.1		14.3	ns
$t_{DDTENFS}$	Data Enable from Late FS or MCE = 1, MFD = 0[4]	3.0		3.5		ns

To determine whether communication is possible between two devices at clock speed *n*, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

[1] Referenced to sample edge.
[2] RFS hold after RCK when MCE = 1, MFD = 0 is 0.5 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0.5 ns minimum from drive edge.
[3] Referenced to drive edge.
[4] MCE = 1, TFS enable and TFS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.

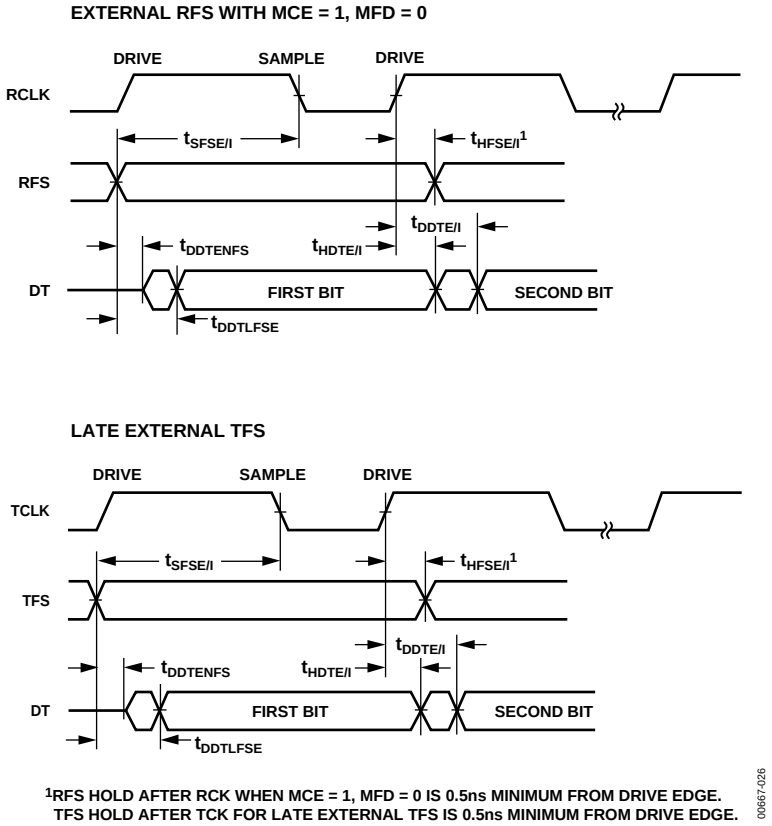


Figure 17. External Late Frame Sync

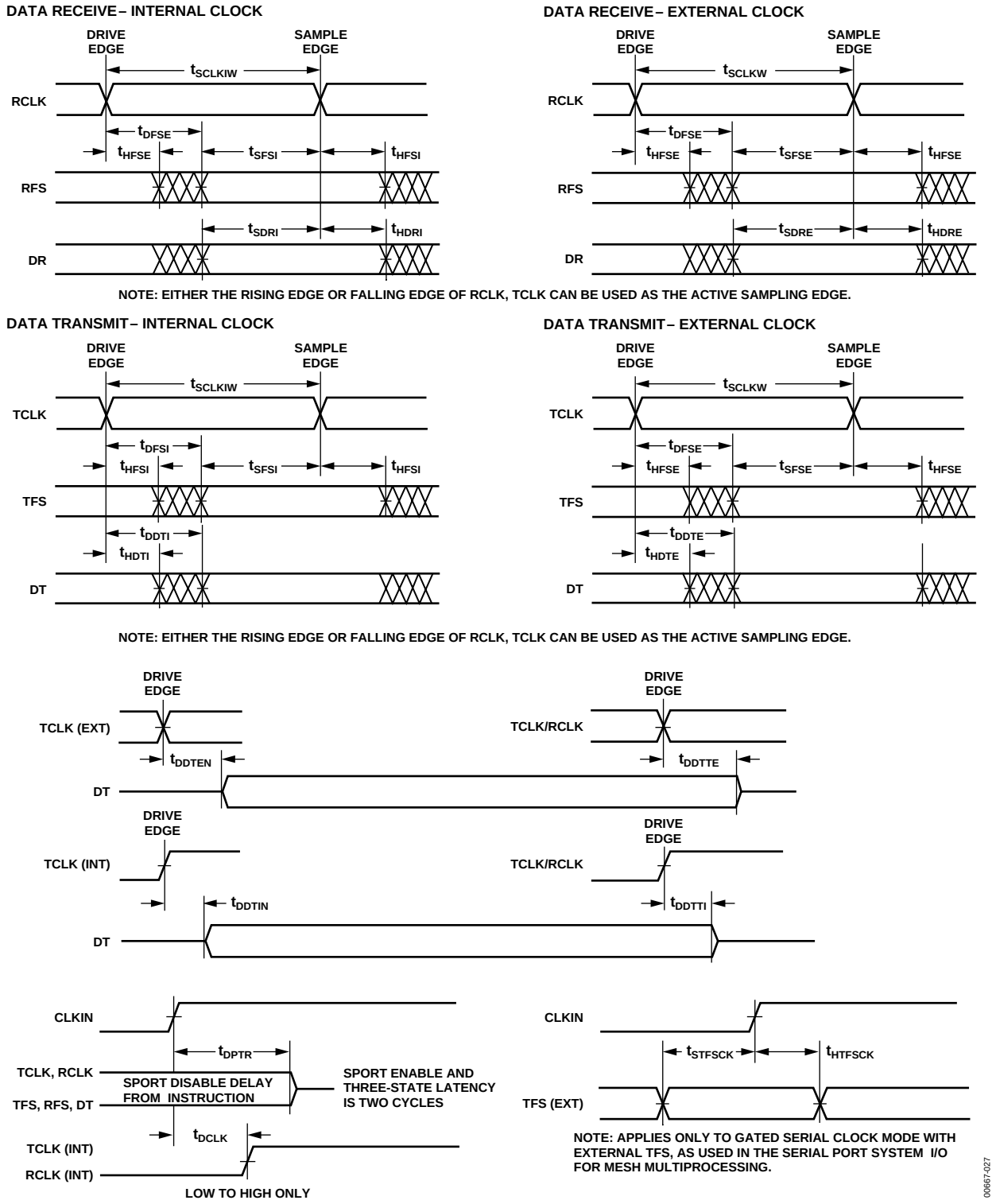


Figure 18. Serial Ports

Table 19. JTAG Test Access Port and Emulation

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements:						
t_{TCK}	TCK Period	t_{CK}		t_{CK}		ns
t_{STAP}	TDI, TMS Setup before TCK High	5				ns
t_{HTAP}	TDI, TMS Hold after TCK High	6		6		ns
t_{SSYS}	System Inputs Setup before TCK Low[1]	7		8		ns
t_{HSYS}	System Inputs Hold after TCK Low[1]	18.5		19		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width	4 t_{CK}		4 t_{CK}		ns
Switching Characteristics:						
t_{DTDO}	TDO Delay from TCK Low		13.5		13.5	ns
t_{DSYS}	System Outputs Delay after TCK Low[2]		20		20	ns

[1] System Inputs = $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{SW}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR_{6-1}}$, RPBA, $\overline{IRQ_{2-0}}$, FLAG2-0, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, CLKIN, $\overline{RESET}$.

[2] System Outputs = $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS_{3-0}}$, $\overline{RD}$, $\overline{WR}$, ACK, PAGE, ADRCLK, $\overline{SW}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR_{6-1}}$, $\overline{CPA}$, $FLAG_{2-0}$, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, $\overline{BMS}$.

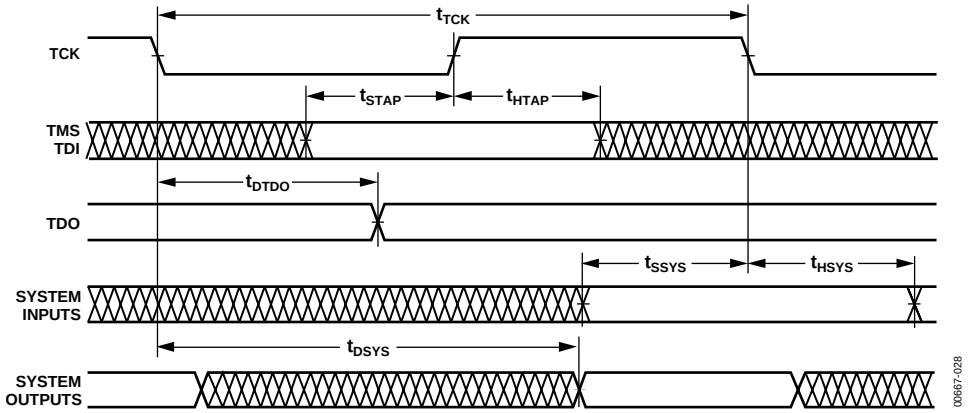


Figure 19. IEEE 11499.1 JTAG Test Access Port

ABSOLUTE MAXIMUM RATINGS

Table 20.

Parameters	Ratings
Supply Voltage (5 V)	−0.3 V to +7 V
Supply Voltage (3.3 V)	−0.3 V to +4.6 V
Input Voltage	−0.5 V to V_{DD} + 0.5 V
Output Voltage Swing	−0.5 V to V_{DD} + 0.5 V
Load Capacitance	200 pF
Junction Temperature under Bias	130°C
Storage Temperature Range	−65°C to +150°C
Lead	280°C

Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

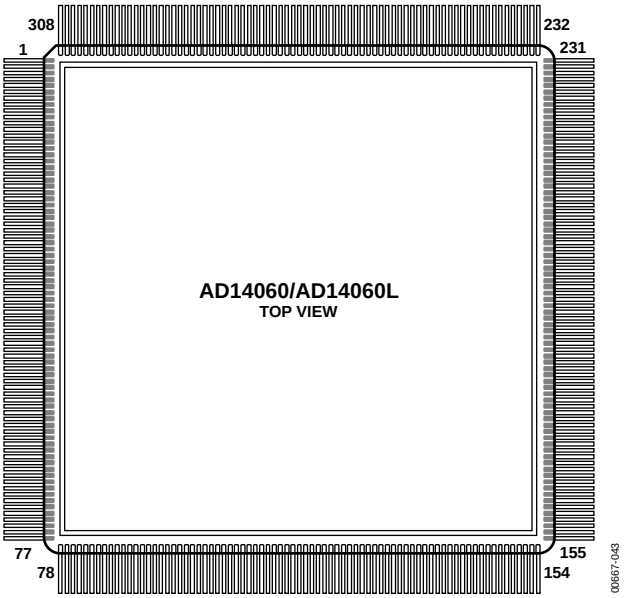


Figure 20. 308-Lead CQFP Pin Configuration

Table 21. Pin Numbers and Mnemonics

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
1	$\overline{WR}$	45	GND	89	ADDR13	133	$\overline{IRQB0}$	177	LC4DAT2	221	GND	265	GND
2	$\overline{RD}$	46	RFSD1	90	ADDR12	134	$\overline{IRQB1}$	178	LC4DAT3	222	LA3ACK	266	DATA24
3	GND	47	RCLKD1	91	ADDR11	135	$\overline{IRQB2}$	179	GND	223	LA3CLK	267	DATA25
4	$\overline{CSA}$	48	DRD1	92	GND	136	GND	180	LC3ACK	224	LA3DAT0	268	DATA26
5	$\overline{CSB}$	49	TFSD1	93	ADDR10	137	$\overline{IRQC0}$	181	LC3CLK	225	LA3DAT1	269	DATA27
6	$\overline{CSC}$	50	TCLKD1	94	ADDR9	138	$\overline{IRQC1}$	182	LC3DAT0	226	LA3DAT2	270	V_{DD}
7	$\overline{CSD}$	51	DTD1	95	ADDR8	139	$\overline{IRQC2}$	183	LC3DAT1	227	LA3DAT3	271	DATA28
8	GND	52	V_{DD}	96	V_{DD}	140	$\overline{IRQD0}$	184	LC3DAT2	228	V_{DD}	272	DATA29
9	$\overline{HBG}$	53	$\overline{HBR}$	97	ADDR7	141	$\overline{IRQD1}$	185	LC3DAT3	229	LA1ACK	273	DATA30
10	REDY	54	$\overline{DMAR1}$	98	ADDR6	142	$\overline{IRQD2}$	186	V_{DD}	230	LA1CLK	274	DATA31
11	ADRCLK	55	$\overline{DMAR2}$	99	ADDR5	143	V_{DD}	187	LC1ACK	231	LA1DAT0	275	GND
12	V_{DD}	56	$\overline{SBTS}$	100	GND	144	EBOOTA	188	LC1CLK	232	LA1DAT1	276	DATA32
13	RFS0	57	$\overline{BMSA}$	101	ADDR4	145	LBOOTA	189	LC1DAT0	233	LA1DAT2	277	DATA33
14	RCLK0	58	$\overline{BMSBCD}$	102	ADDR3	146	EBOOTBCD	190	LC1DAT1	234	LA1DAT3	278	DATA34
15	DR0	59	$\overline{SW}$	103	ADDR2	147	LBOOTBCD	191	LC1DAT2	235	GND	279	DATA35
16	TFS0	60	GND	104	V_{DD}	148	GND	192	LC1DAT3	236	DATA0	280	V_{DD}
17	TCLK0	61	$\overline{MS0}$	105	ADDR1	149	$\overline{RESET}$	193	GND	237	DATA1	281	DATA36
18	DT0	62	$\overline{MS1}$	106	ADDR0	150	RPBA	194	LB4ACK	238	DATA2	282	DATA37
19	GND	63	$\overline{MS2}$	107	FLAGA0	151	GND	195	LB4CLK	239	DATA3	283	DATA38
20	CPAA	64	$\overline{MS3}$	108	GND	152	LD4ACK	196	LB4DAT0	240	V_{DD}	284	DATA39
21	CPAB	65	V_{DD}	109	FLAGA2	153	LD4CLK	197	LB4DAT1	241	DATA4	285	GND
22	CPAC	66	ADDR31	110	FLAGB0	154	LD4DAT0	198	LB4DAT2	242	DATA5	286	DATA40
23	CPAD	67	ADDR30	111	FLAGB2	155	LD4DAT1	199	LB4DAT3	243	DATA6	287	DATA41
24	V_{DD}	68	ADDR29	112	FLAGC0	156	LD4DAT2	200	V_{DD}	244	DATA7	288	CLKIN
25	RFSA1	69	GND	113	FLAGC2	157	LD4DAT3	201	LB3ACK	245	GND	289	GND
26	RCLKA1	70	ADDR28	114	FLAGD0	158	V_{DD}	202	LB3CLK	246	DATA8	290	DATA42
27	DRA1	71	ADDR27	115	FLAGD2	159	LD3ACK	203	LB3DAT0	247	DATA9	291	DATA43
28	TFSA1	72	ADDR26	116	V_{DD}	160	LD3CLK	204	LB3DAT1	248	DATA10	292	V_{DD}
29	TCLKA1	73	V_{DD}	117	FLAG1	161	LD3DAT0	205	LB3DAT2	249	DATA11	293	DATA44
30	DTA1	74	ADDR25	118	$\overline{EMU}$	162	LD3DAT1	206	LB3DAT3	250	V_{DD}	294	DATA45
31	GND	75	ADDR24	119	TIMEXPA	163	LD3DAT2	207	GND	251	DATA12	295	DATA46
32	RFSB1	76	ADDR23	120	TIMEXPB	164	LD3DAT3	208	LB1ACK	252	DATA13	296	DATA47
33	RCLKB1	77	ADDR22	121	TIMEXPC	165	GND	209	LB1CLK	253	DATA14	297	GND
34	DRB1	78	ADDR21	122	TIMEXPD	166	LD1ACK	210	LB1DAT0	254	DATA15	298	$\overline{BR1}$
35	TFSB1	79	ADDR20	123	GND	167	LD1CLK	211	LB1DAT1	255	GND	299	$\overline{BR2}$
36	TCLKB1	80	V_{DD}	124	TDO	168	LD1DAT0	212	LB1DAT2	256	DATA16	300	$\overline{BR3}$
37	DTB1	81	ADDR19	125	$\overline{TRST}$	169	LD1DAT1	213	LB1DAT3	257	DATA17	301	$\overline{BR4}$
38	V_{DD}	82	ADDR18	126	TDI	170	LD1DAT2	214	V_{DD}	258	DATA18	302	$\overline{BR5}$
39	RFSC1	83	ADDR17	127	TMS	171	LD1DAT3	215	LA4ACK	259	DATA19	303	$\overline{BR6}$
40	RCLKC1	84	GND	128	TCK	172	V_{DD}	216	LA4CLK	260	V_{DD}	304	PAGE
41	DRC1	85	ADDR16	129	V_{DD}	173	LC4ACK	217	LA4DAT0	261	DATA20	305	V_{DD}
42	TFSC1	86	ADDR15	130	$\overline{IRQA0}$	174	LC4CLK	218	LA4DAT1	262	DATA21	306	$\overline{DMAG1}$
43	TCLKC1	8	ADDR14	131	$\overline{IRQA1}$	175	LC4DAT0	219	LA4DAT2	263	DATA22	307	$\overline{DMAG2}$
44	DTC1	88	V_{DD}	132	$\overline{IRQA2}$	176	LC4DAT1	220	LA4DAT3	264	DATA23	308	ACK

PIN FUNCTION DESCRIPTIONS

AD14060/AD14060L pin function descriptions are listed in Table 22. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to V_{DD} or GND, except for $ADDR_{31-0}$, $DATA_{47-0}$, $FLAG_{2-0}$, $\overline{SW}$, and inputs that have internal pull-up or pull-down resistors (CPA, ACK, DTx, DRx, TCLKx, RCLKx, $LxDAT_{3-0}$, LxCLK, LxACK, TMS, and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

Table 22. Pin Function Descriptions

Pin	Type[1]	Function
$ADDR_{31-0}$	I/O/T	External Bus Address (common to all SHARCs). The AD14060/AD14060L outputs addresses for external memory and peripherals on these pins. In a multiprocessor system, the bus master outputs addresses for read/writes on the internal memory or IOP registers of slave ADSP-2106xs. The AD14060/AD14060L inputs addresses when a host processor or multiprocessing bus master is reading or writing the internal memory or IOP registers of internal ADSP-21060s.
$DATA_{47-0}$	I/O/T	External Bus Data (common to all SHARCs). The AD14060/AD14060L inputs and outputs data and instructions on these pins. 32-bit single-precision floating-point data and 32-bit fixed-point data is transferred over Bits 47–16 of the bus. 40-bit extended-precision floating-point data is transferred over Bits 47–48 of the bus. 16-bit short word data is transferred over Bits 31–16 of the bus. In PROM boot mode, 8-bit data is transferred over Bits 23–16. Pull-up resistors on unused DATA pins are not necessary.
$\overline{MS}_{3-0}$	O/T	Memory Select Lines (common to all SHARCs). These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the individual ADSP-21060's system control registers (SYSCON). The $\overline{MS}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring, the $\overline{MS}_{3-0}$ lines are inactive. They are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. $\overline{MS}_0$ can be used with the PAGE signal to implement a bank of DRAM memory (Bank 0). In a multiprocessing system, the $\overline{MS}_{3-0}$ lines are output by the bus master.
$\overline{RD}$	I/O/T	Memory Read Strobe (common to all SHARCs). This pin is asserted (low) when the AD14060/AD14060L reads from external devices or when the internal memory of internal ADSP-2106xs is being accessed. External devices (including other ADSP-2106xs) must assert $\overline{RD}$ to read from the AD14060/AD14060L's internal memory. In a multiprocessing system, $\overline{RD}$ is output by the bus master and is input by all other ADSP-2106xs.
$\overline{WR}$	I/O/T	Memory Write Strobe (common to all SHARCs). This pin is asserted (low) when the AD14060/AD14060L writes to external devices or when the internal memory of internal ADSP-2106xs is being accessed. External devices (including other ADSP-2106xs) must assert $\overline{WR}$ to write to the AD14060/ AD14060L's internal memory. In a multiprocessing system, $\overline{WR}$ is output by the bus master and is input by all other ADSP-2106xs.
PAGE	O/T	DRAM Page Boundary. The AD14060/AD16060L asserts this pin to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the individual ADSP-21060's memory control register (WAIT). DRAM can be implemented only in external memory Bank 0. The PAGE signal can be activated only for Bank 0 accesses. In a multiprocessing system, PAGE is output by the bus master.
ADRCLK	O/T	Clock Output Reference (common to all SHARCs). In a multiprocessing system, ADRCLK is output by the bus master.
$\overline{SW}$	I/O/T	Synchronous Write Select (common to all SHARCs). This signal is used to interface the AD14060/AD14060L to synchronous memory devices (including other ADSP-2106xs). The AD14060/AD14060L asserts $\overline{SW}$ (low) to provide an early indication of an impending write cycle, which can be aborted, if $\overline{WR}$ is not later asserted (for example, in a conditional write instruction). In a multiprocessing system, $\overline{SW}$ is output by the bus master and is input by all other ADSP-2106xs to determine if the multiprocessor memory access is a read or write. $\overline{SW}$ is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to the AD14060/AD14060L.
ACK	I/O/S	Memory Acknowledge (common to all SHARCs). External devices can de-assert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The AD14060/AD14060L de-asserts ACK, as an output, to add wait states to a synchronous access of its internal memory. In a multiprocessing system, a slave ADSP-2106x de-asserts the bus master's ACK input to add wait state(s) to an access of its internal memory. The bus master has a keeper latch on its ACK pin that maintains the input at the level to which it was last driven.

Pin	Type[1]	Function
$\overline{SBTS}$	I/S	Suspend Bus Three-State (common to all SHARCs). External devices can assert $\overline{SBTS}$ (low) to place the external bus address, data, selects, and strobes in a high impedance state for the following cycle. If the AD14060/AD14060L attempts to access external memory while $\overline{SBTS}$ is asserted, the processor halts and the memory access does not complete until $\overline{SBTS}$ is de-asserted. $\overline{SBTS}$ should be used only to recover from host processor/AD14060/AD14060L deadlock, or used with a DRAM controller.
$\overline{HBR}$	I/A	Host Bus Request (common to all SHARCs). Must be asserted by a host processor to request control of the AD14060/AD14060L's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the ADSP-2106x that is bus master relinquishes the bus and asserts $\overline{HBG}$. To relinquish the bus, the ADSP-2106x places the address, data, select, and strobe lines in a high impedance state. $\overline{HBR}$ has priority over all ADSP-2106x bus requests ($\overline{BR}_{6-1}$) in a multiprocessing system.
$\overline{HBG}$	I/O	Host Bus Grant (common to all SHARCs). Acknowledges an $\overline{HBR}$ bus request, indicating that the host processor can take control of the external bus. $\overline{HBG}$ is asserted (held low) by the AD14060/AD14060L until $\overline{HBR}$ is released. In a multiprocessing system, $\overline{HBG}$ is output by the ADSP-2106x bus master and is monitored by all others.
$\overline{CSA}$	I/A	Chip Select. Asserted by host processor to select SHARC_A.
$\overline{CSB}$	I/A	Chip Select. Asserted by host processor to select SHARC_B.
$\overline{CSC}$	I/A	Chip Select. Asserted by host processor to select SHARC_C.
$\overline{CSD}$	I/A	Chip Select. Asserted by host processor to select SHARC_D.
REDY (O/D)	O	Host Bus Acknowledge (common to all SHARCs). The AD14060/AD14060L de-asserts REDY (low) to add wait states to an asynchronous access of its internal memory or IOP registers by a host. Open-drain output (O/D) by default; can be programmed in ADREDY bit of SYSCON register of individual ADSP-21060s to be active drive (A/D). REDY is output only if the CS and $\overline{HBR}$ inputs are asserted.
$\overline{BR}_{6-1}$	I/O/S	Multiprocessing Bus Requests (common to all SHARCs). Used by multiprocessing ADSP-2106xs to arbitrate for bus mastership. An ADSP-2106x drives only its own $\overline{BR}$x line (corresponding to the value of its ID2-0 inputs) and monitors all others. In a multiprocessor system with less than six ADSP-2106xs, the unused $\overline{BR}$x pins should be pulled high; $\overline{BR}_{4-1}$ must not be pulled high or low, because they are outputs.
RPBA	I/S	Rotating Priority Bus Arbitration Select (common to all SHARCs). When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection that must be set to the same value on every ADSP-2106x. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every ADSP-2106x.
$\overline{CPA}$y (O/D)	I/O	Core Priority Access (y = SHARC_A, B, C, D). Asserting its $\overline{CPA}$ pin allows the core processor of an ADSP-2106x bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{CPA}$ is an open-drain output that is connected to all ADSP-2106xs in the system, if this function is required. The $\overline{CPA}$ pin of each internal ADSP-21060 is brought out individually. The $\overline{CPA}$ pin has an internal 5 kΩ pull-up resistor. If core access priority is not required in a system, the $\overline{CPA}$ pin should be left unconnected.
DT0	O/T	Data Transmit (common Serial Ports 0 to all SHARCs, TDM). The DT pin has a 50 kΩ internal pull-up resistor.
DR0	I	Data Receive (common Serial Ports 0 to all SHARCs, TDM). The DR pin has a 50 kΩ internal pull-up resistor.
TCLK0	I/O	Transmit Clock (common Serial Ports 0 to all SHARCs, TDM). The TCLK pin has a 50 kΩ internal pull-up resistor.
RCLK0	I/O	Receive Clock (common Serial Ports 0 to all SHARCs, TDM). The RCLK pin has a 50 kΩ internal pull-up resistor.
TFS0	I/O	Transmit Frame Sync (common Serial Ports 0 to all SHARCs, TDM).
RFS0	I/O	Receive Frame Sync (common Serial Ports 0 to all SHARCs, TDM).
DTy1	O/T	Data Transmit (Serial Port 1 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D). The DT pin has a 50 kΩ internal pull-up resistor.
DRy1	I	Data Receive (Serial Port 1 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D). The DR pin has a 50 kΩ internal pull-up resistor.
TCLKy1	I/O	Transmit Clock (Serial Port 1 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D). The TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKy1	I/O	Receive Clock (Serial Port 1 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D). The RCLK pin has a 50 kΩ internal pull-up resistor.
TFSy1	I/O	Transmit Frame Sync (Serial Port 1 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D).
RFSy1	I/O	Receive Frame Sync (Serial Port 1 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D).
FLAGy0	I/O/A	Flag Pins (FLAG0 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D). Each pin is configured via control bits as either an input or an output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.

Pin	Type[1]	Function
FLAG1	I/O/A	Flag Pins (FLAG1 common to all SHARCs). This pin is configured via control bits internal to individual ADSP-21060s as either an input or an output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
FLAGy2	I/O/A	Flag Pins (FLAG2 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D). Each pin is configured via control bits as either an input or an output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
$\overline{\text{IRQ}}$y2-0	I/A	Interrupt Request Lines (individual $\overline{\text{IRQ}}_{2\text{-}0}$ from y = SHARC_A, SHARC_B, SHARC_C, SHARC_D). Can be either edge-triggered or level-sensitive.
$\overline{\text{DMAR1}}$	I/A	DMA Request 1 (DMA Channel 7). Common to SHARC_A, SHARC_B, SHARC_C, SHARC_D.
$\overline{\text{DMAR2}}$	I/A	DMA Request 2 (DMA Channel 8). Common to SHARC_A, SHARC_B, SHARC_C, SHARC_D.
$\overline{\text{DMAG1}}$	O/T	DMA Grant 1 (DMA Channel 7). Common to SHARC_A, SHARC_B, SHARC_C, SHARC_D.
$\overline{\text{DMAG2}}$	O/T	DMA Grant 2 (DMA Channel 8). Common to SHARC_A, SHARC_B, SHARC_C, SHARC_D.
LyxCLK	I/O	Link Port Clock (y = SHARC_A, B, C, D; x = Link Ports 1, 3, 4)[2]. Each LyxCLK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register of the ADSP-20160.
LyxDAT3-0	I/O	Link Port Data (y = SHARC_A, B, C, D; x = Link Ports 1, 3, 4)[2]. Each LyxDAT pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register of the ADSP-21060.
LyxACK	I/O	Link Port Acknowledge (y = SHARC_A, B, C, D; x = Link Ports 1, 3, 4)[2]. Each LyxACK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register of the ADSP-21060.
EBOOTA	I	EPROM Boot Select (SHARC_A). When EBOOTA is high, SHARC_A is configured for booting from an 8-bit EPROM. When EBOOTA is low, the LBOOTA and $\overline{\text{BMSA}}$ inputs determine booting mode for SHARC_A. See the following table. This signal is a system configuration selection that should be hardwired.
LBOOTA	I	Link Boot. When LBOOTA is high, SHARC_A is configured for link port booting. When LBOOTA is low, SHARC_A is configured for host processor booting or no booting. See the following table. This signal is a system configuration selection that should be hardwired.
$\overline{\text{BMSA}}$	I/O/T[3]	Boot Memory Select. When this pin is an output, it is used as chip select for boot EPROM devices (when EBOOTA = 1, LBOOTA = 0). In a multiprocessor system, $\overline{\text{BMS}}$ is output by the bus master. As an input, when low, this pin indicates that no booting is to occur and that SHARC_A is to begin executing instructions from external memory. See the following table. This input is a system configuration selection that should be hardwired.
EBOOTBCD	I	EPROM Boot Select (common to SHARC_B, SHARC_C, SHARC_D). When EBOOTBCD is high, SHARC_B, C, and D are configured for booting from an 8-bit EPROM. When EBOOTBCD is low, the LBOOTBCD and $\overline{\text{BMSBCD}}$ inputs determine booting mode for SHARC_B, C, and D. See the following table. This signal is a system configuration selection that should be hardwired.
LBOOTBCD	I	LINK Boot (common to SHARC_B, SHARC_C, SHARC_D). When LBOOTBCD is high, SHARC_B, C, and D are configured for link port booting. When LBOOTBCD is low, SHARC_B, C, and D are configured for host processor booting or no booting. See the following table. This signal is a system configuration selection that should be hardwired.
$\overline{\text{BMSBCD}}$	I/O/T[3]	Boot Memory Select. When this pin is an output, it is used as chip select for boot EPROM devices (when EBOOTBCD = 1, LBOOTBCD = 0). In a multiprocessor system, $\overline{\text{BMS}}$ is output by the bus master. As an input, when low, this pin indicates that no booting is to occur and that SHARC_B, C, and D are to begin executing instructions from external memory. See table below. This input is a system configuration selection that should be hardwired.

EBOOT	LBOOT	$\overline{\text{BMS}}$	Booting Mode
1	0	Output	EPROM (connect $\overline{\text{BMS}}$ to EPROM chip select).
0	0	1 (Input)	Host processor.
0	1	1 (Input)	Link port.
0	0	0 (Input)	No booting. Processor executes from external memory.
0	1	0 (Input)	Reserved.
1	1	x (Input)	Reserved.

TIMEXPy	O	Timer Expired (individual TIMEXP from y = SHARC_A, SHARC_B, SHARC_C, SHARC_D). Asserted for four cycles when the timer is enabled and TCOUNT decrements to 0.
CLKIN	I	Clock In (common to all SHARCs). External clock input to the AD14060/AD14060L. The instruction cycle rate is equal to CLKIN. CLKIN cannot be halted, changed, or operated below the minimum specified frequency.
$\overline{\text{RESET}}$	I/A	Module Reset (common to all SHARCs). Resets the AD14060/AD14060L to a known state. This input must be asserted (low) at power-up.
TCK	I	Test Clock (JTAG) (common to all SHARCs). Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	Test Mode Select (JTAG) (common to all SHARCs). Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.

Pin	Type[1]	Function
TDI	I/S	Test Data Input (JTAG). Provides serial data for the boundary scan logic chain starting at SHARC_A. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	Test Data Output (JTAG). Serial scan output of the boundary scan chain path, from SHARC_D.
$\overline{\text{TRST}}$	I/A	Test Reset (JTAG) (common to all SHARCs). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the AD14060/AD14060L. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$ (O/D)	O	Emulation Status (common to all SHARCs). Must be connected to the ADSP-2106x EZ-ICE target board connector only.
V_{DD}	P	Power Supply. Nominally 5.0 V dc for 5 V devices or 3.3 V dc for 3.3 V devices (26 pins).
GND	G	Power Supply Return (28 pins).

FLAG3 is connected internally, common to SHARC_A, B, C, and D.
ID pins are hardwired internally as shown in Figure 1.

[1] I = input; P = power supply; (A/D) = active drive; O = output; S = synchronous; (O/D) = open drain; G = ground; A = asynchronous; T = three-state, when $\overline{\text{SBTS}}$ is asserted, or when the AD14060/AD14060L is a bus slave.
[2] Link Ports 0, 2, and 5 are connected internally, as described in the Link Port I/O section.
[3] Three-statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output).

DETAILED DESCRIPTION

ARCHITECTURAL FEATURES

ADSP-21060 Core

The AD14060/AD14060L is based on the powerful ADSP-21060 (SHARC) DSP chip. The ADSP-21060 SHARC combines a high performance floating-point DSP core with integrated, on-chip system features, including a 4-Mbit SRAM memory, host processor interface, DMA controller, serial ports, and both link port and parallel bus connectivity for glueless DSP multiprocessing (see Figure 21). It is fabricated in a high speed, low power CMOS process, and has a 25 ns instruction cycle time. The arithmetic/logic unit (ALU), multiplier, and shifter all perform single-cycle instructions, and the three units are arranged in parallel, maximizing computational throughput.

The SHARC features an enhanced Harvard architecture, in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data. An on-chip instruction cache selectively caches only those instructions whose fetches conflict with the PM bus data accesses. This combines with the separate program and data memory buses to enable 3-bus operation for fetching an instruction and two operands, all in a single cycle. The SHARC also contains a general-purpose data register file, which is a 10-port, 32-register (16 primary, 16 secondary) file. Each SHARC's core also implements two data address generators (DAGs), implementing circular data buffers in hardware. The DAGs contain sufficient registers to allow the creation of up to 32 circular buffers. The 48-bit instruction word accommodates a variety of parallel operations for concise programming. For example, the ADSP-21060 can conditionally execute a multiply, an add, a subtract, and a branch, all in a single instruction.

The SHARCs contain 4 Mbits of on-chip SRAM each, organized as two blocks of 2 Mbits, which can be configured for different combinations of code and data storage. The memory can be configured as a maximum of 128k words of 32-bit data, 256k words of 16-bit data, 80k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 4 Mbits. A 16-bit floating-point storage format is supported, which effectively doubles the amount of data that can be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction. Each memory block is dual-ported for single-cycle, independent access by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from the I/O, all in a single cycle.

SHARED MEMORY MULTIPROCESSING

The AD14060/AD14060L takes advantage of the powerful multiprocessing features built into the SHARC. The SHARCs are connected to maximize the performance of this cluster-of-four architecture, and still allow for off-module expansion. The AD14060/AD14060L in itself is a complete shared memory multiprocessing system, as shown in Figure 22. The unified address space of the SHARCs allows direct interprocessor accesses of each SHARCs' internal memory. In other words, each SHARC can directly access the internal memory and IOP registers of each of the other SHARCs by simply reading or writing to the appropriate address in multiprocessor memory space (see Figure 23)—this is called a direct read or direct write.

Bus arbitration is accomplished with the on-SHARC arbitration logic. Each SHARC has a unique ID, and drives the bus-request ($\overline{BR}$) line corresponding to its ID, while monitoring all others. $\overline{BR1}$ to $\overline{BR4}$ are used within the AD14060/AD14060L, while $\overline{BR5}$ and $\overline{BR6}$ can be used for expansion. All bus requests ($\overline{BR1}$ to $\overline{BR6}$) are included in the module I/O. Two different priority schemes, fixed and rotating, are available to resolve competing bus requests. The RPBA pin selects which scheme is used. When RPBA is high, rotating priority bus arbitration is selected; when RPBA is low, fixed priority is selected.

Bus mastership is passed from one SHARC to another during a bus transition cycle. A bus transition cycle occurs only when the current bus master de-asserts its BR line and one of the slave SHARCs asserts its BR line. The bus master can, therefore, retain bus mastership by keeping its BR line asserted. When the bus master de-asserts its BR line and no other BR line is asserted, then the master does not lose any bus cycles. When more than one SHARC asserts its BR line, the SHARC with the highest priority request becomes bus master on the following cycle. Each SHARC observes all the BR lines, and, therefore, tracks when a bus transition cycle has occurred, and which processor has become the new bus master. Master processor changeover incurs only one cycle of overhead. Table 23 shows an example of a bus transition sequence.

Table 23. Rotating Priority Arbitration Example

	Hardware Processor IDs						
Cycle	**ID1**	**ID2**	**ID3**	**ID4**	**ID5**	**ID6**	**Priority**
1	M	1	2 BR	3	4	5	Initial priority assignments
2	4	5 BR	M-BR	1	2	3	
3	4	5 BR	M	1	2	3	
4	5 BR	M	1	2	3	4 BR	
5	1 BR	2	3	4	5	M	Final priority assignments

1–5 = Assigned priority.
M = Bus mastership (in that cycle).
BR = Requesting bus mastership with $\overline{BR}$x.

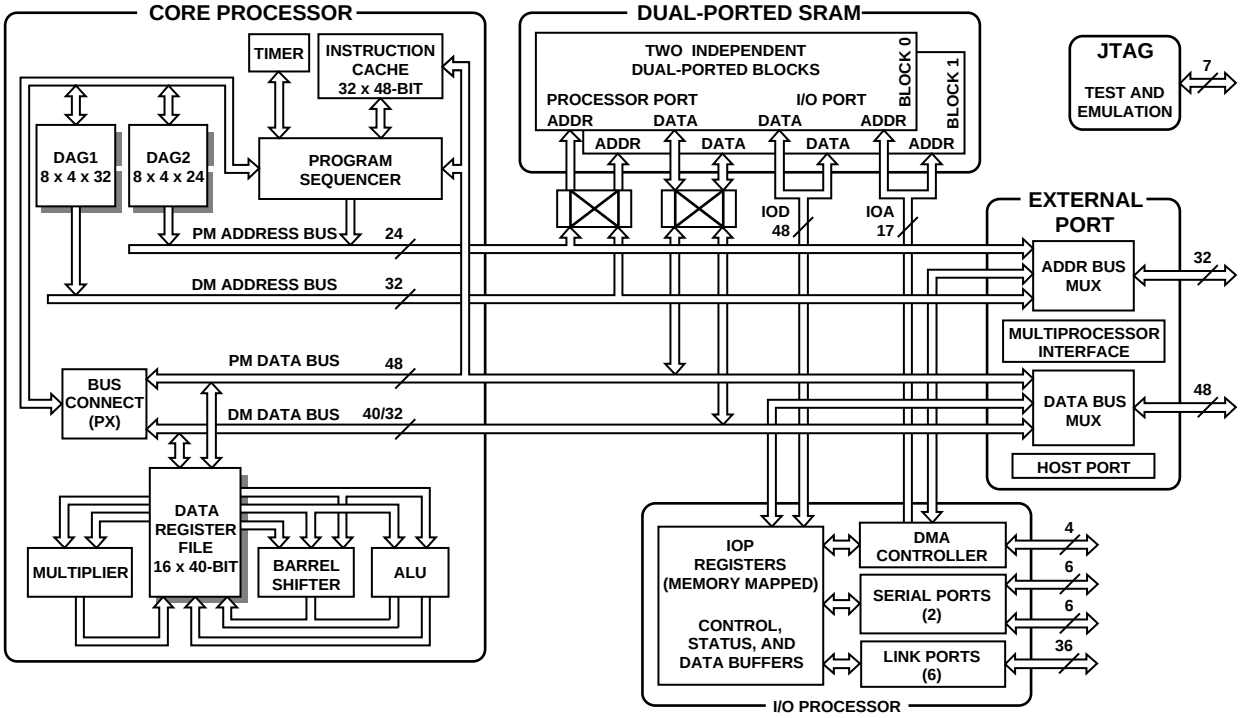


Figure 21. ADSP-21060 Processor Block Diagram (Core of AD10460)

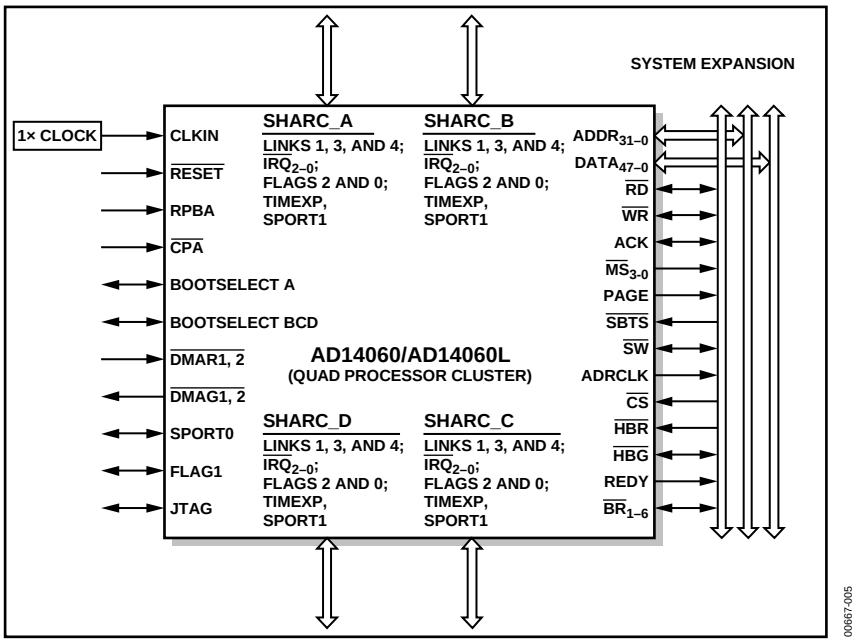


Figure 22. Complete Shared Memory Multiprocessing System

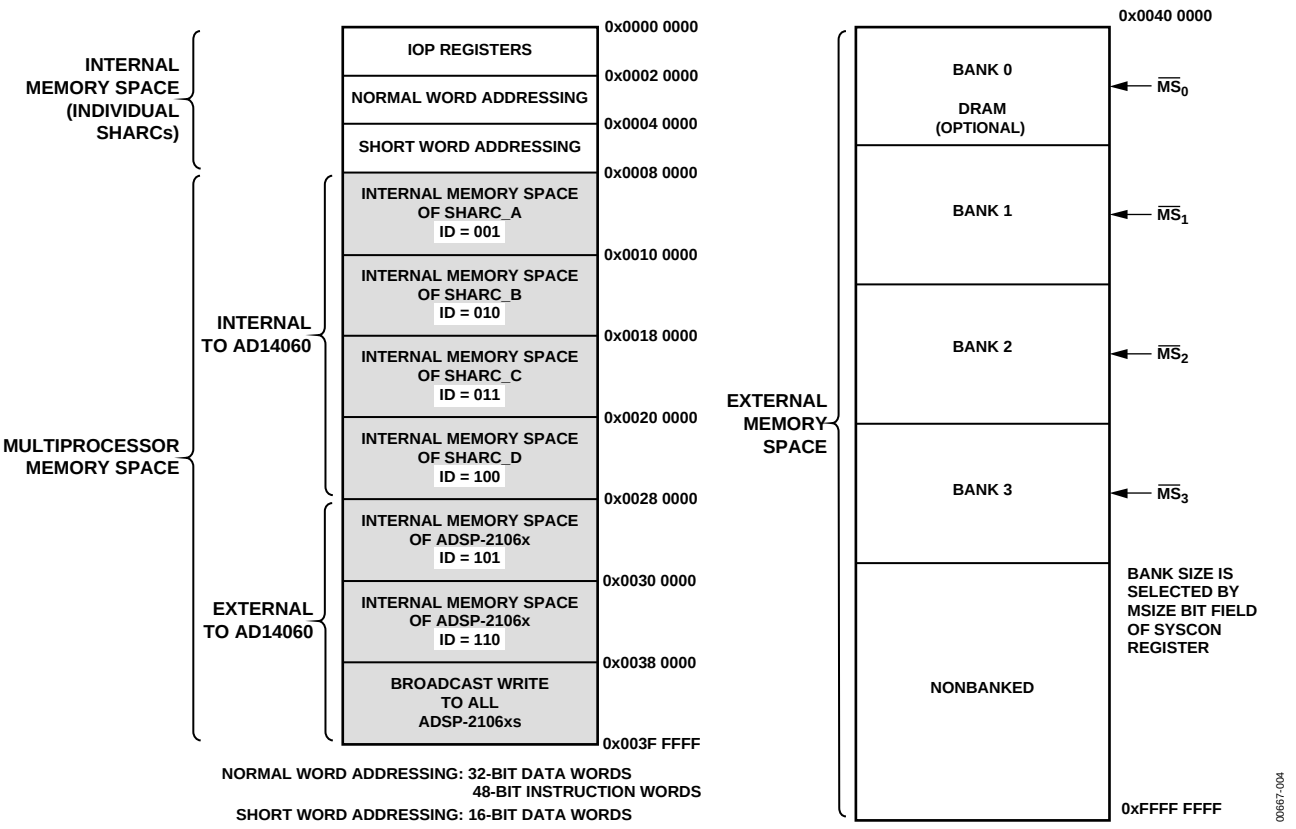


Figure 23. AD14060/AD14060L Memory Map

Bus locking is possible, allowing indivisible read-modify-write sequences for semaphores. In either the fixed or rotating priority scheme, it is also possible to limit the number of cycles that the master can use to control the bus. The AD14060/AD14060L provides the option of using the core priority access (CPA) mode of the SHARC. Using the CPA signal allows external bus accesses by the core processor of a slave SHARC to take priority over ongoing DMA transfers. Also, each SHARC can broadcast write to all other SHARCs simultaneously, allowing the implementation of reflective semaphores.

The bus master can communicate with slave SHARCs by writing messages to their internal IOP registers. The MSRG0 to MSRG7 registers are general-purpose registers that can be used for convenient message passing, semaphores, and resource sharing among the SHARCs. For message passing, the master communicates with a slave by writing and/or reading any of the eight message registers on the slave. For vector interrupts, the master can issue a vector interrupt to a slave by writing the address of an interrupt service routine to the slave's VIRPT register. This causes an immediate high priority interrupt on the slave, which, when serviced, causes it to branch to the specified service routine.

OFF-MODULE MEMORY AND PERIPHERALS INTERFACE

The AD14060/AD14060L's external port provides the interface to off-module memory and peripherals (see Figure 24). This port consists of the complete external port bus of the SHARC, bused in common among the four SHARCs.

The 4-gigaword off-module address space is included in the ADSP-14060's unified address space. Addressing of external memory devices is facilitated by each SHARC internally decoding the high-order address lines to generate memory-bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The AD14060/AD14060L also supports programmable memory wait states and external memory acknowledge controls to allow interfacing to DRAM and peripherals with variable access, hold, and disable time requirements.

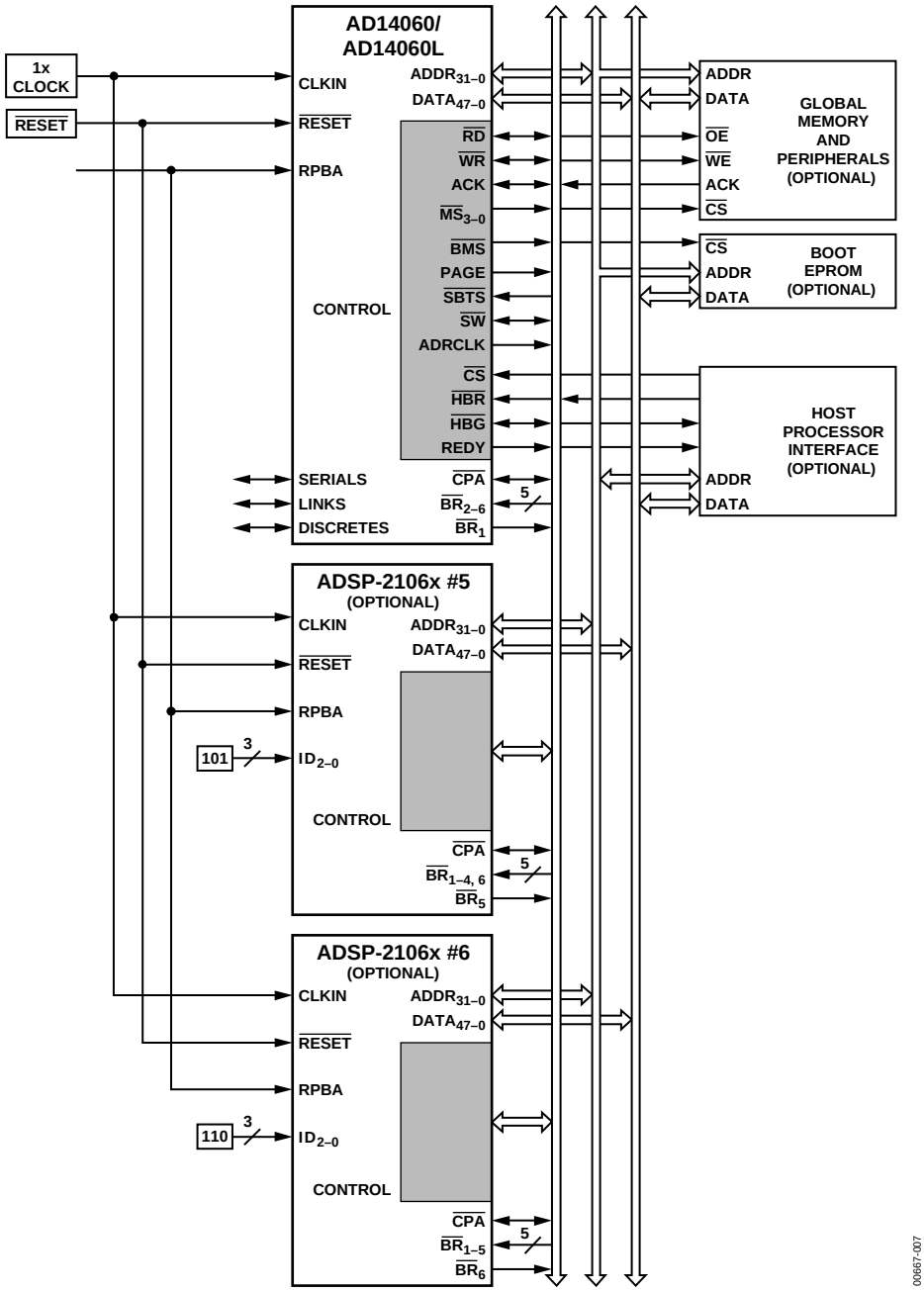


Figure 24. Optional System Interconnections

LINK PORT I/O

Each individual SHARC features six 4-bit link ports that facilitate SHARC-to-SHARC communication and external I/O interfacing. Each link port can be configured for either 1× or 2× operation, allowing each to transfer either four or eight bits per cycle.

The link ports can operate independently and simultaneously, with a maximum bandwidth of 40 MBytes/s each, or a total of 240 MBytes/s per SHARC.

The AD14060/AD14060L optimizes the link port connections internally, and brings a total of 12 of the link ports off-module for user-defined system connections. Internally, each SHARC has a connection to the other three SHARCs with a dedicated link port interface. Thus, each SHARC can directly interface with its nearest and next-nearest neighbor. The remaining three link ports from each SHARC are brought out independently from each SHARC. A maximum of 480 MBytes/s link port bandwidth is then available off of the AD14060/AD14060L. The link port connections are shown in Figure 25.

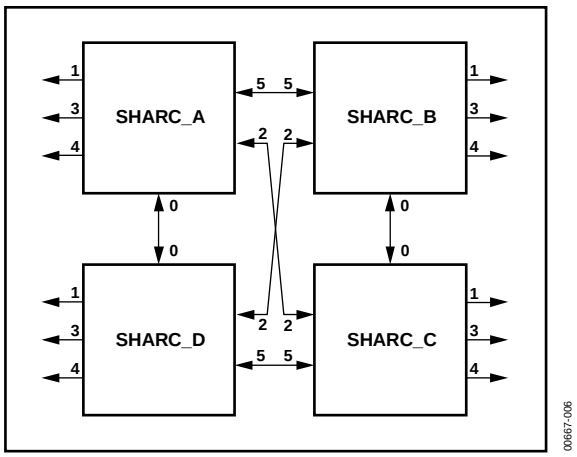


Figure 25. Link Port Connections

Link Port 4, the boot-link port, is brought off independently from each SHARC. Individual booting is then allowed, or chained link-port booting is possible, as described in the Multiprocessor Link-Port Booting section.

Link port data is packed into 32-bit or 48-bit words, and can be directly read by the SHARC core processor or DMA transferred to on-SHARC memory.

Each link port has its own double-buffered input and output registers. Clock/acknowledge handshaking controls link port transfers. Transfers are programmable as either transmit or receive.

SERIAL PORTS

The SHARC serial ports provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. Each SHARC has two serial ports. The AD14060/AD14060L provides direct access to Serial Port 1 of each SHARC. Serial Port 0 is bused in common to each SHARC, and brought off-module.

The serial ports can operate at the full clock rate of the module, providing each with a maximum data rate of 40 Mbit/s. Independent transmit and receive functions provide more flexible communications. Serial port data can be automatically transferred to and from on-SHARC memory via DMA, and each of the serial ports offers time-division-multiplexed (TDM) multichannel mode.

The serial ports can operate with little-endian or big-endian transmission formats, with word lengths selectable from 3 bits to 32 bits. They offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated.

PROGRAM BOOTING

The AD14060/AD14060L supports automatic downloading of programs following power-up or a software reset. The SHARC offers the following options for program booting:

- From an 8-bit EPROM
- From a host processor
- Through the link ports
- No boot

In no-boot mode, the SHARC starts executing instructions from Address 0x0040 0004 in external memory. The boot mode is selected by the state of the following signals: $\overline{\text{BMS}}$, EBOOT, and LBOOT.

On the AD14060/AD14060L, SHARC_A's boot mode is separately controlled, while SHARC_B, C, and D are controlled as a group. With this flexibility, the AD14060/AD14060L can be configured to boot using any of the following methods.

Multiprocessor Host Booting

To boot multiple ADSP-21060 processors from a host, each ADSP-21060 must have its EBOOT, LBOOT, and $\overline{\text{BMS}}$ pins configured for host booting: EBOOT = 0, LBOOT = 0, and $\overline{\text{BMS}}$ = 1. After system power-up, each ADSP-21060 is in the idle state and the $\overline{\text{BR}}$x bus request lines are de-asserted. The host must assert the $\overline{\text{HBR}}$ input and boot each ADSP-21060 by asserting its CS pin and downloading instructions.

Multiprocessor EPROM Booting

The following methods boot the multiprocessor system from an EPROM:

- **SHARC_A is booted, which then boots the others.**

  The EBOOT pin on the SHARC_A must be set high for EPROM booting. All other ADSP-21060s should be configured for host booting (EBOOT = 0, LBOOT = 0, and $\overline{\text{BMS}}$ = 1), which leaves them in the idle state at startup and allows SHARC_A to become bus master and boot itself. Only the $\overline{\text{BMS}}$ pin of SHARC_A is connected to the chip select of the EPROM. When SHARC_A has finished booting, it can boot the remaining ADSP-21060s by writing to their external port DMA Buffer 0 (EPB0) via multiprocessor memory space.

- **All ADSP-21060s boot in turn from a single EPROM.**

  The $\overline{\text{BMS}}$ signals from each ADSP-21060 can be wire-OR'ed together to drive the chip select pin of the EPROM. Each ADSP-21060 can boot in turn, according to its priority. When the last one has finished booting, it must inform the others (which can be in the idle state) that program execution can begin.

Multiprocessor Link-Port Booting

Booting can also be accomplished from a single source through the link ports. Link Buffer 4 must always be used for booting. To simultaneously boot all the ADSP-21060s, a parallel common connection is available through Link Port 4 on each of the processors. Or, using the daisy-chain connection that exists between the processors' link ports, each ADSP-21060 can boot the next one in turn. In this case, the link assignment register (LAR) must be programmed to configure the internal link ports with Link Buffer 4.

Multiprocessor Booting from External Memory

If external memory contains a program after reset, then SHARC_A should be set up for no-boot mode. It begins executing from Address 0x0040 0004 in external memory. When booting has completed, the other ADSP-21060s can be booted by SHARC_A, if they are set up for host booting; or they can begin executing out of external memory, if they are set up for no-boot mode. Multiprocessor bus arbitration allows this booting to occur in an orderly manner.

HOST PROCESSOR INTERFACE

The AD14060/AD14060L's host interface allows easy connection to standard microprocessor buses, both 16-bit and 32-bit, with little additional hardware required. Asynchronous transfers at speeds of up to the full clock rate of the module are supported. The host interface is accessed through the AD14060/AD14060L external port and is memory-mapped into the unified address space. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the AD14060/AD14060L's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the internal memory of the SHARCs, and can access the DMA channel setup and mailbox registers. Vector interrupt support is provided for efficient execution of host commands.

DIRECT MEMORY ACCESS (DMA) CONTROLLER

The SHARCs' on-chip DMA control logic allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to each SHARC's processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

DMA transfers can occur between SHARC internal memory and either external memory, external peripherals, or a host processor. DMA transfers can also occur between the SHARC's internal memory and its serial ports or link ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32- or 48-bit words is performed during DMA transfers.

Ten channels of DMA are available on the SHARCs: two via the link ports, four via the serial ports, and four via the processor's external port (for either host processor, other SHARCs, memory, or I/O transfers). Four additional link port DMA channels are shared with Serial Port 1 and the external port. Programs can be downloaded to the SHARCs using DMA transfers. Asynchronous off-module peripherals can control two DMA channels using DMA request/grant lines ($\overline{\text{DMAR}}$1-2, $\overline{\text{DMAG}}$1-2). Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

APPLICATIONS

DEVELOPMENT TOOLS

The AD14060/AD14060L is supported with a complete set of software and hardware development tools, including an in-circuit emulator and development software.

Analog Devices, Inc. (ADI) uses VisualDSP++®, which is an easy-to-use integrated software development and debugging environment (IDDE) that efficiently manages projects from start to finish from within a single interface.

The ADSP-21262 EZ-KIT LITE™ provides developers with a cost-effective method for initial evaluation of the ADSP-2106x SHARC processor architecture for applications via a USB-based PC-hosted tool set. With this EZ-KIT LITE, users can learn about ADI's ADSP-2106x hardware and software development and can quickly prototype applications.

The EZ-KIT LITE includes an ADSP-2106x processor desktop evaluation board, along with an evaluation suite of the VisualDSP++ development and debugging environment with the C/C++ compiler, assembler, and linker. VisualDSP++ development and debugging software, along with the USB-based debugger interface, enables users to perform standard debugging functions (such as read and write memory, read and write registers, load and execute executables, set and clear breakpoints, and single-step assembly, C, and C++ source code).

The ADI cost-effective universal serial bus (USB)-based emulator and high performance (HP) universal serial bus (USB)-based emulator each provide an easy, portable, non-intrusive, target-based debugging solution for ADI JTAG processors and DSPs. These powerful USB-based emulators perform a wide range of emulation functions, including single-step and full speed execution with predefined breakpoints, and viewing and altering of register and memory contents. With the ability to automatically detect and support multiple I/O voltages, the USB and HP USB emulators enable users to communicate with all the ADI JTAG processors and DSPs using either a full speed USB 1.1 or high speed USB 2.0 port on the host PC. Applications and data can be easily and rapidly tested and transferred between the emulators and the separately available VisualDSP++ development and debugging environment (sold separately).

The plug-and-play architecture of the USB allows the host operating system to automatically detect and configure the emulators. The USB can be connected to and disconnected from the host without opening the PC or turning off the power to the PC. A 3-meter cable is included to connect the emulators to the host PC, providing abundant accessibility to hard-to-reach targets.

The HP USB-based emulator supports the background telemetry channel (BTC), a nonintrusive method for exchanging data between the host and target application without affecting the target system's real-time characteristics. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface. The emulator does not affect target system loading or timing.

Further details and ordering information are available on the analog.com Web site.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Hardware tools include SHARC PC plug-in cards, multiprocessor SHARC VME boards, and daughter card modules with multiple SHARCs and additional memory. These modules are based on the SHARCPAC module specification. Third-party software tools include an Ada compiler, DSP libraries, operating systems, and block diagram design tools.

QUAD-SHARC DEVELOPMENT BOARD

The BlackTip-MCM, AD14060 development board with software is available from Bittware Research Systems, Inc. This board has one AD14060 BITSI interface, and PROM and SRAM expansion options on an ISA card. It is supported by Bittware's SHARC software development package. To contact Bittware, call 1-800-848-0436.

OTHER PACKAGE DETAILS

The AD14060/AD14060L contains 16 on-module 0.018 µF bypass capacitors. It is recommended that, in the target system, at least four additional capacitors of 0.018 µF value be placed around the module, one near each of the four corners.

The top surface (lid) of the AD14060/AD14060L is electrically connected to GND on the industrial and military grade parts.

TARGET BOARD CONNECTOR FOR EMULATOR PROBE

The ADSP-2106x emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x to monitor and control the target board processor during emulation. The emulator probe requires that the AD14060/AD14060L's CLKIN (optional), TMS, TCK, $\overline{\text{TRST}}$, TDI, TDO, $\overline{\text{EMU}}$, and GND signals be made accessible on the target system via a 14-pin connector (pin strip header) similar to Figure 26. The emulator probe plugs directly into this connector for chip-on-board emulation. You must add this connector to your target board design, if you intend to use the ADSP-2106x emulator. The length of the traces between the connector and the AD14060/AD14060L's JTAG pins should be as short as possible.

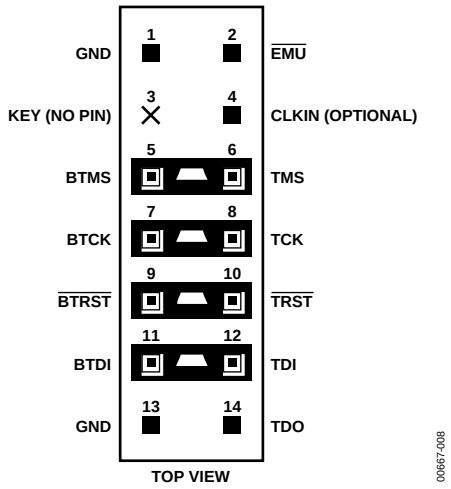


Figure 26. Target Board Connector for ADSP-2106x Emulator (Jumpers in Place)

The 14-pin, 2-row pin-strip header is keyed at the Pin 3 location; Pin 3 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 inch × 0.1 inch. Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

The BTMS, BTCK, $\overline{\text{BTRST}}$, and BTDI signals are provided so that the test access port can also be used for board-level testing. When the connector is not being used for emulation, place jumpers between the Bxxx pins and the other pins, as shown in Figure 26. If you are not going to use the test access port for board testing, tie $\overline{\text{BTRST}}$ to GND and tie or pull up BTCK to V_{DD}. The $\overline{\text{TRST}}$ pin must be asserted after power-up (through $\overline{\text{BTRST}}$ on the connector) or held low for proper operation of the AD14060/AD14060L. None of the Bxxx pins (Pins 5, 7, 9, 11) are connected on the emulator probe.

The JTAG signals are terminated on the emulator probe as listed in Table 24.

Figure 27 shows JTAG scan path connections for the multiprocessor system.

Table 24. JTAG Signals

Signal	Termination
TMS	Driven through 22 Ω resistor (16 µA to 3.2 µA driver).
TCK	Driven at 10 MHz through 22 Ω resistor (16 µA to 3.2 µA driver).
$\overline{\text{TRST}}$	Driven by open-drain driver[1] (pulled up by on-chip 20 kΩ resistor).
TDI	Driven by 16 µA to 3.2 µA driver.
TDO	One TTL load, no termination.
CLKIN	One TTL load, no termination (optional signal).
$\overline{\text{EMU}}$	4.7 kΩ pull-up resistor, one TTL load (open-drain output from ADSP-2106x).

[1] $\overline{\text{TRST}}$ is driven low until the emulator probe is turned on by the emulator software (after the invocation command).

Connecting CLKIN to Pin 4 of the emulator header is optional. The emulator uses CLKIN only when directed to perform operations such as starting, stopping, and single-stepping multiple ADSP-2106xs in a synchronous manner. If these operations do not need to occur synchronously on the multiple processors, tie Pin 4 of the emulator header to ground.

If synchronous multiprocessor operations are needed and CLKIN is connected, clock skew between the AD14060/AD14060L and the CLKIN pin on the emulator header must be minimal. If the skew is too large, synchronous operations might be off by one cycle between processors. For synchronous multiprocessor operation, TCK, TMS, CLKIN, and $\overline{\text{EMU}}$ should be treated as critical signals in terms of skew, and should be laid out as short as possible on the board.

If TCK, TMS, and CLKIN are driving a large number of ADSP-2106x's (more than eight) in the system, treat them as a clock tree using multiple drivers to minimize skew. (See the *ADSP-2106x User's Manual* for details).

If synchronous multiprocessor operations are not needed (CLKIN is not connected), use appropriate parallel termination on TCK and TMS. Note that TDI, TDO, $\overline{\text{EMU}}$, and $\overline{\text{TRST}}$ are not critical signals in terms of skew.

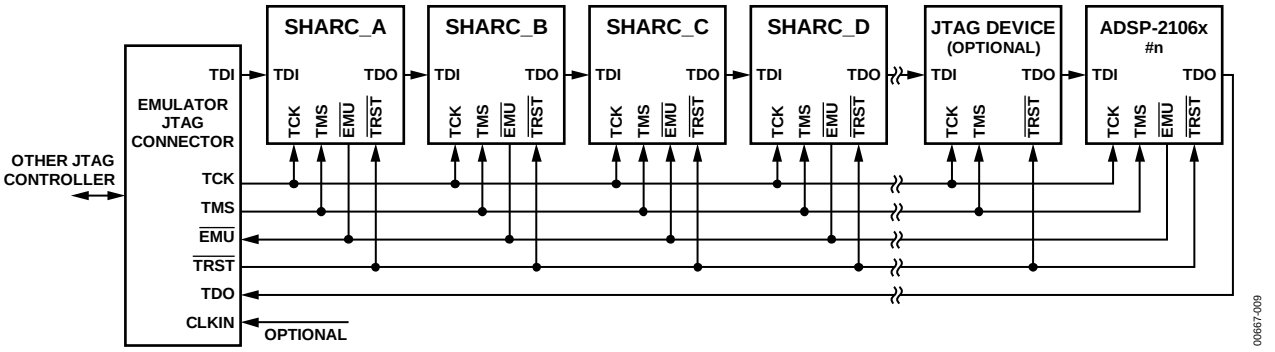


Figure 27. JTAG Scan Path Connections for the AD14060/AD14060L

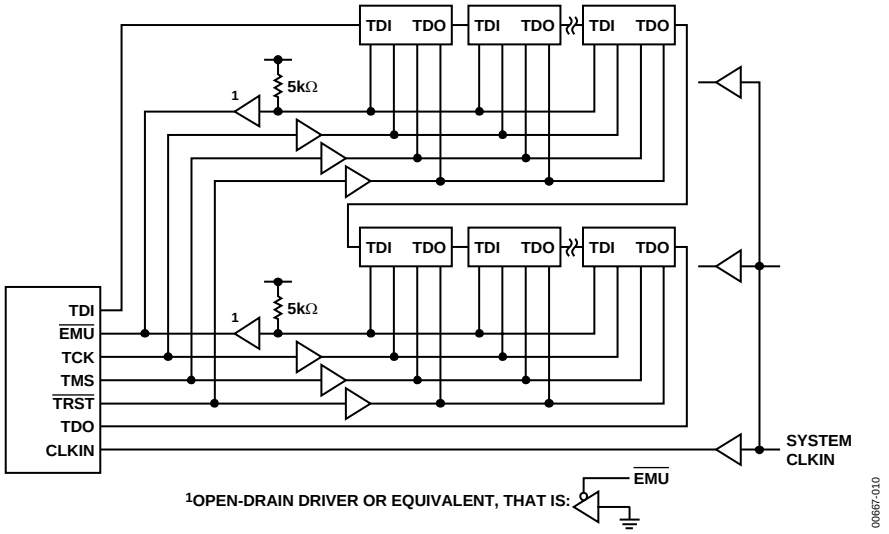


Figure 28. JTAG Clock Tree for Multiple ADSP-2106x Systems

OUTPUT DRIVE CURRENTS

Figure 29 shows typical I-V characteristics for the output drivers of the ADSP-2106x. The curves represent the current drive capability of the output drivers as a function of output voltage.

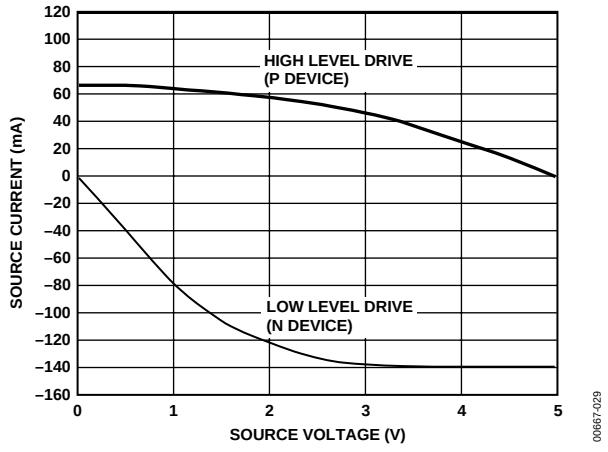


Figure 29. ADSP-2106x Typical Drive Currents (V_{DD} = 5 V)

POWER DISSIPATION

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated as follows:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on the following:

- Number of output pins that switch during each cycle (O)
- Maximum frequency at which they can switch (f)
- Load capacitance (C)
- Voltage swing (V_{DD})

and is calculated by

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (C_{IN}). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2\ t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2\ t_{CK})$, but selects can switch on each cycle.

Example

Estimate P_{EXT} with the following assumptions: a system with one bank of external data memory RAM (32-bit); four 128k × 8 RAM chips are used, each with a load of 10 pF; external data memory writes occur every other cycle; a rate of $1/(4\ t_{CK})$ with 50% of the pins switching; and an instruction cycle rate is 40 MHz (t_{CK} = 25 ns) and V_{DD} = 5.0 V.

The P_{EXT} equation is calculated for each class of pins that can drive, as shown in Table 25.A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 5.0\ V)$$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all 1s to all 0s. It is uncommon for an application to have 100% or even 50% of the outputs switching simultaneously.

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L, and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L\ \Delta V}{I_L}$$

The output disable time, t_{DIS}, is the difference between $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 30. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time, t_{ENA}, is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the output enable/disable diagram (Figure 30). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

System Hold Time Calculation Example

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the previous equation. Choose ΔV to be the difference between the ADSP-2106x's output voltage and the input threshold for the device requiring the hold time. A typical ΔV is 0.4 V. C_L is the total bus capacitance per data line, and I_L is the total leakage or three-state current per data line. The hold time is t_{DECAY} plus the minimum disable time (t_{HDWD} for the write cycle).

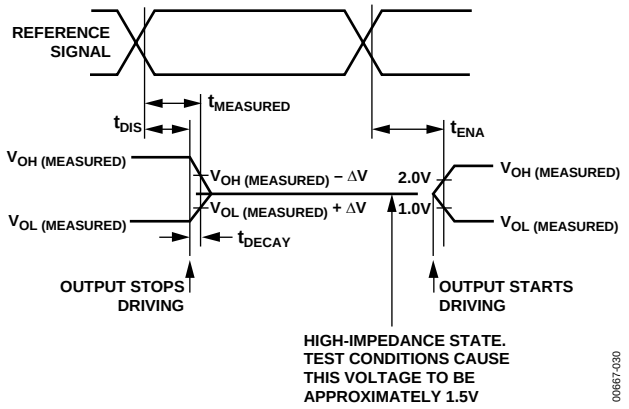


Figure 30. Output Enable/Disable

Table 25. P_{EXT} Calculations

Pin Type	Number of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 55 pF	× 20 MHz	× 25 V	= 0.206 W
$\overline{MSO}$	1	0	× 55 pF	× 20 MHz	× 25 V	= 0.00 W
$\overline{WR}$	1	–	× 55 pF	× 40 MHz	× 25 V	= 0.055 W
Data	32	50	× 25 pF	× 20 MHz	× 25 V	= 0.200 W
ADRCLK	1	–	× 15 pF	× 40 MHz	× 25 V	= 0.015 W

P_{EXT} (5 V) = 0.476 W.
P_{EXT} (3.3 V) = 0.207 W.

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins (see Figure 31). The delay and hold specifications given should be derated by a factor of 1.5 ns/50 pF for loads other than the nominal value of 50 pF. Figure 33 and Figure 34 show how output rise time varies with capacitance. Figure 35 graphically shows how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the Output Disable Time section.) The graphs in Figure 33, Figure 34, and Figure 35 might not be linear outside the ranges shown.

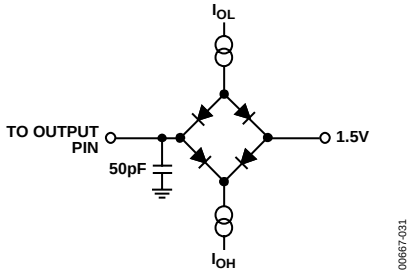


Figure 31. Equivalent Device Loading for AC Measurement (Includes All Fixtures)

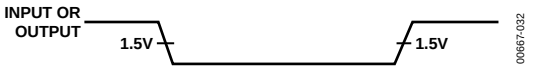


Figure 32. Voltage Reference Levels for AC Measurements (except Output Enable/Disable)

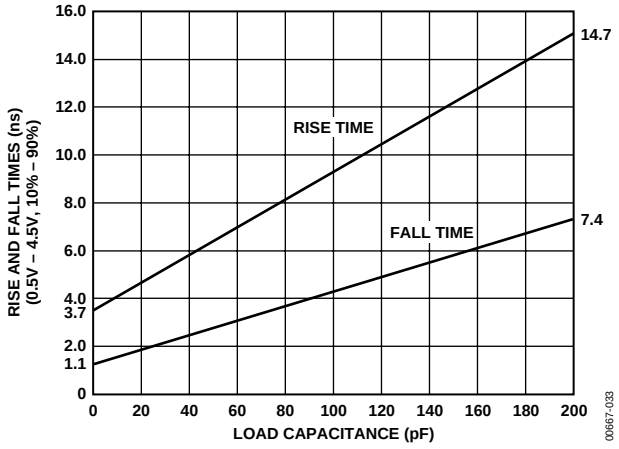


Figure 33. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 5 V)

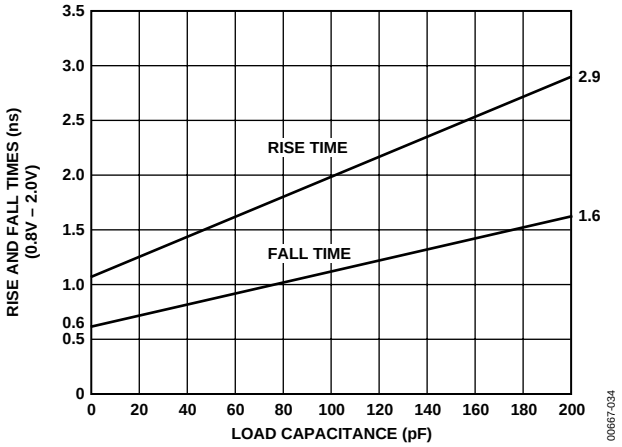


Figure 34. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 5 V)

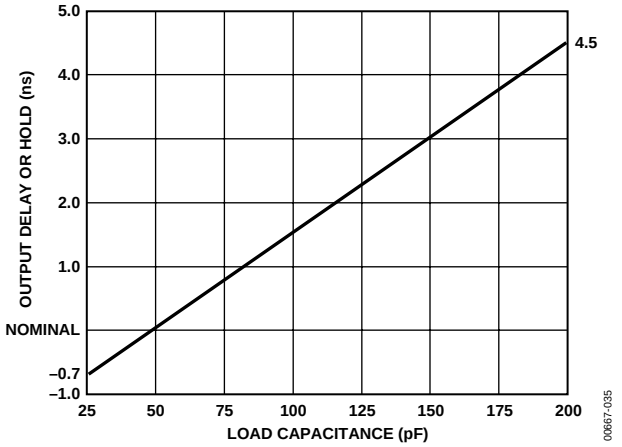


Figure 35. Typical Output Delay or Hold vs. Load Capacitance at Maximum Case Temperature (V_{DD} = 5 V)

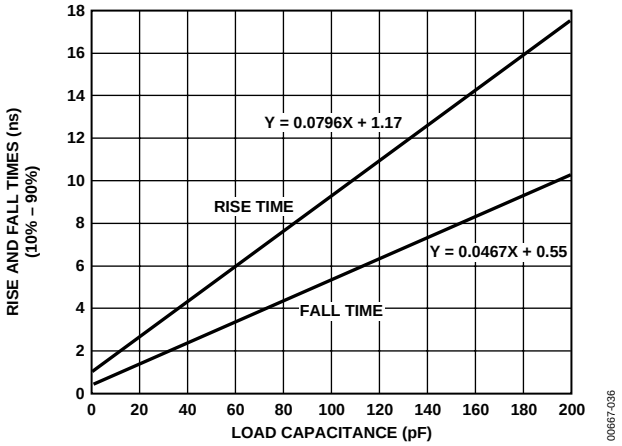


Figure 36. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 3.3 V)

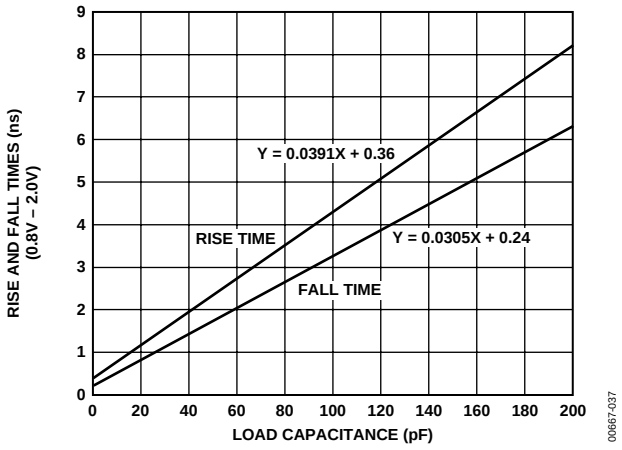


Figure 37. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 3.3 V)

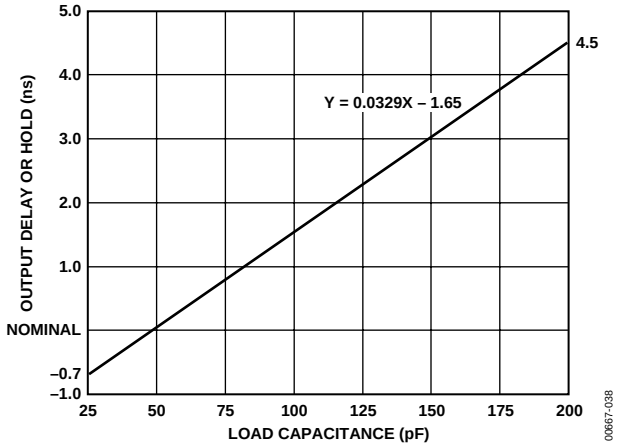


Figure 38. Typical Output Delay or Hold vs. Load Capacitance at Maximum Case Temperature (V_{DD} = 3.3 V)

ASSEMBLY RECOMMENDATIONS

Socket Information

Standard sockets and carriers are available for the AD14060/AD14060L, if needed. Socket part number IC53-3084-262 and carrier part number ICC-308-1 are available from Yamaichi Electronics.

Trim and Form

The AD14060/AD14060L is shipped as shown in Figure 43 with untrimmed and unformed leads and with the nonconductive tie bar in place. This avoids disturbance of lead spacing and coplanarity prior to assembly. Optimally, the leads should be trimmed, formed, and solder-dipped just prior to placement on the board.

Trim/form can be accomplished with a universal trim/form, a customer-designed trim/form, or with the Analog Devices developed tooling described as follows.

A trim/form tool specific to the AD14060/AD14060L has been developed and is available for use by all parties at

Tintronics Industries
2122-A Metro Circle
Huntsville, AL 35801
256-650-0220
Contact Person: Tom Rice

The package outline and dimensions resulting from this tool are shown in Figure 39. (Alternatively, the package can be trimmed/formed for cavity-down placement.)

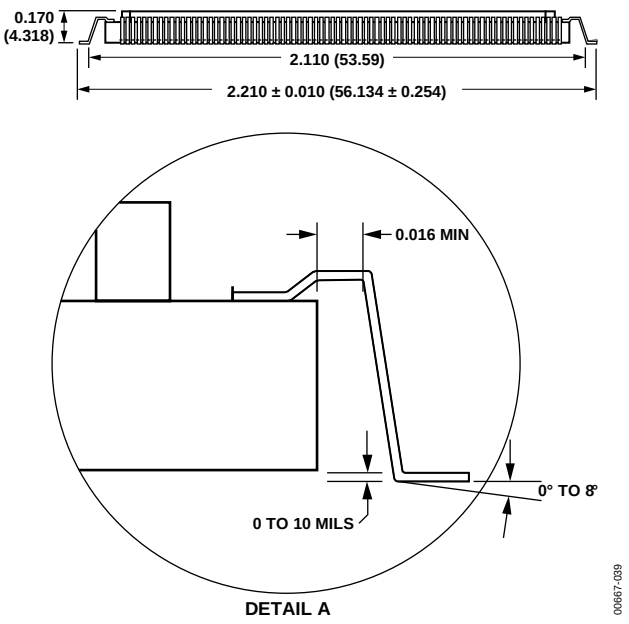


Figure 39. Package and Lead Profile Dimensions shown in inches and (millimeters)

PCB LAYOUT GUIDELINES

The drawing in Figure 40 assumes that the trim/form tooling described previously is used. These recommendations are provided for user convenience and are PCB layout guidelines only, based on standard practice. PCB pad footprint geometries and placement are illustrated.

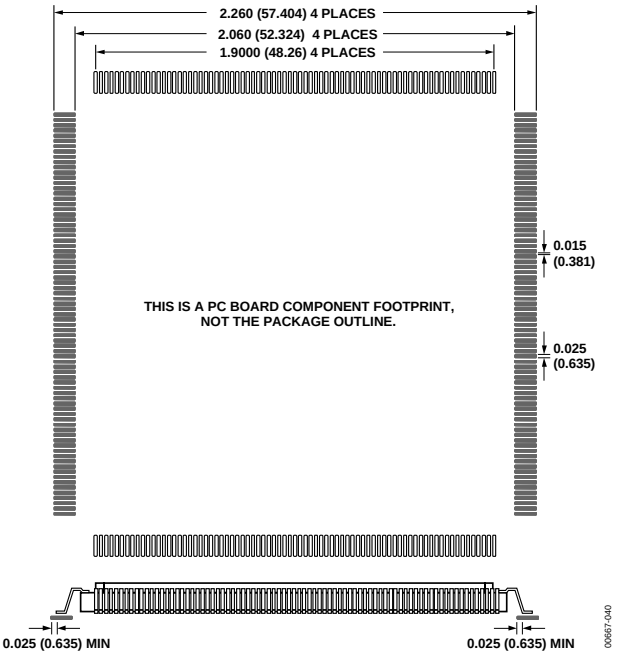


Figure 40. PC Board Component Footprint
Dimensions shown in inches and (millimeters)

Thermal Characteristics

The AD14060/AD14060L is packaged in a 308-lead ceramic quad flatpack (CQFP). The package is optimized for thermal conduction through the core (base of the package) down to the mounting surface. The AD14060/AD14060L is specified for a case temperature (T_{CASE}). Design of the mounting surface and attachment material should be such that T_{CASE} is not exceeded.

θ_{JC} = 0.36°C/W

Thermal Cross-Section

The following data, together with the detailed mechanical drawings in Figure 43, allows the designer to construct simple thermal models for further analysis within targeted systems. The top layer of the package, where the die are mounted, is a metal V_{DD} layer. The approximate metal area coverage from the metal planes and routing layers is estimated in Table 27. The layers are shown in Figure 41.

Table 26. Thermal Conductivity

Material	Thermal Conductivity (W/cm°C)
Ceramic	0.18
Kovar™	0.14
Tungsten	1.78
Thermoplastic	0.03
Silicon	1.45

Table 27. Metal Coverage per Layer

Layer	% Metal (1 Mil Thick)
V_{DD}	88
SIG2	16
SIG3	14
GND	91
SIG4	15
SIG5	13
BASE	95

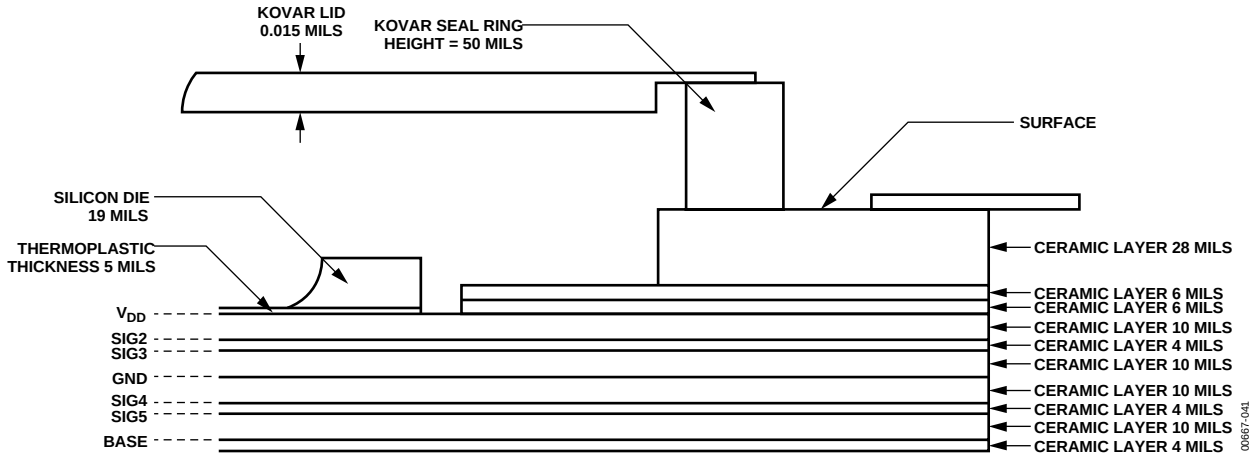


Figure 41. Co-Fired Packaged Profile

MECHANICAL CHARACTERISTICS

Lid Deflection Analysis

Table 28. External Pressure Reduction

Δ Pressure	Deflection
12 psi	10.0 mil
15 psi	11.9 mil

Mechanical Model

The following data, together with the detailed mechanical drawings in Figure 43, allows the designer to construct simple mechanical models for further analysis within targeted systems.

Table 29. Mechanical Properties

Material	Modulas of Elasticity
Ceramic	26×10^3 kg/mm^2
Kovar	14.1×10^3 kg/mm^2
Tungsten	35×10^3 kg/mm^2
Thermoplastic	279 kg/mm^2
Silicon	11×10^3 kg/mm^2

ADDITIONAL INFORMATION

This data sheet provides a general overview of the AD14060/AD14060L architecture and functionality. For detailed information on the ADSP-2106x SHARC and the ADSP-21000 Family core architecture and instruction set, refer to the *ADSP-2106x SHARC User's Manual*.

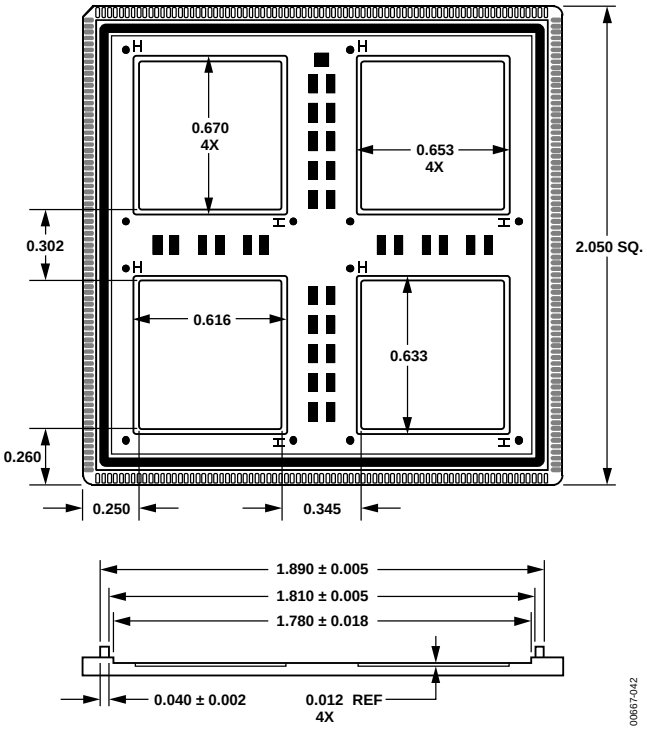


Figure 42. Internal Package Dimensions
Dimensions shown in inches

OUTLINE DIMENSIONS

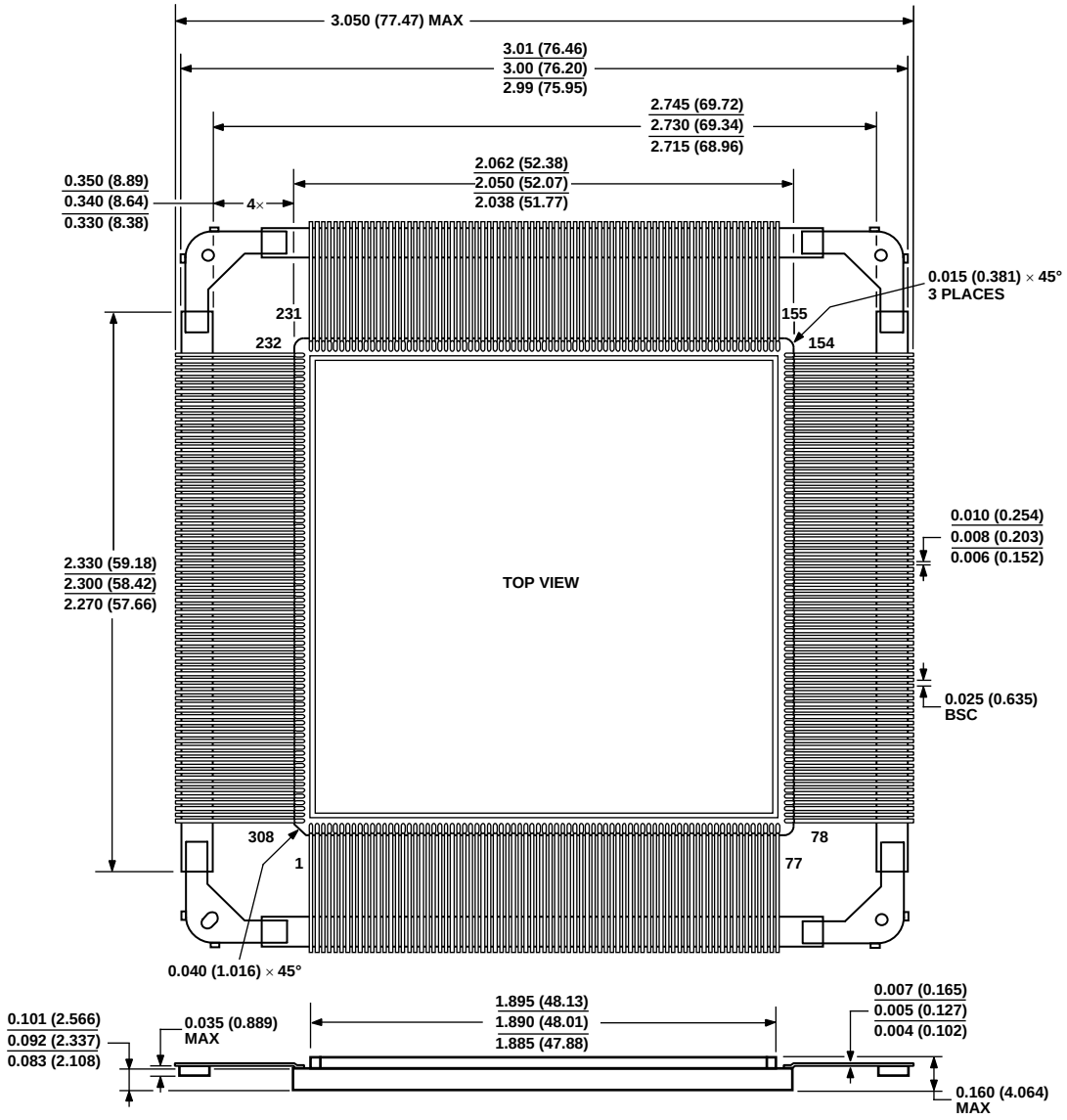


Figure 43. 308-Lead Ceramic Quad Flatpack (CQFP)
(QS-308)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	SMD	Instruction Rate	Operating Voltage	Package Description	Package Option
AD14060BF-4	–40°C to +100°C	N/A	40 MHz	5 V	308-Lead Ceramic Quad Flatpack (CQFP)	QS-308
AD14060LBF-4	–40°C to +100°C	N/A	40 MHz	3.3 V	308-Lead Ceramic Quad Flatpack (CQFP)	QS-308