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ISL59441

900MHz Multiplexing Amplifier

FN6163
Rev 2.00
September 21, 2005

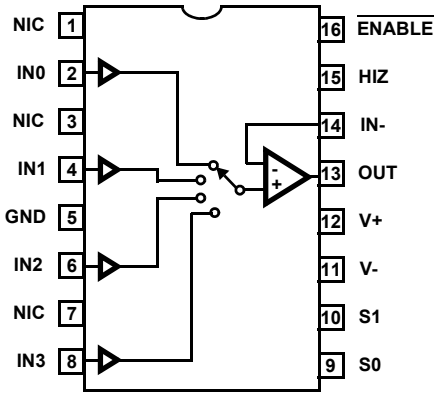
The ISL59441 is 900MHz bandwidth 4:1 multiplexing amplifier designed primarily for video switching. This Mux amp has a user-settable gain and also features a high speed three-state function to enable the output of multiple devices to be wired together. All logic inputs have pull-downs to ground and may be left floating. The $\overline{\text{ENABLE}}$ pin, when pulled high, sets the ISL59441 to the low current power-down mode for power sensitive applications - consuming just 5mW.

TABLE 1. CHANNEL SELECT LOGIC TABLE

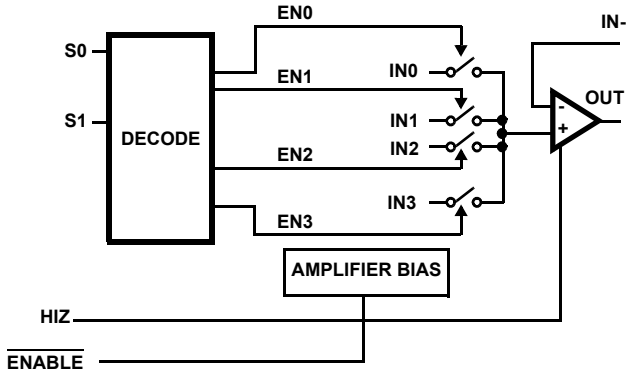
S1	S0	$\overline{\text{ENABLE}}$	HIZ	OUTPUT
0	0	0	0	IN0
0	1	0	0	IN1
1	0	0	0	IN2
1	1	0	0	IN3
X	X	1	X	Power Down
X	X	0	1	High Z

Pinout

ISL59441 (16 LD QSOP)
TOP VIEW



Functional Diagram



$\overline{\text{ENABLE}}$ pin must be low in order to activate the HIZ state

Features

- 900MHz (-3dB) Bandwidth (A_V = 1, V_{OUT} = 100mV_{P-P})
- 230MHz (-3dB) Bandwidth (A_V = 2, V_{OUT} = 2V_{P-P})
- Slew Rate (A_V = 1, R_L = 500Ω, V_{OUT} = 4V) 1349V/µs
- Slew Rate (A_V = 2, R_L = 500Ω, V_{OUT} = 5V) 1927V/µs
- Adjustable Gain
- High Speed Three-State Output (HIZ)
- Low Current Power-Down 5mW
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- HDTV/DTV Analog Inputs
- Video Projectors
- Computer Monitors
- Set-top Boxes
- Security Video
- Broadcast Video Equipment

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
ISL59441IA	59441IA	-	16 Ld QSOP	MDP0040
ISL59441IA-T7	59441IA	7”	16 Ld QSOP	MDP0040
ISL59441IA-T13	59441IA	13”	16 Ld QSOP	MDP0040
ISL59441IAZ (Note)	59441IAZ	-	16 Ld QSOP (Pb-free)	MDP0040
ISL59441IAZ-T7 (Note)	59441IAZ	7”	16 Ld QSOP (Pb-free)	MDP0040
ISL59441IAZ-T13 (Note)	59441IAZ	13”	16 Ld QSOP (Pb-free)	MDP0040

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V+ to V-). 11V
Input Voltage . . . . . V- -0.5V, V+ +0.5V
Supply Turn-on Slew Rate 1V/µs
IN- Input Current (Note 1) 5mA
Digital & Analog Input Current (Note 1) 50mA
Output Current (Continuous) 50mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7). . . . 2.5kV
Machine Model 300V

Storage Temperature Range . . . . . .-65°C to +150°C
Ambient Operating Temperature . . . . . .-40°C to +85°C
Operating Junction Temperature . . . . . .-40°C to +125°C
Power Dissipation . . . . . See Curves
θ_{JA} . . . . . See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V+ = +5V, V- = -5V, GND = 0V, T_A = 25°C, R_L = 500Ω to GND unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
±I_S Enabled	Supply Current	No load, V_{IN} = 0V, $\overline{\text{ENABLE}}$ Low	15	17	19.5	mA
I_S Disabled	Disabled Supply Current I+	No load, V_{IN} = 0V, $\overline{\text{ENABLE}}$ High	0.6	1	1.5	mA
	Disabled Supply Current I-	No load, V_{IN} = 0V, $\overline{\text{ENABLE}}$ High		3	10	µA
V_{OUT}	Positive Output Swing	V_{IN} = 2V, R_L = 500Ω, A_V = 2	2.8	3.9		V
	Negative Output Swing	V_{IN} = -2V, R_L = 500Ω, A_V = 2		-4	-3.5	V
I_{OUT}	Output Current	R_L = 10Ω to GND	±80	±130	±180	mA
V_{OS}	Output Offset Voltage		0	9	18	mV
Ib+	Input Bias Current	V_{IN} = 0V	-4	-2.5	-1.5	µA
Ib-	Feedback Input Bias Current	V_{IN} = 0V	-28	16	28	µA
R_{out}	Output Resistance	HIZ = logic high, (DC), A_V = 1		1.4		MΩ
		HIZ = logic low, (DC), A_V = 1		0.2		Ω
R_{IN}	Input Resistance	V_{IN} = ±3.5V		10		MΩ
A_{CL} or A_V	Voltage Gain	V_{IN} = ±1.5V, R_L = 500Ω, R_F = R_G = 600Ω	1.99	2	2.01	V/V
I_{TRI}	Output Current in Three-State	V_{OUT} = 0V	-35		35	µA
LOGIC						
V_H	Input High Voltage (Logic Inputs)		2			V
V_L	Input Low Voltage (Logic Inputs)				0.8	V
I_{IH}	Input High Current (Logic Inputs)		55	90	135	µA
I_{IL}	Input Low Current (Logic Inputs)			2	10	µA
AC GENERAL						
- 3dB BW	-3dB Bandwidth	A_V = 1, R_F = 301Ω, V_{OUT} = 200mV_{P-P}, C_L = 1.6pF, C_G = 0.6pF		900		MHz
		A_V = 2, R_F = R_G = 205Ω, V_{OUT} = 2V_{P-P}, C_L = 1.6pF, C_G = 0.6pF		230		MHz

Electrical Specifications $V+ = +5V$, $V- = -5V$, GND = 0V, $T_A = 25°C$, $R_L = 500\Omega$ to GND unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
0.1dB BW	0.1dB Bandwidth	$A_V = 1$, $R_F = 301\Omega$, $V_{OUT} = 200mV_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$		90		MHz
		$A_V = 2$, $R_F = R_G = 205\Omega$, $V_{OUT} = 2V_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$		32		MHz
dG	Differential Gain Error	NTC-7, $R_L = 150$, $C_L = 1.6pF$, $A_V = 1$		0.01		%
		NTC-7, $R_L = 150$, $C_L = 1.6pF$, $A_V = 2$		0.01		%
dP	Differential Phase Error	NTC-7, $R_L = 150$, $C_L = 1.6pF$, $A_V = 1$		0.02		°
		NTC-7, $R_L = 150$, $C_L = 1.6pF$, $A_V = 2$		0.02		°
+SR	Slew Rate Low to High	25% to 75%, $A_V = 1$, $V_{OUT} = 5V$, $R_L = 500\Omega$, $C_L = 1.6pF$		1349		V/µs
		25% to 75%, $A_V = 2$, $V_{OUT} = 5V$, $R_L = 500\Omega$, $C_L = 1.6pF$		1927		V/µs
-SR	Slew Rate High to Low	25% to 75%, $A_V = 1$, $V_{OUT} = 5V$, $R_L = 500\Omega$, $C_L = 1.6pF$		1135		V/µs
		25% to 75%, $A_V = 2$, $V_{OUT} = 5V$, $R_L = 500\Omega$, $C_L = 1.6pF$		1711		V/µs
PSRR	Power Supply Rejection Ratio	DC, PSRR V+ and V- combined	-50	-57		dB
ISO	Channel Isolation	f = 10MHz, Ch-Ch X-Talk and Off Isolation, $C_L = 1.6pF$		75		dB
SWITCHING CHARACTERISTICS						
V_{GLITCH}	Channel-to-Channel Switching Glitch	$V_{IN} = 0V$, $C_L = 1.6pF$, $A_V = 2$		1		mV_{P-P}
	$\overline{\text{ENABLE}}$ Switching Glitch	$V_{IN} = 0V$, $C_L = 1.6pF$, $A_V = 2$		935		mV_{P-P}
	HIZ Switching Glitch	$V_{IN} = 0V$, $C_L = 1.6pF$, $A_V = 2$		255		mV_{P-P}
t_{SW-L-H}	Channel Switching Time Low to High	1.2V logic threshold to 10% movement of analog output		24		ns
t_{SW-H-L}	Channel Switching Time High to Low	1.2V logic threshold to 10% movement of analog output		19		ns
TRANSIENT RESPONSE						
t_R, t_F	Rise & Fall Time, 10% to 90%	$A_V = 1$, $R_F = 301\Omega$, $V_{OUT} = 100mV_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$		0.44		ns
		$A_V = 2$, $R_F = R_G = 205\Omega$, $V_{OUT} = 2V_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$		1.23		ns
t_S	0.1% Settling Time	$A_V = 2$, $R_F = R_G = 205\Omega$, $V_{OUT} = 2V_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$		4.5		ns
O_S	Overshoot	$A_V = 1$, $R_F = 301\Omega$, $V_{OUT} = 100mV_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$		9.52		%
		$A_V = 2$, $R_F = R_G = 205\Omega$, $V_{OUT} = 2V_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$		8.81		%
t_{PLH}	Propagation Delay - Low to High, 10% to 10%	$A_V = 1$, $R_F = 301\Omega$, $V_{OUT} = 100mV_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$		0.48		ns
		$A_V = 2$, $R_F = R_G = 205\Omega$, $V_{OUT} = 2V_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$		0.69		ns
t_{PHL}	Propagation Delay- High to Low, 10% to 10%	$A_V = 1$, $R_F = 301\Omega$, $V_{OUT} = 100mV_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$		0.54		ns
		$A_V = 2$, $R_F = R_G = 205\Omega$, $V_{OUT} = 2V_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$		0.74		ns

Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = 25°C$, unless otherwise specified.

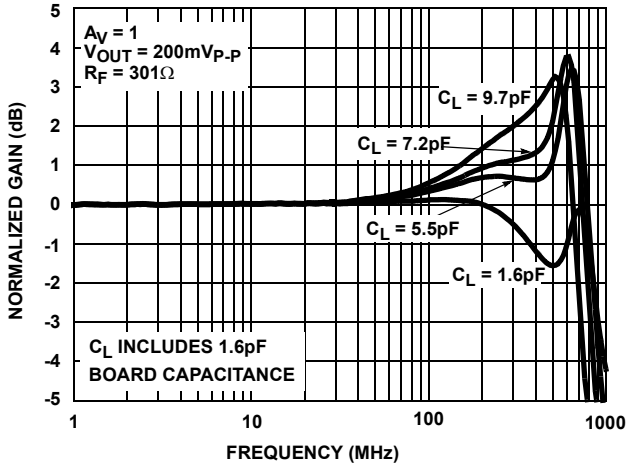


FIGURE 1. SMALL SIGNAL GAIN vs FREQUENCY vs C_L

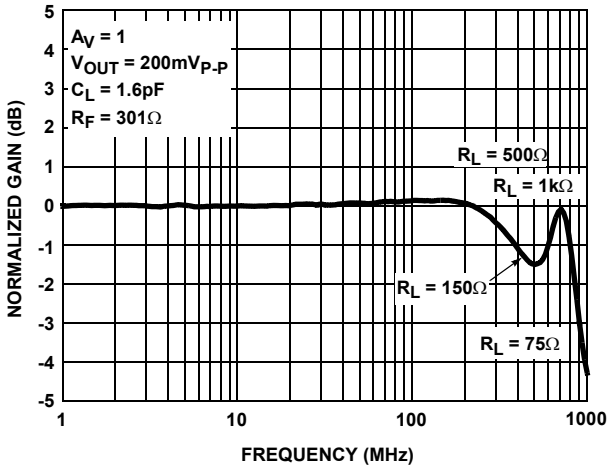


FIGURE 2. SMALL SIGNAL GAIN vs FREQUENCY vs R_L

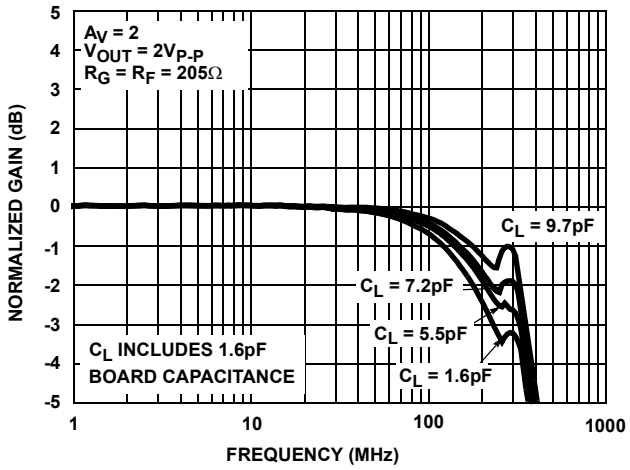


FIGURE 3. LARGE SIGNAL GAIN vs FREQUENCY vs C_L

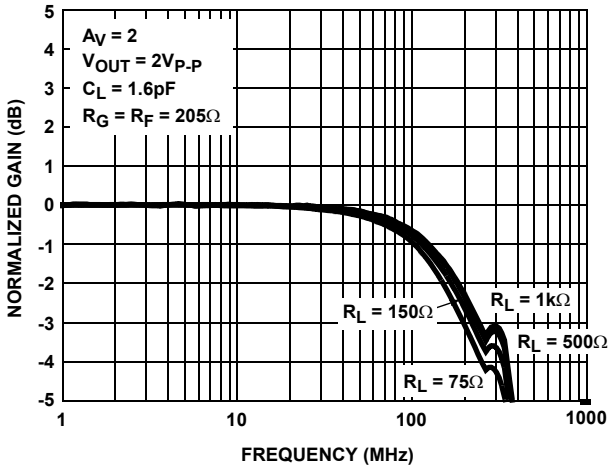


FIGURE 4. LARGE SIGNAL GAIN vs FREQUENCY vs R_L

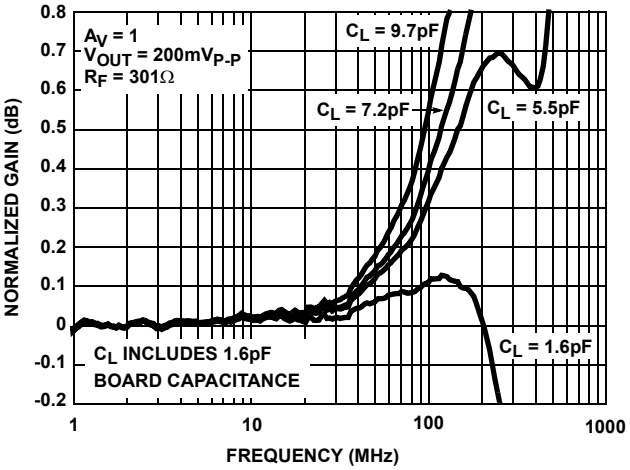


FIGURE 5. SMALL SIGNAL 0.1dB GAIN vs FREQUENCY vs C_L

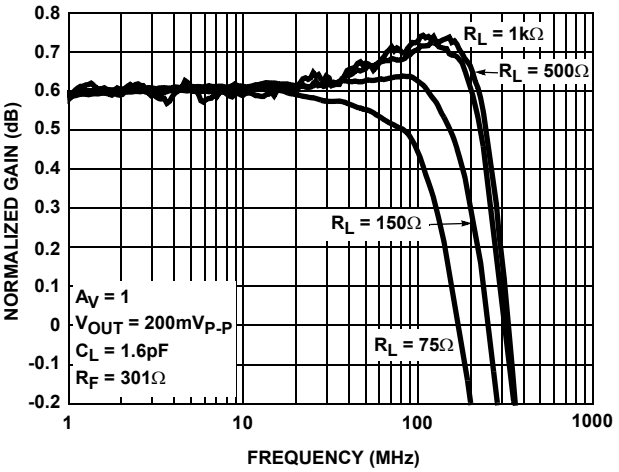


FIGURE 6. SMALL SIGNAL 0.1dB GAIN vs FREQUENCY vs R_L

Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = 25°C$, unless otherwise specified. **(Continued)**

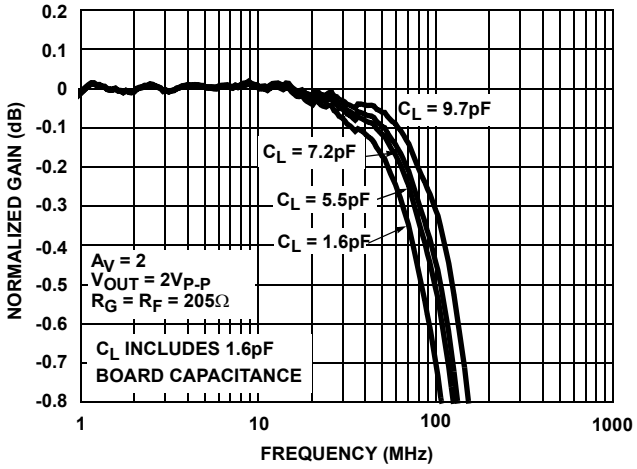


FIGURE 7. LARGE SIGNAL 0.1dB GAIN vs FREQUENCY vs C_L

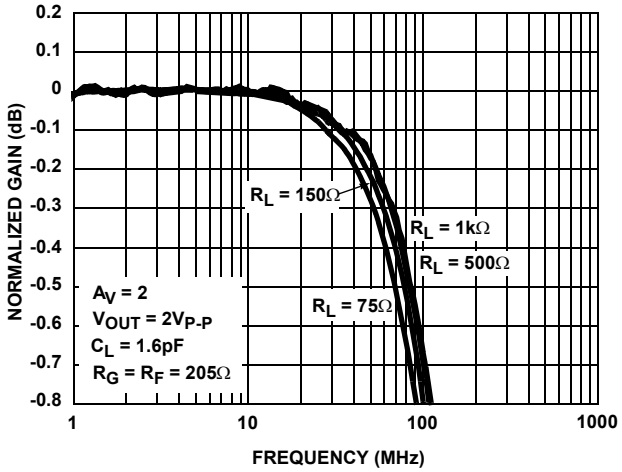


FIGURE 8. LARGE SIGNAL 0.1dB GAIN vs FREQUENCY vs R_L

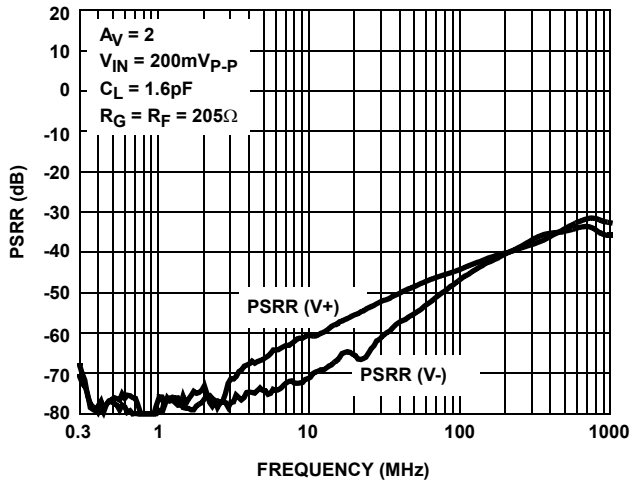


FIGURE 9. PSRR CHANNELS

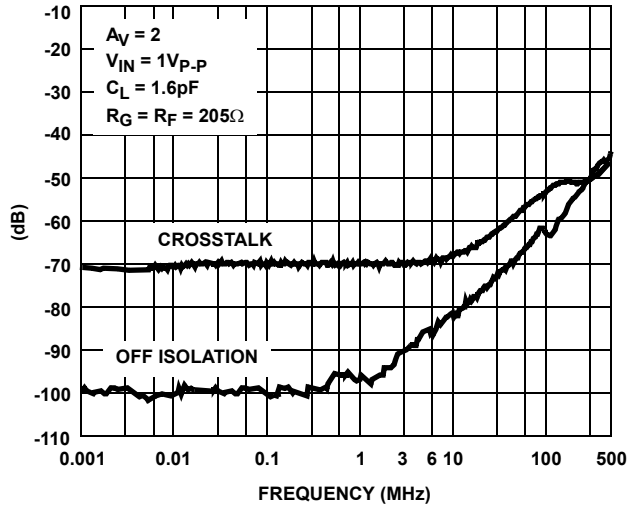


FIGURE 10. CROSSTALK AND OFF ISOLATION

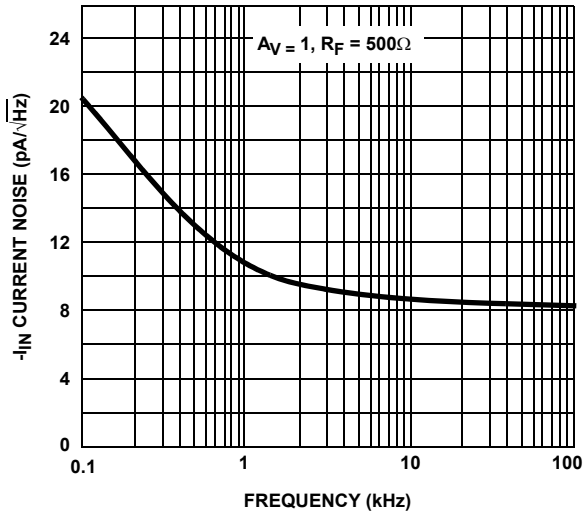


FIGURE 11. INPUT NOISE vs FREQUENCY

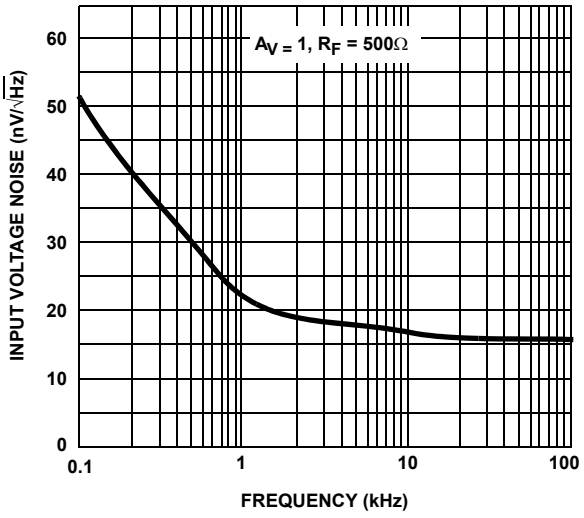


FIGURE 12. INPUT NOISE vs FREQUENCY

Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = 25°C$, unless otherwise specified. **(Continued)**

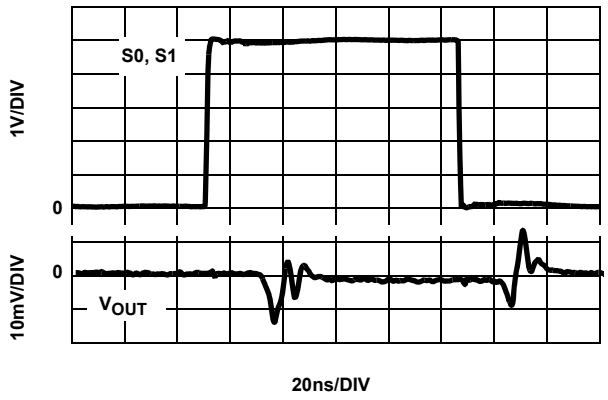


FIGURE 13. CHANNEL TO CHANNEL SWITCHING GLITCH V_{IN} = 0V, A_V = 2

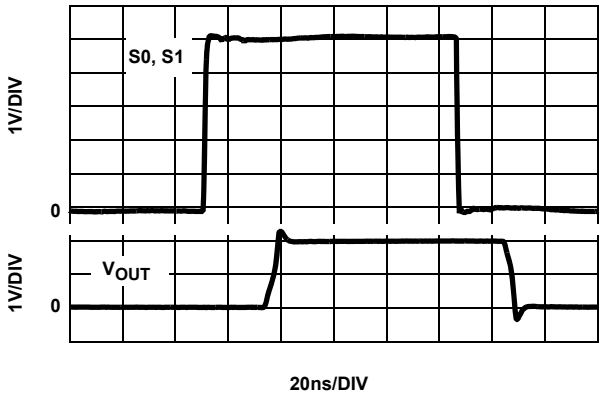


FIGURE 14. CHANNEL TO CHANNEL TRANSIENT RESPONSE V_{IN} = 1V, A_V = 2

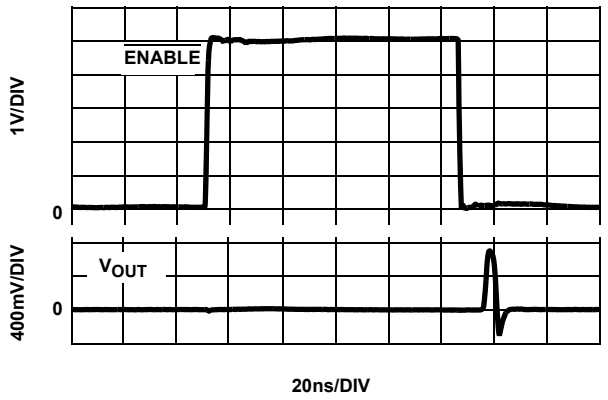


FIGURE 15. $\overline{\text{ENABLE}}$ SWITCHING GLITCH V_{IN} = 0V, A_V = 2

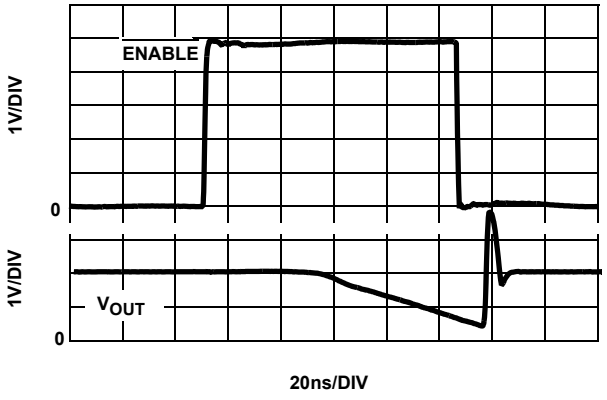


FIGURE 16. $\overline{\text{ENABLE}}$ TRANSIENT RESPONSE V_{IN} = 1V, A_V = 2

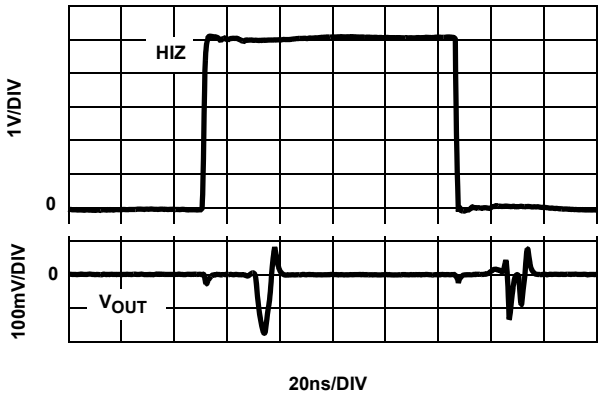


FIGURE 17. HIZ SWITCHING GLITCH V_{IN} = 0V, A_V = 2

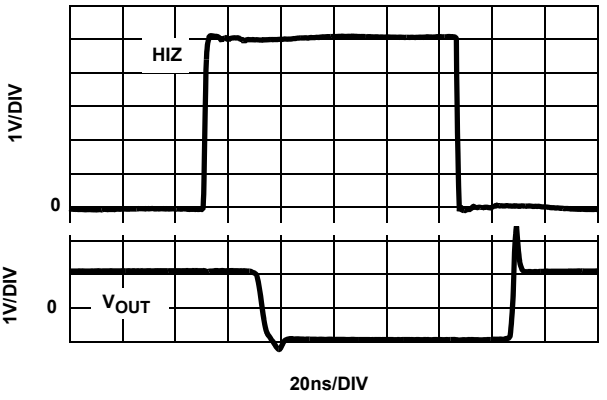


FIGURE 18. HIZ TRANSIENT RESPONSE V_{IN} = 1V, A_V = 2

Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = 25°C$, unless otherwise specified. **(Continued)**

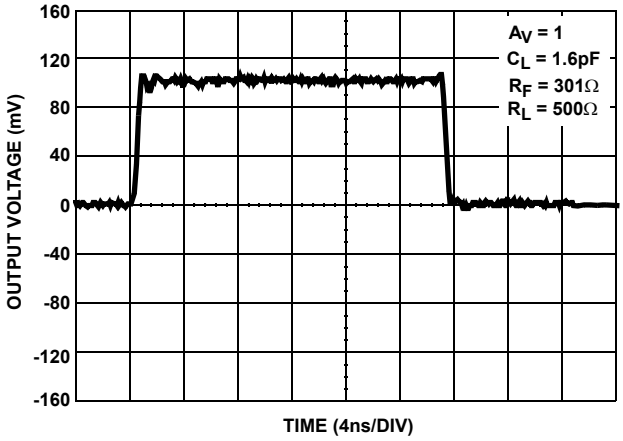


FIGURE 19. SMALL SIGNAL TRANSIENT RESPONSE

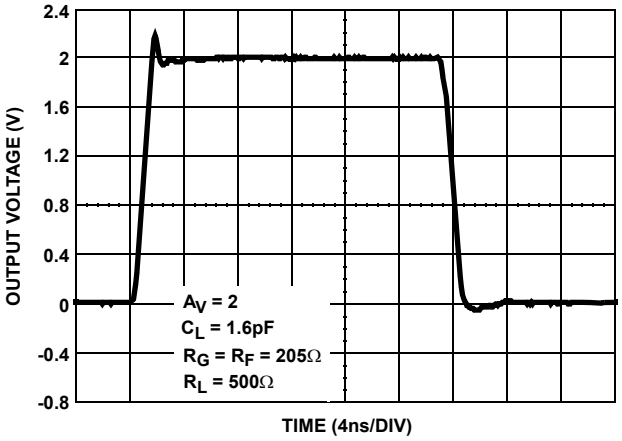


FIGURE 20. LARGE SIGNAL TRANSIENT RESPONSE

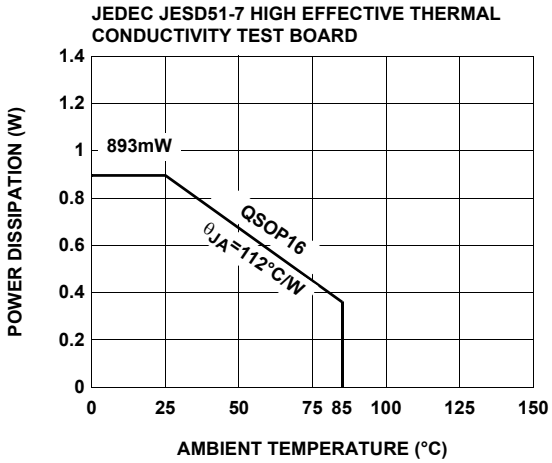


FIGURE 21. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

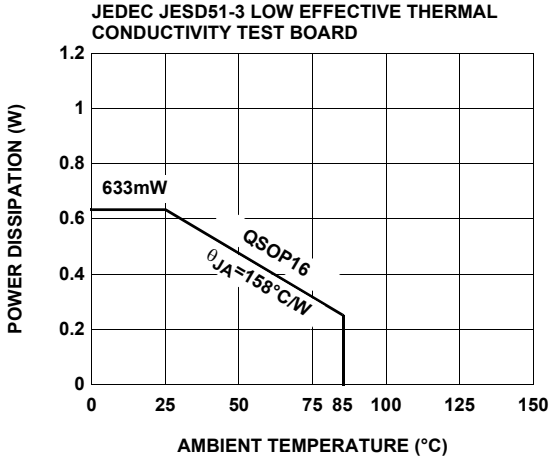


FIGURE 22. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

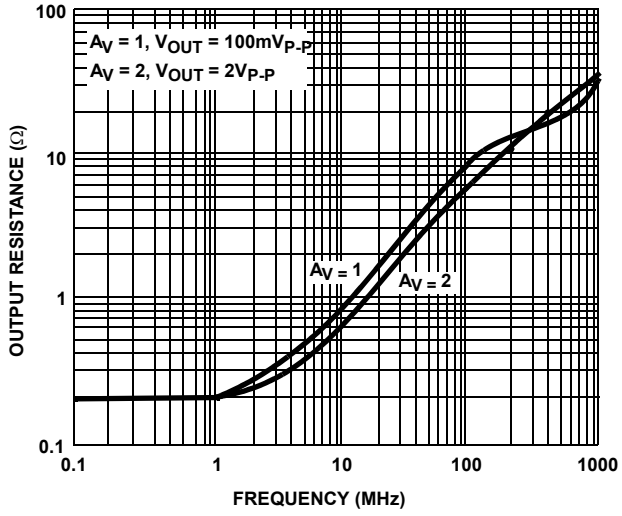
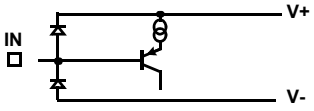


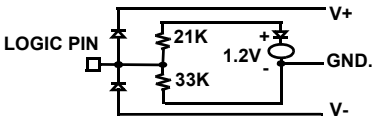
FIGURE 23. R_{OUT} vs FREQUENCY

Pin Descriptions

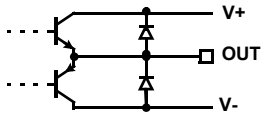
PIN NUMBER	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1, 3, 7	NIC		**N**ot **I**nternally **C**onnected; it is recommended this pin be tied to ground to minimize crosstalk
2	IN0	Circuit 1	Input for channel 0
4	IN1	Circuit 1	Input for channel 1
5	GND	Circuit 4	Ground pin
6	IN2	Circuit 1	Input for channel 2
8	IN3	Circuit 1	Input for channel 3
9	S0	Circuit 2	Channel selection pin LSB (binary logic code)
10	S1	Circuit 2	Channel selection pin MSB (binary logic code)
11	V-	Circuit 4	Negative power supply
12	V+	Circuit 4	Positive power supply
13	OUT	Circuit 3	Output
14	IN-	Circuit 1	Inverting input of output amplifier
15	HIZ	Circuit 2	Output disable (active high); there are internal pull-down resistors, so the device will be active with no connection; “HI” puts the output in high impedance state
16	$\overline{\text{ENABLE}}$	Circuit 2	Device enable (active low); there are internal pull-down resistors, so the device will be active with no connection; "HI" puts device into power-down mode



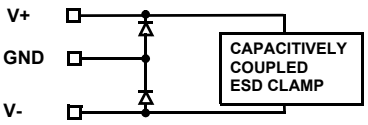
CIRCUIT 1.



CIRCUIT 2.



CIRCUIT 3.



CIRCUIT 4.

AC Test Circuits

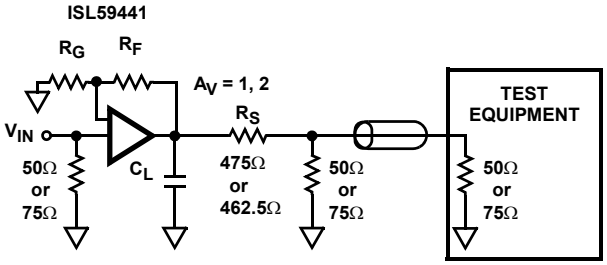


FIGURE 24A. TEST CIRCUIT FOR MEASURING WITH A 50Ω OR 75Ω INPUT TERMINATED EQUIPMENT

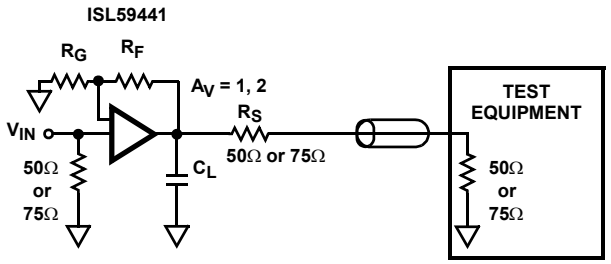


FIGURE 24B. BACKLOADED TEST CIRCUIT FOR VIDEO CABLE APPLICATION. BANDWIDTH AND LINEARITY FOR R_L LESS THAN 500Ω WILL BE DEGRADED.

NOTE: Figure 24A illustrates the optimum output load when connecting to input terminated equipment. Figure 24B illustrates backloaded test circuit for video cable applications.

Application Circuits

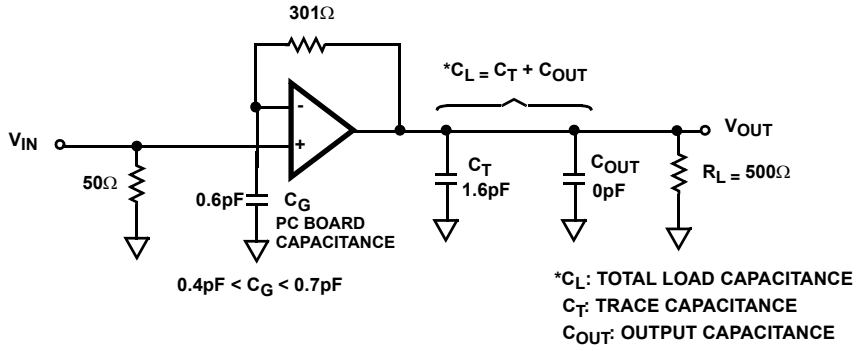


FIGURE 25A. GAIN OF 1 APPLICATION CIRCUIT

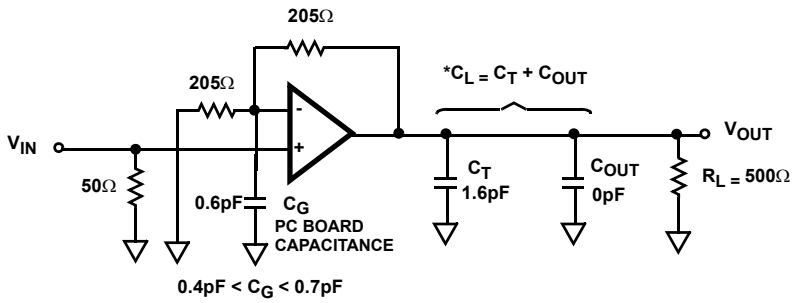


FIGURE 25B. GAIN OF 2 APPLICATION CIRCUIT

Application Information

General

The ISL59441 is a 4:1 mux that is ideal as a matrix element in high performance switchers and routers. The ISL59441 is optimized to drive 5pF in parallel with a 500Ω load. The capacitance can be split between the PCB capacitance and an external load capacitance. Its low input capacitance and high input resistance provide excellent 50Ω or 75Ω terminations.

Parasitic Effects on Frequency Performance

Capacitance at the Inverting Input

The AC performance of current-feedback amplifiers in the non-inverting gain configuration is strongly affected by stray capacitance at the inverting input. Stray capacitance from the inverting input pin to the output (C_F), and to ground (C_G), increase gain peaking and bandwidth. Large values of either capacitance can cause oscillation. The ISL59441 has been optimized for a 0.4pF to 0.7pF capacitance (C_G). Capacitance (C_F) to the output should be minimized. To achieve optimum performance the feedback network resistor(s) must be placed as close to the device as possible. Trace lengths greater than 1/4 inch combined with resistor pad capacitance can result in inverting input to ground capacitance approaching 1pF. Inverting input and output traces should not run parallel to each other. Small size surface mount resistors (604 or smaller) are recommended.

Capacitance at the Output

The output amplifier is optimized for capacitance to ground (C_L) directly on the output pin. Increased capacitance causes higher peaking with an increase in bandwidth. The optimum range for most applications is ~1.0pF to ~6pF. The optimum value can be achieved through a combination of PC board trace capacitance (C_T) and an external capacitor (C_{OUT}). A good method to maintain control over the output pin capacitance is to minimize the trace length (C_T) to the next component, and include a discrete surface mount capacitor (C_{OUT}) directly at the output pin.

Feedback Resistor Values

The AC performance of the output amplifier is optimized with the feedback resistor network (R_F, R_G) values recommended in the application circuits. The amplifier bandwidth and gain peaking are directly affected by the value(s) of the feedback resistor(s) in unity gain and gain >1 configurations. Transient response performance can be tailored simply by changing these resistor values. Generally, lower values of R_F and R_G increase bandwidth and gain peaking. This has the effect of decreasing rise/fall times and increasing overshoot.

Ground Connections

For the best isolation and crosstalk rejection, the GND pin and NIC pins must connect to the GND plane.

Control Signals

S0, S1, $\overline{\text{ENABLE}}$, HIZ - These pins are TTL/CMOS compatible control inputs. The S0 pin selects which one of the inputs connect to the output. The $\overline{\text{ENABLE}}$, HIZ pins are used to disable the part to save power and three-state the output amplifiers, respectively. For control signal rise and fall times less than 10ns the use of termination resistors close to the part will minimize transients coupled to the output.

Power-Up Considerations

The ESD protection circuits use internal diodes from all pins the V+ and V- supplies. In addition, a dV/dT- triggered clamp is connected between the V+ and V- pins, as shown in the Equivalent Circuits 1 through 4 section of the Pin Description table. The dV/dT triggered clamp imposes a maximum supply turn-on slew rate of 1V/µs. Damaging currents can flow for power supply rates-of-rise in excess of 1V/µs, such as during hot plugging. Under these conditions, additional methods should be employed to ensure the rate of rise is not exceeded.

Consideration must be given to the order in which power is applied to the V+ and V- pins, as well as analog and logic input pins. Schottky diodes (Motorola MBR0550T or equivalent) connected from V+ to ground and V- to ground (Figure 26) will shunt damaging currents away from the internal V+ and V- ESD diodes in the event that the V+ supply is applied to the device before the V- supply.

If positive voltages are applied to the logic or analog video input pins before V+ is applied, current will flow through the internal ESD diodes to the V+ pin. The presence of large decoupling capacitors and the loading effect of other circuits connected to V+, can result in damaging currents through the ESD diodes and other active circuits within the device. Therefore, adequate current limiting on the digital and analog inputs is needed to prevent damage during the time the voltages on these inputs are more positive than V+.

HIZ State

An internal pull-down resistor connected to the HIZ pin ensures the device will be active with no connection to the HIZ pin. The HIZ state is established within approximately 30ns (Figure 18) by placing a logic high (>2V) on the HIZ pin. If the HIZ state is selected, the output is a high impedance 1.4MΩ. Use this state to control the logic when more than one mux shares a common output.

In the HIZ state the output is three-stated, and maintains its high Z even in the presence of high slew rates. The supply current during this state is basically the same as the active state.

$\overline{\text{ENABLE}}$ & Power Down States

The enable pin is active low. An internal pull-down resistor ensures the device will be active with no connection to the $\overline{\text{ENABLE}}$ pin. The Power Down state is established when a logic high (>2V) is placed on the $\overline{\text{ENABLE}}$ pin. In the Power Down state, the output has no leakage but has a large capacitance (on the order of 15pF), and is capable of being back-driven. Under this condition, large incoming slew rates can cause fault currents of tens of mA. **Do not use this state as a high Z state for applications driving more than one mux on a common output.**

Limiting the Output Current

No output short circuit current limit exists on this part. All applications need to limit the output current to less than 50mA. Adequate thermal heat sinking of the parts is also required.

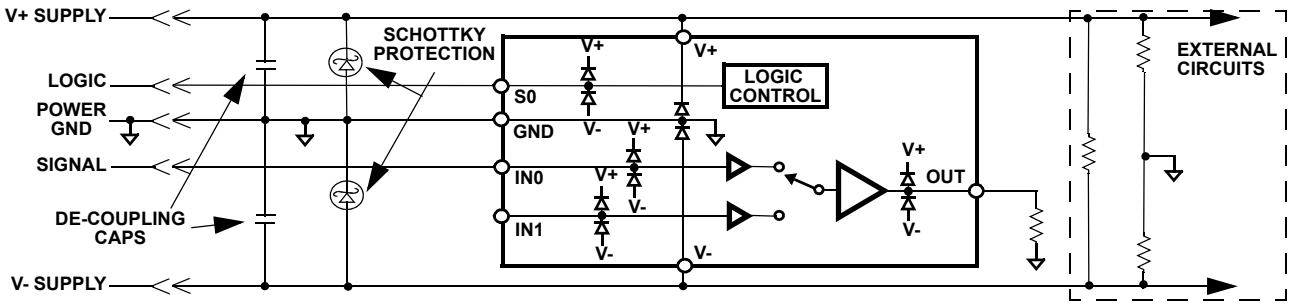


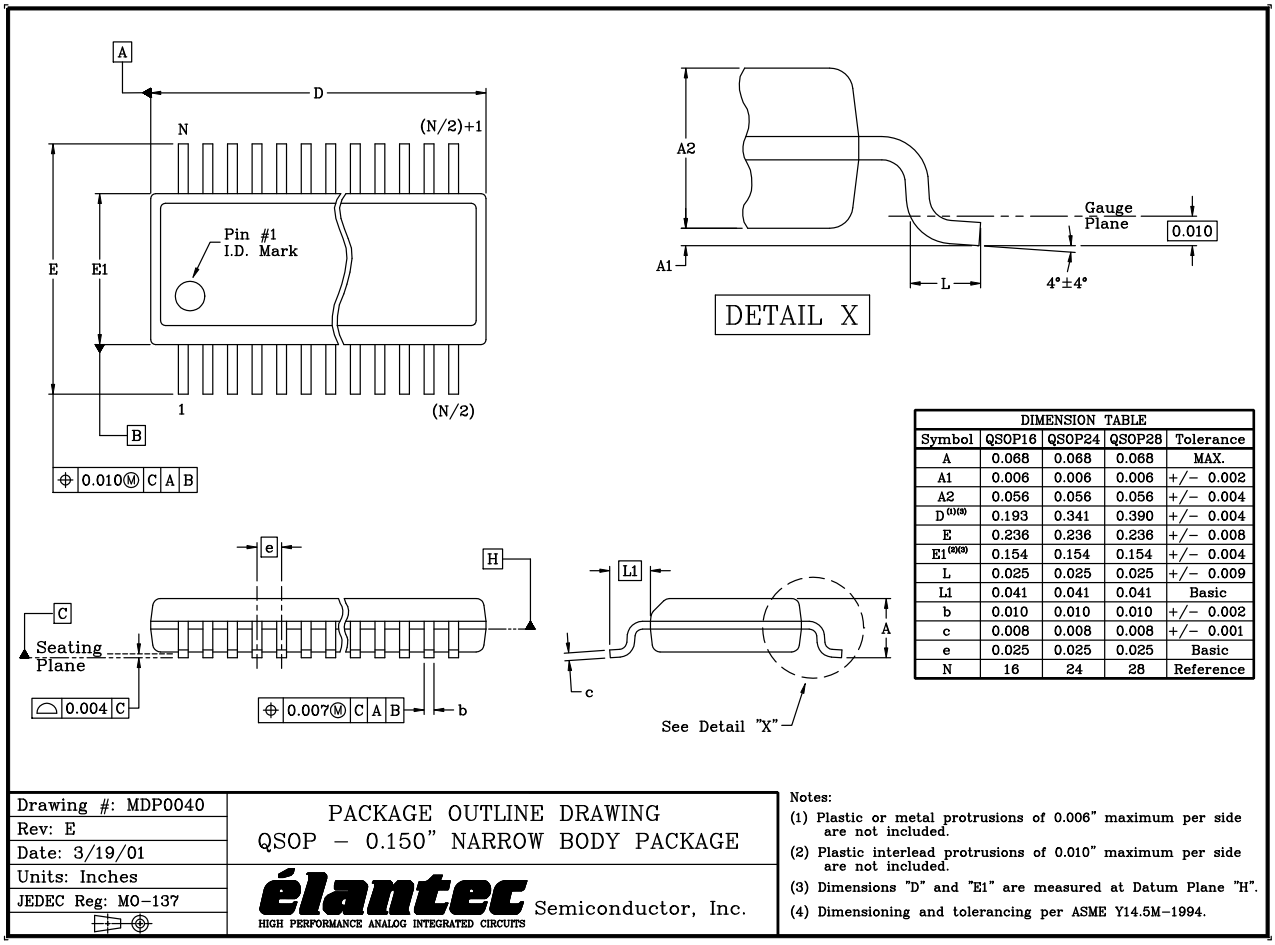
FIGURE 26. SCHOTTKY PROTECTION CIRCUIT

PC Board Layout

The frequency response of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- The use of low inductance components such as chip resistors and chip capacitors is strongly recommended.
- Minimize signal trace lengths. Trace inductance and capacitance can easily limit circuit performance. Avoid sharp corners, use rounded corners when possible. Vias in the signal lines add inductance at high frequency and should be avoided. PCB traces greater than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. High frequency performance may be degraded for traces greater than one inch, unless strip lines are used.
- Match channel-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- Maximize use of AC de-coupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e. no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.
- Use proper value and location of termination resistors. Termination resistors should be as close to the device as possible.
- When testing use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- Minimum of 2 power supply de-coupling capacitors are recommended (1000pF, 0.01µF) as close to the device as possible. Avoid vias between the cap and the device because vias add unwanted inductance. Larger caps can be farther away. When vias are required in a layout, they should be routed as far away from the device as possible.
- The NIC pins are placed on both sides of the input pins. These pins are not internally connected to the die. It is recommended these pins be tied to ground to minimize crosstalk.

QSOP Package Outline Drawing



DIMENSION TABLE				
Symbol	QSOP16	QSOP24	QSOP28	Tolerance
A	0.068	0.068	0.068	MAX.
A1	0.006	0.006	0.006	+/- 0.002
A2	0.056	0.056	0.056	+/- 0.004
D (1)(3)	0.193	0.341	0.390	+/- 0.004
E	0.236	0.236	0.236	+/- 0.008
E1 (2)(3)	0.154	0.154	0.154	+/- 0.004
L	0.025	0.025	0.025	+/- 0.009
L1	0.041	0.041	0.041	Basic
b	0.010	0.010	0.010	+/- 0.002
c	0.008	0.008	0.008	+/- 0.001
e	0.025	0.025	0.025	Basic
N	16	24	28	Reference

Drawing #: MDP0040	PACKAGE OUTLINE DRAWING
Rev: E	QSOP – 0.150" NARROW BODY PACKAGE
Date: 3/19/01	
Units: Inches	élantec Semiconductor, Inc.
JEDEC Reg: MO-137	HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Notes:
(1) Plastic or metal protrusions of 0.006" maximum per side are not included.
(2) Plastic interlead protrusions of 0.010" maximum per side are not included.
(3) Dimensions "D" and "E1" are measured at Datum Plane "H".
(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>