TPS55065-Q1 Buck and Boost Switched-Mode Regulator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 1B
  - Device CDM ESD Classification Level C4B
- Switched-Mode Regulator
  - 5 V ±2%, Normal Mode
  - 5 V ±3%, Low-Power or Crossover Mode
- Switching Frequency, 440 kHz (Typical)
- Input Operating Range, 1.5 V to 40 V, (V_{driver})
  - 500-mA Load-Current Capability
  - 200-mA Load-Current Capability Down to 2-V Input (V_{driver})
  - 120-mA Load-Current Capability Down to 1.5-V Input (V_{driver})
- Enable Function
- Low-Power Operation Mode
- Switched 5-V Regulated Output on 5Vg With Current Limit
- Programmable Slew Rate and Frequency Modulation for EMI Consideration
- Reset Function With Deglitch Timer and Programmable Delay
- Alarm Function for Undervoltage Detection and Indication
- Thermally Enhanced Package for Efficient Heat Management

2 Applications

- Automotive Infotainment and Cluster
- 12-V Industrial Power Systems
- Servers

3 Description

The TPS55065 is a switched-mode regulator with integrated switches for voltage-mode control. With the aid of external components (LC combination), the device regulates the output to 5 V ±3% for a wide input-voltage range.

The TPS55065 device offers a reset function to detect and indicate when the 5-V output rail is outside of the specified tolerance. This reset delay is programmable using an external timing capacitor on the REST terminal. Additionally, an alarm (A_{OUT}) feature is activated when the input supply rail V_{driver} is below a prescaled specified value (set by the A_{IN} terminal).

The TPS55065 device has a frequency-modulation scheme to minimize EMI. The clock modulator permits a modulation of the switching frequency to reduce interference energy in the frequency band.

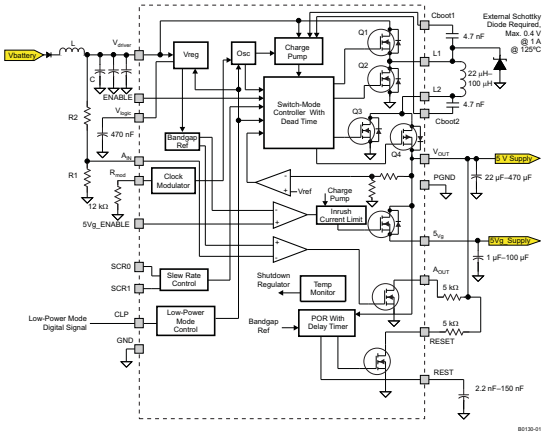
The 5-Vg output is a switched 5-V regulated output with internal current limiting to prevent assertion of RESET when powering a capacitive load on the supply line. This function is controlled by the 5Vg_ENABLE terminal. If there is a short to ground on this output (5Vg output), the output self-protects by operating in a chopping mode. This does, however, increase the output ripple voltage on V_{OUT} during this fault condition.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS55065-Q1	HTSSOP (20)	6.50 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



All component values are typical.

Table of Contents

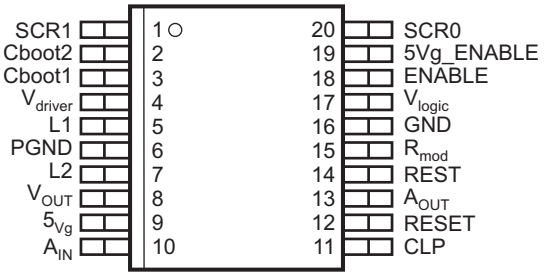
4 Revision History

Changes from Original (October 2008) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 4

5 Pin Configuration and Functions

PWP HTSSOP Package
20 Pins
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SCR1	1	I	Programmable slew-rate control
Cboot2	2	I	External bootstrap capacitor
Cboot1	3	I	External bootstrap capacitor
V_{driver}	4	I	Input voltage source
L1	5	I	Inductor input (an external Schottky diode(1) to GND must be connected to L1)
PGND	6	I	Power ground
L2	7	I	Inductor output
V_{OUT}	8	O	5-V regulated output
5Vg	9	O	Switched 5-V supply
A_{IN}	10	I	Programmable alarm setting
CLP	11	I/O	Low-power operation mode (digital input)
RESET	12	O	Reset function (open drain)
A_{OUT}	13	O	Alarm output (open drain)
REST	14	O	Programmable reset timer delay
R_{mod}	15	I	Main switching frequency modulation setting to minimize EMI
GND	16	I	Ground
V_{logic}	17	O	Supply decoupling output (may be used as a 5-V supply for logic-level inputs)
ENABLE	18	I	Switched-mode regulator enable/disable
5Vg_ENABLE	19	I	Switched 5-V voltage regulator output enable/disable
SCR0	20	I	Programmable slew-rate control
Exposed thermal pad	—	—	Connect to GND or left floating.

(1) Maximum 0.4 V at 1 A at 125°C

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
$V_{(driver)}$ (2)	Unregulated input voltage,	–0.5	40	V
$V_{(AIN)}$, $V_{(ENABLE)}$ (2)	Unregulated inputs	–0.5	40	V
$V_{(Cboot1)}$	Bootstrap voltages		52	V
$V_{(Cboot2)}$			14	V
$V_{(L1)}$	Switch mode voltages	–1	40	V
$V_{(L2)}$		–1	7	V
$V_{(Rmod)}$,$V_{(SCR0)}$,$V_{(SCR1)}$, $V_{(CLP)}$, and $V_{(5Vg\_ENABLE)}$ (2)	Logic input voltages	–0.5	7	V
$V_{(RESET)}$,$V_{(AOUT)}$,$V_{(logic)}$, and $V_{(REST)}$ (2)	Low output voltages	–0.5	7	V
P_D	Continuous power dissipation	See *Dissipation Ratings*		
T_J	Operating virtual junction temperature	–40	150	°C
T_A	Operating ambient temperature	–40	125	°C
T_{stg}	Storage temperature	–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)(2)	Classification 1B for pin 7, pin 8, pin 9	±800	V
		Classification 2 for pins 1 to 6 and 10 to 20	±2000	
	Charged device model (CDM), per AEC Q100-011	Classification Level C4B for All pins	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each terminal.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Unregulated input voltage, $V_{(driver)}$		6		24	V
Unregulated input voltages, $V_{(AIN)}$ and $V_{(ENABLE)}$		0		24	V
Switched-mode terminals	$V_{(L1)}$	–1		17	V
	$V_{(L2)}$	5		5.5	
Bootstrap voltages	$V_{(Cboot1)}$			$V_{(driver)}$ + 10	V
	$V_{(Cboot2)}$			8	
Logic levels (I/O), $V_{(Rmod)}$, $V_{(logic)}$,$V_{(SCR0)}$,$V_{(SCR1)}$,$V_{(5Vg\_ENABLE)}$,$V_{(RESET)}$, $V_{(AOUT)}$, $V_{(CLP)}$, and $V_{(REST)}$		0		5.25	V
Operating ambient temperature range, T_A		–40		125	°C
Logic levels (I/O), $V_{(SCR0)}$, $V_{(SCR1)}$, $V_{(CLP)}$ directly connected to $V_{(logic)}$		$V_{(logic)}$		$V_{(logic)}$	V

6.4 Thermal Information

THERMAL METRIC(1)		TPS55065-Q1 PWP [HTSSOP] 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	20.2	
ψ_{JT}	Junction-to-top characterization parameter	0.7	
ψ_{JB}	Junction-to-board characterization parameter	19.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Dissipation Ratings

$R_{\theta JA}$	POWER RATING $T_A \le 25°C$	DERATING FACTOR ABOVE $T_A = 25°C$	POWER RATING $T_A = 85°C$	POWER RATING $T_A = 125°C$
32°C/W	3.9 W	31.25 mW/°C	2.03 W	0.781 W
40°C/W	3.125 W	25 mW/°C	1.625 W	0.625 W

6.6 Electrical Characteristics

$V_{(driver)}$ = 6 V to 17 V, T_A = -40°C to 125°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(driver)}$	Unregulated input voltage		1.5		40	V
$V_{(driver)}$	Start-up condition voltage	I_O = 500 mA			5	V
S_{OM}	Soft-start ramp	C_O = 36 µF (minimum) to 220 µF (maximum)	4		20	V/ms
		C_O = 220 µF (min) to 470 µF (max), see Note (1)	2		20	
$I_{(standby)}$	Standby current	ENABLE = low		10	20	µA
I_q	Quiescent current	CLP = 0 V, $V_{(driver)}$ = 11 V, I_O = 0 mA		100	160	µA
V_O	Output voltage	DC		5		V
V_O	Output-voltage tolerance	Normal mode			2%	
		Boost/buck crossover or low-power mode			3%	
I_O	Output current	$V_{(driver)}$ ≥ 7 V			0.5	A
$I_{O(Boost)}$	Output current, boost mode	$V_{(driver)}$ = 2 V, see Note (2)			200	mA
		$V_{(driver)}$= 1.5 V, see Note (2)			120	
I_{PPn}	Internal peak current limit (normal mode)	See (1)	1.75		2.5	A
I_{PPl}	Internal peak current limit (low-power mode)	See (1)	0.75		1.25	A
I_P	Peak current	$V_{(driver)}$ = 16 V, I_O = 500 mA, L = 33 µH		1.5		A
$V_{(driver)}$	Boost/buck crossover voltage window	See (3)	5		5.9	V
T_{ot}	Thermal shutdown(4)		160	180	200	°C
5Vg OUTPUT AND ENABLE						
$r_{DS(on)}$	On-state resistance			135	225	mΩ
I_O	Output current				400	mA
V_I	5Vg_ENABLE input-voltage range		–0.5		V_O	V
V_{IH}	5Vg_ENABLE threshold high voltage	$V_{(5Vg)}$ = 5 V	2.5	3	3.5	V
V_{IL}	5Vg_ENABLE threshold low voltage	$V_{(5Vg)}$ = 0 V	1.5	2	2.5	V
$V_{(hys)}$	Hysteresis voltage		0.5	1		V
$r_{(pd)}$	Internal pulldown resistor		300	500	850	kΩ
ENABLE						
V_I	ENABLE input-voltage range		–0.5		40	V
V_{IH}	ENABLE threshold high voltage	8 V ≤ $V_{(driver)}$ ≤ 17 V	2.5	3	3.5	V
		6 V ≤ $V_{(driver)}$ < 8 V	1.9	3	3.5	
V_{IL}	ENABLE threshold low voltage	V_O = 5 V	1.5	2	2.5	V
$V_{(hys)}$	Hysteresis voltage	8 V ≤ $V_{(driver)}$ ≤ 17 V	0.5	1		V
		6 V ≤ $V_{(driver)}$ < 8 V	0.1			

(1) Ensured by characterization.
(2) Tested with inductor having following characteristics: L = 33 µH, R_{max} = 0.1 Ω, I_R = 1.8 A. Output current must be verified in application when inductor R_{max} (ESR) is increased.
(3) Ensured by characterization. For further details, see *Buck/Boost Transitioning*.
(4) Ensured by characterization; hysteresis 15°C (typical)

Electrical Characteristics (continued)

$V_{(driver)}$ = 6 V to 17 V, T_A = -40°C to 125°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESET						
$V_{(th)}$	RESET threshold voltage		4.51	4.65	4.79	V
$V_{(RESET)}$	RESET tolerance				3%	
$t_{(RESET)}$	RESET time	$C_{(REST)}$ = 10 nF	8	10	12	ms
		$C_{(REST)}$ = 100 nF, see (1)	80	100	120	
V_{OL}	RESET output low voltage	I_{sink} = 5 mA			450	mV
		I_{sink} = 1 mA			84	
$t_{(deglitch)}$	RESET deglitch time	See (1)	8	10	12.5	µs
ALARM						
V_I	Alarm input-voltage range		–0.5		40	V
V_{IL}	Alarm threshold low voltage		2.2	2.3	2.35	V
V_{IH}	Alarm threshold high voltage		2.43	2.5	2.58	V
$V_{(hys)}$	Hysteresis voltage			200		mV
V_{OL}	Alarm output low voltage	I_{sink} = 5 mA			450	mV
		I_{sink} = 1 mA			84	
LOW-POWER MODE (PULSE MODE) PFM						
$I_{O(LPM)}$	Load current in low-power mode	$V_{(driver)}$ < 7 V			50	mA
$I_{I(avg)}$	Average input current	$V_{(driver)}$ = 11 V, I_O = 5 mA, CLP = low			3.55	mA
V_O	Output-voltage tolerance	V_O = 5 V		2.4%	3%	
DIGITAL LOW-POWER MODE (CLP)						
V_{IH}	High-level CLP input threshold voltage	Normal mode	2.6			V
V_{IL}	Low-level CLP input threshold voltage	Low-power mode			1.15	V

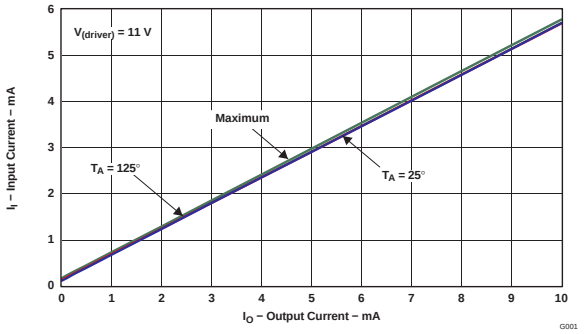
6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(sw)}$	Switching frequency	$V_{(Rmod)}$ = 0 V, modulator OFF		440		kHz
$f_{(sw)ac}$	Operating-frequency accuracy	$f_{(sw)}$ = 440 kHz			20%	
$f_{(sw)min}$	Modulation minimum frequency		270	330	445	kHz
$f_{(sw)max}$	Modulation maximum frequency		450	550	680	kHz
$f_{(mod)span}$	Modulation span			220		kHz
$f_{(mod)}$	Modulation frequency	R_{mod} = 12 kΩ ±1%		28		kHz
$f_{(mod)ac}$	Modulation-frequency accuracy				12%	

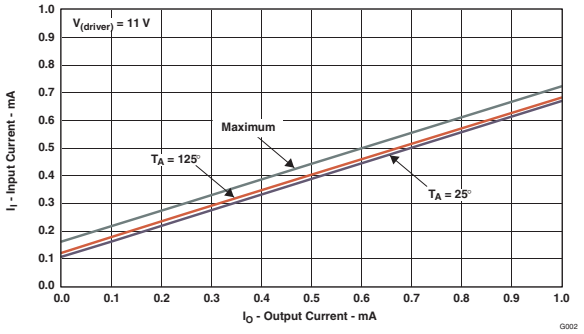
6.8 Typical Characteristics

(Reference L1 Terminal, see Figure 8 through Figure 10)



Maximum characteristic specified by design.

Figure 1. Low-Power Mode Current, I_O = 0 mA–10 mA



Maximum characteristic specified by design.

Figure 2. Low-Power-Mode Current, I_O = 0 mA–1 mA

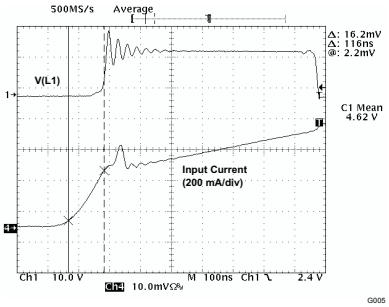


Figure 3. Input Current with Slope Control, SCR0 = 0, SCR1 = 0, Input-Current Slew Rate = 2.8 A/µs, I_L = 500 mA, $V_{(driver)}$ = 15 V

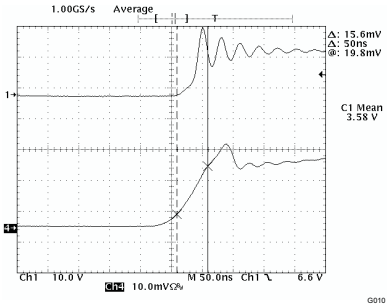


Figure 4. Input Current with Slope Control, SCR1 = 0, SCR0 = 1, Input-Current Slew Rate = 6.25 A/µs, I_L = 500 mA, $V_{(driver)}$ = 15 V

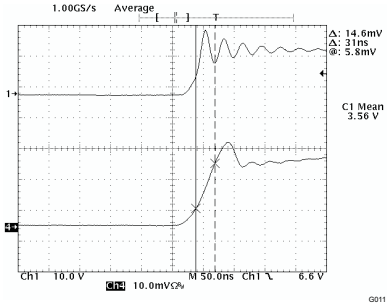


Figure 5. Input Current with Slope Control, SCR1 = 1, SCR0 = 0, Input-Current Slew Rate = 9.4 A/µs, I_L = 500 mA, $V_{(driver)}$ = 15 V

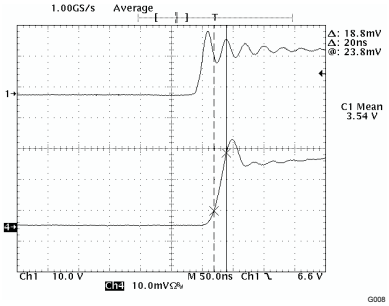


Figure 6. Input Current With Slope Control, SCR0 = 1, SCR1 = 1, Input-Current Slew Rate = 18.8 A/µs, I_L = 500 mA, $V_{(driver)}$ = 15 V

Typical Characteristics (continued)

(Reference L1 Terminal, see Figure 8 through Figure 10)

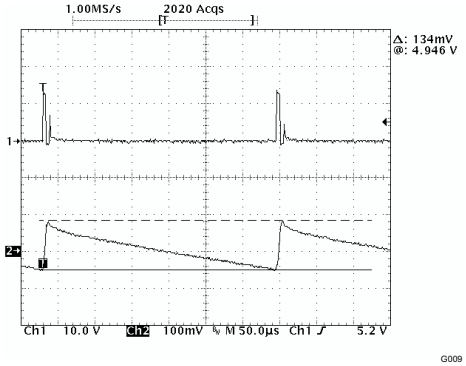


Figure 7. Low-Power-Mode Operation, I_L = 15 mA, C_O = 47 µF

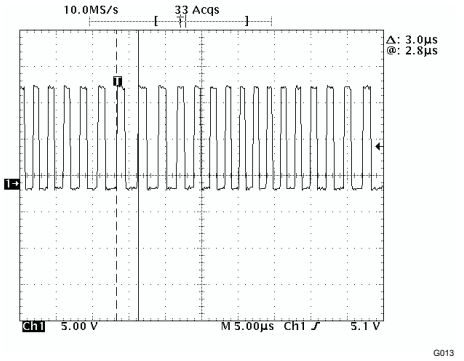


Figure 8. Minimum Switching Frequency (333 kHz) with Modulation Enabled, R_{mod} = 12 kΩ, I_L = 200 mA

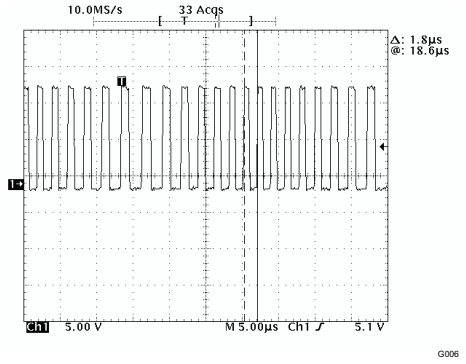


Figure 9. Maximum Switching Frequency (555 kHz) With Modulation Enabled, R_{mod} = 12 kΩ, I_L = 200 mA

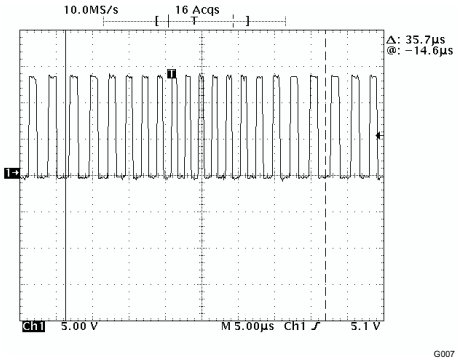


Figure 10. Modulation Frequency (Full Span) of 28 kHz

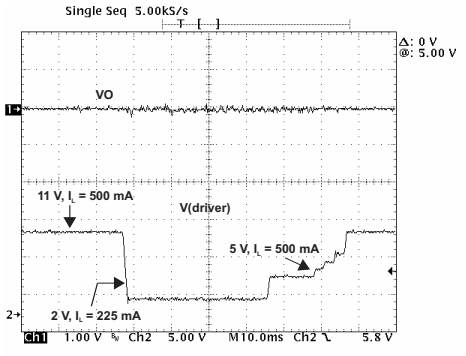


Figure 11. Input Voltage Excursions (Similar to Low-Crank Conditions)

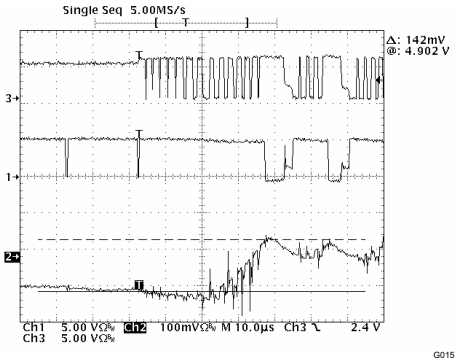


Figure 12. Switched-Mode Regulator Transition from Buck Mode to Boost Mode, I_L = 400 mA

Typical Characteristics (continued)

(Reference L1 Terminal, see Figure 8 through Figure 10)

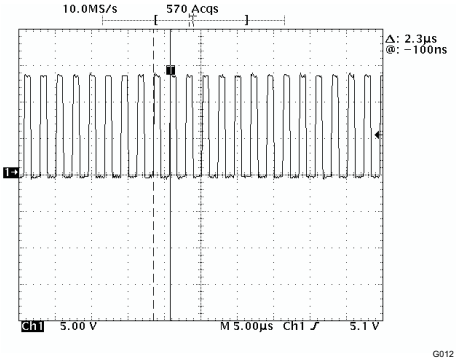


Figure 13. Nominal Switching Frequency of Q1 Switch (446 kHz) With Modulation Function Disabled, I_L = 200 mA

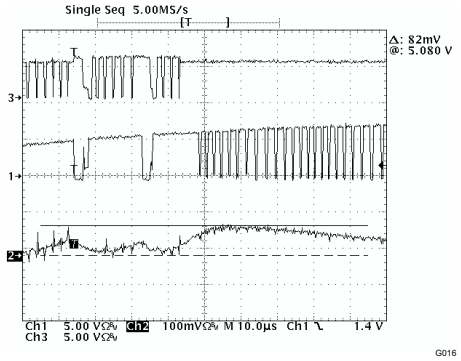
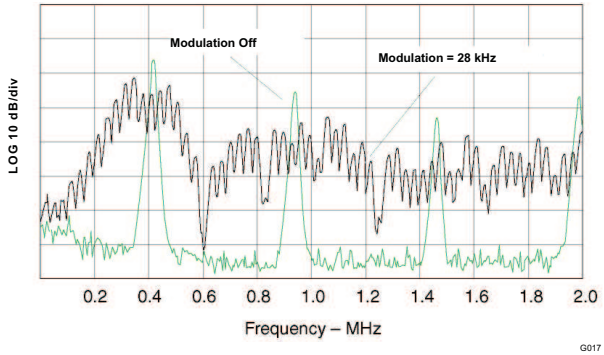
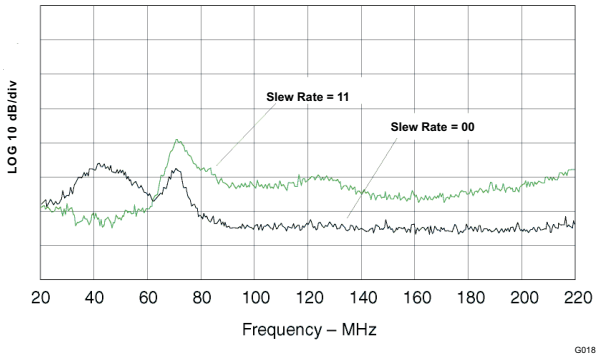


Figure 14. Switched-Mode Regulator Transition from Boost Mode to Buck Mode, I_L = 400 mA



These values represent conducted EMI results of a test board for display purposes only. Actual results may vary greatly depending on board layout and external components and must be verified in actual application.

Figure 15. Conducted Emissions on Test Board Showing Effects of Switching-Frequency Modulation



These values represent conducted EMI results of a test board for display purposes only. Actual results may vary greatly depending on board layout and external components and must be verified in actual application.

Figure 16. Conducted Emissions on Test Board Showing Effects of Minimum and Maximum Slew Rate Settings

7 Detailed Description

7.1 Overview

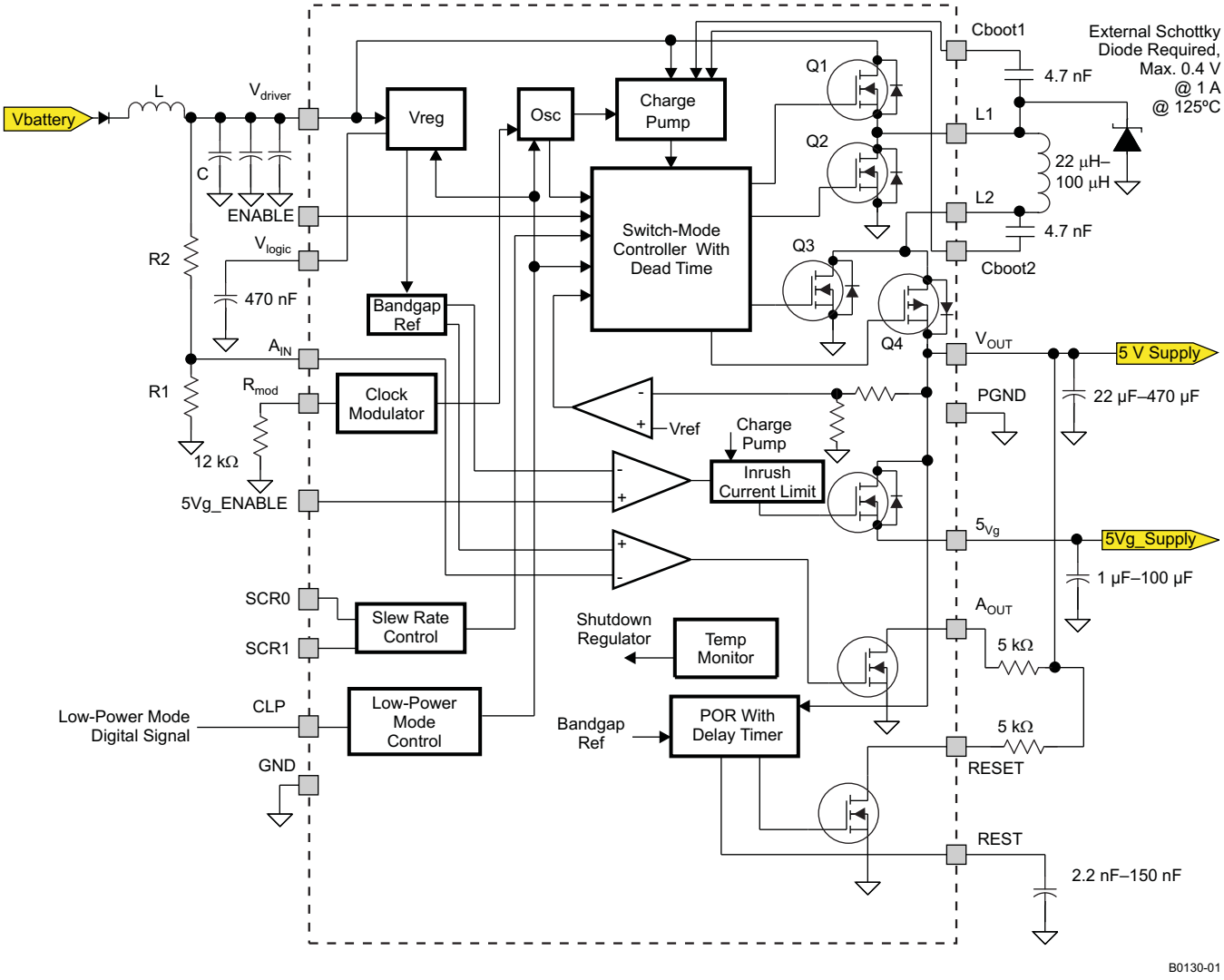
The TPS55065 is a buck/boost switched-mode regulator that operates in a power-supply concept to ensure a stable output voltage with input voltage excursions and specified load range.

The device provides an alarm indicator and reset output to interface with systems that require supervisory function.

The switching regulator offers a clock modulator and a current-mode slew-rate control for the internal switching transistor (Q1) to minimize EMI.

An internal low-$r_{DS(on)}$ switch has a current-limit feature to prevent inadvertent reset when turning on the 5-Vg output.

7.2 Functional Block Diagram



All component values are typical.

7.3 Feature Description

7.3.1 Switched-Mode Input/Output Terminals (L1, L2)

The external inductor for the switched-mode regulator is connected between terminals L1 and L2. This inductor is placed close to the terminals to minimize parasitic effects. For stability, use an inductor with 20 µH to 100 µH.

7.3.2 Supply Terminal (V_{driver})

The input voltage of the device is connected to the V_{driver} terminal. This input line requires a filter capacitor to minimize noise. TI recommends using a low-ESR aluminum or tantalum input capacitor. The relevant parameters for the input capacitor are the voltage rating and RMS current rating. The voltage rating should be approximately 1.5 times the maximum applied voltage for an aluminum capacitor and 2 times for a tantalum capacitor. In buck mode, the RMS current is $I_{OUT} \times \sqrt{D - D^2}$, where D is the duty cycle and its maximum RMS current value is reached when D = 50% with $I_{RMS} = I_{OUT}/2$. In boost mode, the RMS current is 0.3 × ΔI, where ΔI is the peak-to-peak ripple current in the inductor. To achieve this, ESR ceramic capacitors are used in parallel with the aluminum or tantalum capacitors.

7.3.3 Internal Supply Decoupling Terminal (V_{logic})

The V_{logic} terminal is used to decouple the internal power-supply noise by use of a 470-nF capacitor. This terminal can also be used as an output supply for the logic-level inputs for this device (SCR0, SCR1, ENABLE, CLP, and 5Vg_ENABLE).

7.3.4 Input Voltage Monitoring Terminal (A_{IN})

The A_{IN} terminal is used to program the threshold voltage for monitoring and detecting undervoltage conditions on the input supply. A maximum of 40 V may be applied to this terminal and the voltage at this terminal may exceed the $V_{(driver)}$ input voltage without effecting the device operation. The resistor divider network is programmed to set the undervoltage detection threshold on this terminal (see the application schematic). The input has a typical hysteresis of 200 mV with a typical upper limit threshold of 2.5 V and a typical lower limit threshold of 2.3 V. When $V_{(AIN)}$ falls below 2.3 V, $V_{(AOUT)}$ is asserted low; when $V_{(AIN)}$ exceeds 2.5 V, $V_{(AOUT)}$ is in the high-impedance state.

The equations to set the upper and lower thresholds of $V_{(AIN)}$ are:

Upper:

$$V_{(driver)} = 2.5\ V \times \frac{R1 + R2}{R1}$$

Lower:

$$V_{(driver)} = 2.3\ V \times \frac{R1 + R2}{R1} \quad (1)$$

7.3.5 Input Undervoltage Alarm Terminal (A_{OUT})

The A_{OUT} terminal is an open-drain output that asserts low when the input voltage falls below the set threshold on the A_{IN} input.

7.3.6 Reset Delay Timer Terminal (REST)

The REST terminal sets the desired delay time to assert the RESET terminal low after the 5-V supply has exceeded 4.65 V (typical). The delay can be programmed in the range of 2.2 ms to 150 ms using capacitors in the range of 2.2 nF to 150 nF. The delay time is calculated using Equation 2:

$$\text{RESET delay} = C_{(REST)} \times 1\ \text{ms}$$

where $C_{(REST)}$ has nF units. (2)

7.3.7 Reset Terminal (RESET)

The RESET terminal is an open-drain output. The power-on reset output is asserted low until the output voltage exceeds the 4.65-V threshold and the reset delay timer has expired. Additionally, whenever the ENABLE terminal is low, RESET is immediately asserted low regardless of the output voltage.

Feature Description (continued)

7.3.8 Main Regulator Output Terminal (V_{OUT})

The V_{OUT} terminal is the output of the switched-mode regulated supply. This terminal requires a filter capacitor with low-ESR characteristics to minimize output ripple voltage. For stability, a capacitor with 22 µF to 470 µF should be used. The total capacitance at pin V_{OUT} and pin 5Vg must be less than or equal to 470 µF.

7.3.9 Low-Power-Mode Terminal (CLP)

The CLP terminal controls the low-power mode of the device. An external low digital signal switches the device to low-power mode or normal mode when the input is high.

7.3.10 Switch-Output Terminal (5Vg)

The 5Vg terminal switches the 5-V regulated output. The output voltage of the regulator can be enabled or disabled using this low-$r_{DS(on)}$ internal switch. This switch has a current-limiting function to prevent generation of a reset signal at turnon caused by the capacitive load on the output or overload condition. When the switch is enabled, the regulated output may deviate and drop momentarily to a tolerance of 7% until the 5Vg capacitor is fully charged. This deviation depends on the characteristics of the capacitors on V_{OUT} and 5Vg.

7.3.11 5Vg-Enable Terminal (5Vg_ENABLE)

The 5Vg_ENABLE is a logic-level input for enabling the switch output on 5Vg.

For the functional terminal, see 5Vg_ENABLE results in Table 1:

Table 1. 5Vg_ENABLE Function

5Vg_ENABLE	Function
0	5Vg is off
Open (internal pulldown = 500 kΩ)	5Vg is off
1	5Vg is on

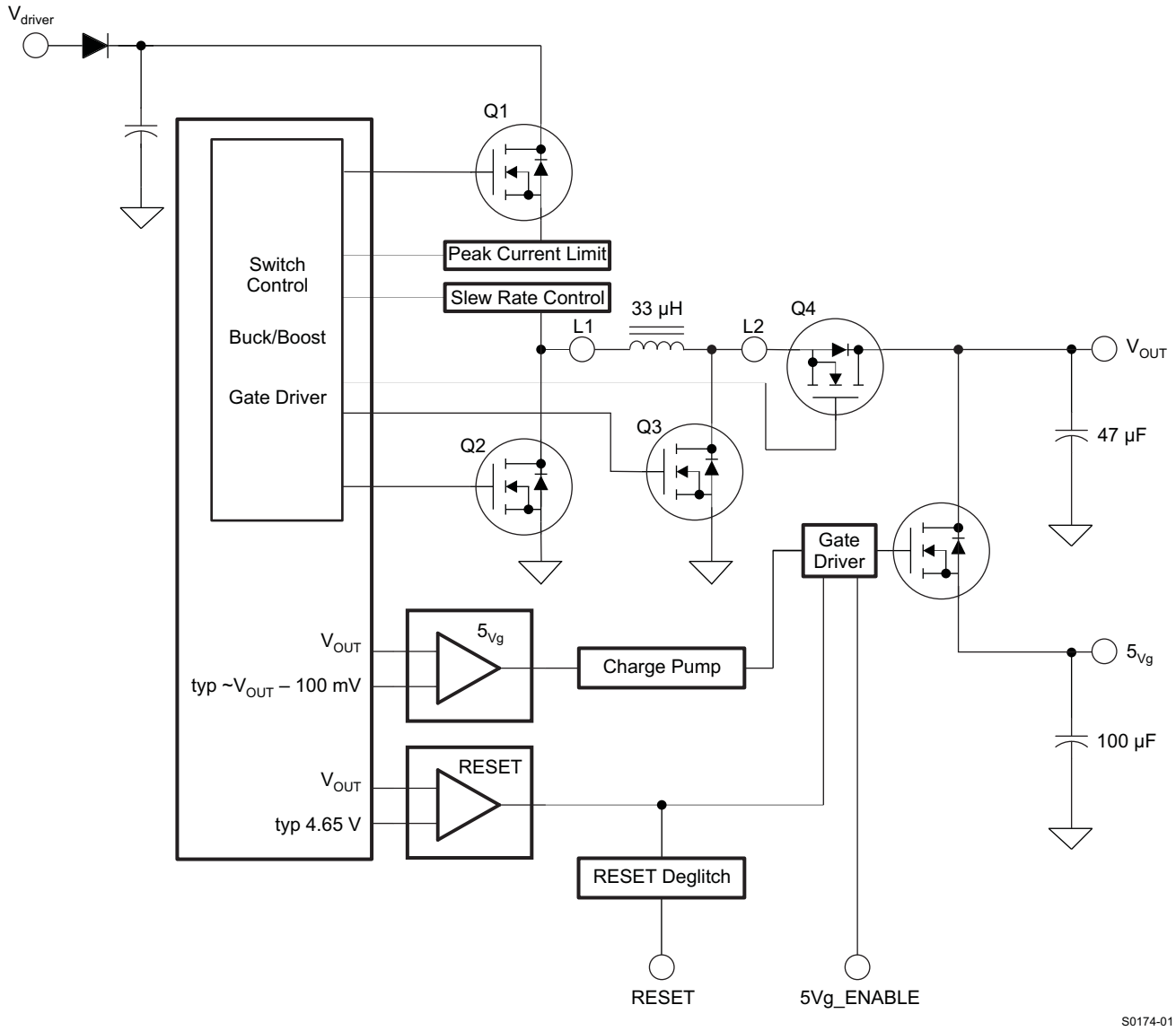


Figure 17. Current-Limit Switched Output 5Vg

7.3.12 Slew-Rate Control Terminals (SCR0, SCR1)

The slew rate of the switching transistor Q1 is set using the SCR0 and SCR1 terminals.

Table 2 shows the values of the slew rate (SR):

Table 2. SR Values

SCR1	SCR0	SR_{Q1}
0	0	Slow
0	1	Medium-slow
1	0	Medium-fast
1	1	Fast

See the converter efficiency plots in the *Typical Characteristics* section to determine power dissipation.

7.3.13 Modulator Frequency Setting (Terminal R_{mod})

The R_{mod} terminal adjusts the clock modulator frequency. A resistor of R_{mod} = 12 kΩ generates a modulation frequency of 28 kHz. The modulator function may be disabled by connecting R_{mod} to GND and the device operates with the nominal frequency. The modulator function cannot be activated during IC operation, only at IC start-up.

7.3.14 Ground Terminal (PGND)

The PGND terminal is the power ground for the device.

7.3.15 Enable Terminal (ENABLE)

The ENABLE terminal allows the enabling and disabling of the switch mode regulator. A maximum of 40 V may be applied to this terminal to enable the device and increasing it above the $V_{(driver)}$ input voltage does not affect the device operation.

The functionality of the ENABLE terminal is described in Table 3:

Table 3. ENABLE Function

ENABLE	Function
0	Vreg is off
Open	Undefined
1	Vreg is on

7.3.16 Bootstrap Terminals (CBOOT1 and CBOOT2)

An external bootstrap capacitor is required for driving the internal high-side MOSFET switch. A 4.7-nF ceramic capacitor is typically required.

7.4 Device Functional Modes

7.4.1 Clock Modulator

To minimize EMI issues associated with the switched-mode regulator, the device offers an integrated clock modulator. The function of the clock modulator is to modulate the switching frequency and to distribute the energy over the wave band.

The average switching frequency is 440 kHz (typical) and varies between 330 kHz and 550 kHz at a rate set by the R_{mod} resistor. A typical value of 12 kΩ on the R_{mod} terminal relates to a 28-kHz modulation frequency. The clock modulator function can only be activated during IC start-up, not during IC operation.

The equation for the modulation frequency is as follows:

$$f_{(mod)} \text{ (Hz)} = (-2.2 \times R_{mod}) + 54.5 \text{ kHz}$$

when R_{mod} = 8 kΩ to 16 kΩ. (3)

7.4.2 Buck/Boost Transitioning

The operation mode switches automatically between buck and boost modes depending on the input voltage of $V_{(driver)}$ and output load conditions. During start up, when $V_{(driver)}$ is less than 5.8 V (typical), the device starts in boost mode and continues to run in boost mode until $V_{(driver)}$ exceeds 5.8 V; at which time, the device switches over to buck mode. In buck mode, the device continues to run in buck mode until it is required to switch back to boost to hold regulation. This crossover window to switch to boost mode is when $V_{(driver)}$ is between 5.8 V and 5 V and depends on the loading conditions. When V_{driver} drops below 5.8 V but the device is holding regulation (~2%), the device remains in buck mode. However, when $V_{(driver)}$ is within the 5.8-V to 5-V window and V_{OUT} drops to 4.9 V, the device crosses over to boost mode to hold regulation. In boost mode, the device remains in

Device Functional Modes (continued)

boost mode until $V_{(driver)}$ exceeds 5.8 V; at which time, the device enters the buck mode. When the device is operating in boost mode and $V_{(driver)}$ is in the crossover window of 5.8 V to 5 V, the output regulation may contain a higher than normal ripple and only maintain a 3% tolerance. This ripple and tolerance depends on the loading and improves with a higher loading condition. When the device is operated with low-power mode active (CLP = low) and high output currents (>50 mA), the buck/boost transitioning can cause a reset signal at the RESET pin.

7.4.3 Buck SMPS

In buck mode, the duty cycle of transistor Q1 sets the voltage V_{OUT}. The duty cycle of transistor Q1 varies 10% to 99% depending on the input voltage, $V_{(driver)}$. If the peak inductor current (measured by Q1) exceeds 450 mA (typical), Q2 is turned on for this cycle (synchronized rectification). Otherwise, the current recirculates through Q2 as a free-wheeling diode. The detection for synchronous or asynchronous mode is done cycle-by-cycle.

To avoid a cross-conduction current between Q1 and Q2, an inherent delay is incorporated when switching Q1 off and Q2 on and vice versa.

In buck mode, transistor Q3 is not required and is switched off. Transistor Q4 is switched on to reduce power dissipation.

The switch timings for transistors Q3 and Q4 are not considered. In buck mode, the logical control of the transistors does not change.

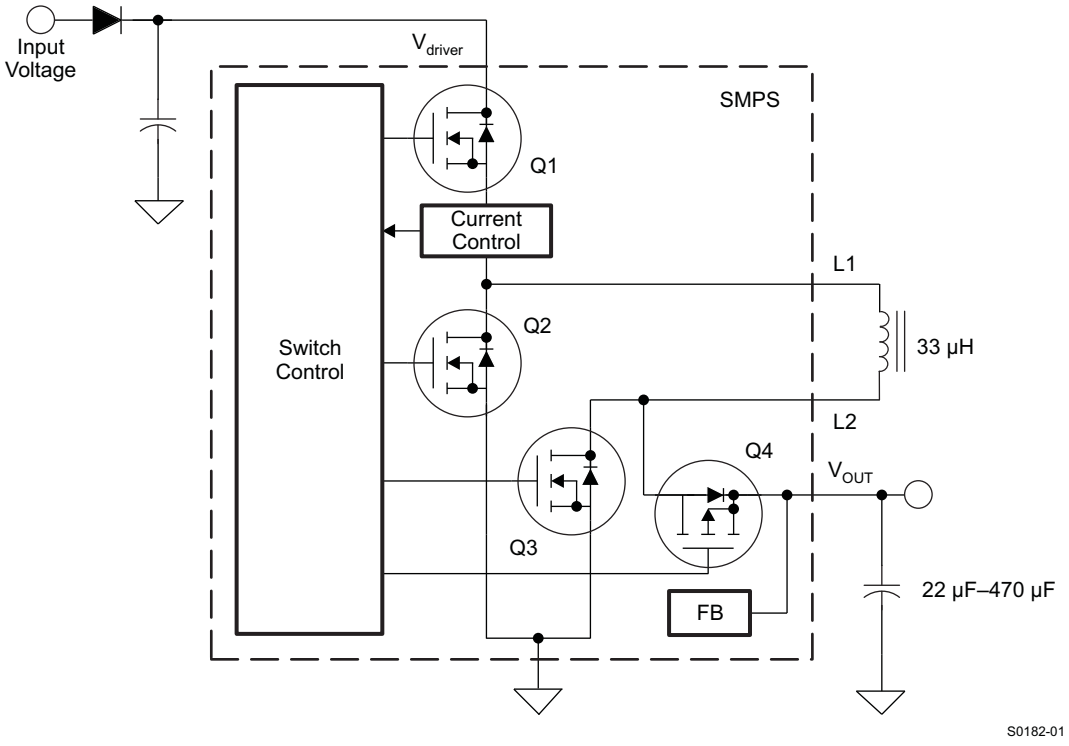


Figure 18. Buck/Boost Switch Mode Configuration

7.4.4 Boost SMPS

In boost mode, the duty cycle of transistor Q3 controls the output voltage V_{OUT}. The duty cycle is internally adjusted 5% to 85% depending on the internally sensed voltage of the output. Synchronized rectification occurs when $V_{(driver)}$ is below 5 V.

To avoid a discharging of the buffer capacitor, a simultaneous switching on of Q3 and Q4 is not allowed. An inherent delay is incorporated between Q3 switching off and Q4 switching on and vice versa.

In boost mode, transistor Q2 is not required and remains off. Transistor Q1 is switched on for the duration of the boost-mode operation (serves as a supply line).

Device Functional Modes (continued)

The switch timings of transistors Q1 and Q2 are not considered. In boost mode, the logical control of the transistors does not change.

7.4.5 Extension of the Input Voltage Range on $V_{(driver)}$

To ensure a stable 5-V output voltage with the output load in the specified range, the $V_{(driver)}$ supply must be greater than or equal to 5 V for greater than 1 ms (typical). After a period of 1 ms (typical), the logic may be supplied by the V_{OUT} regulator and the $V_{(driver)}$ supply may be capable of operating down to 1.5 V.

The switched-mode regulator does not start at $V_{(driver)}$ less than 5 V.

7.4.6 Low-Power Mode

To reduce quiescent current and to provide efficient operation, the regulator enters a pulsed mode.

The device enters this mode by a logic-level low on this terminal.

Automatic low-power mode is not available. The low-power-mode function is not available in boost mode. The device leaves low-power mode during boost mode regardless of the logic level on the CLP terminal.

7.4.7 Temperature and Short-Circuit Protection

To prevent thermal destruction, the device offers overtemperature protection to disable the IC. Also, short-circuit protection is included for added protection on V_{OUT} and 5Vg.

7.4.8 Switch Output Terminal (5Vg) Current Limitation

A charge pump drives the internal FET, which switches the primary output voltage V_{OUT} to the 5Vg pin. Protection is implemented to prevent the output voltage from dropping below its specified value while enabling the secondary output voltage. An explanation of the block diagram (see Figure 1) is given by the following example:

- Device is enabled, output voltage V_{OUT} is up and stable.
- 5Vg is enabled (pin 5Vg_ENABLE set to high) with load resistance connected to 5Vg pin.
- If output voltage V_{OUT} drops below typical (V_{OUT} – 100 mV), the charge pump of the 5Vg FET is switched off and the FET remains on for a while as the gate voltage drops slowly.
- If V_{OUT} drops below the RESET threshold of 4.65 V (typical), the FET of the secondary output voltage 5Vg is switched off (gate drawn to ground level).
- A deglitch time ensures that a device reset does not occur if V_{OUT} drops to the reset level during the 5Vg turnon phase.
- If V_{OUT} rises above typical (V_{OUT} – 100 mV), the charge pump of the 5Vg FET is switched on and drives the gate of the 5Vg FET on.

7.4.9 Soft Start

On power up, the device offers a soft-start feature which ramps the output of the regulator at a slew of 10 V/ms. When a reset occurs, the soft start is reenabled. Additionally, if the output capacitor is greater than 220 µF (typical), the slew rate decreases to a value set by the internal current limit. In boost mode, the soft-start feature is not active.

8 Application and Implementation

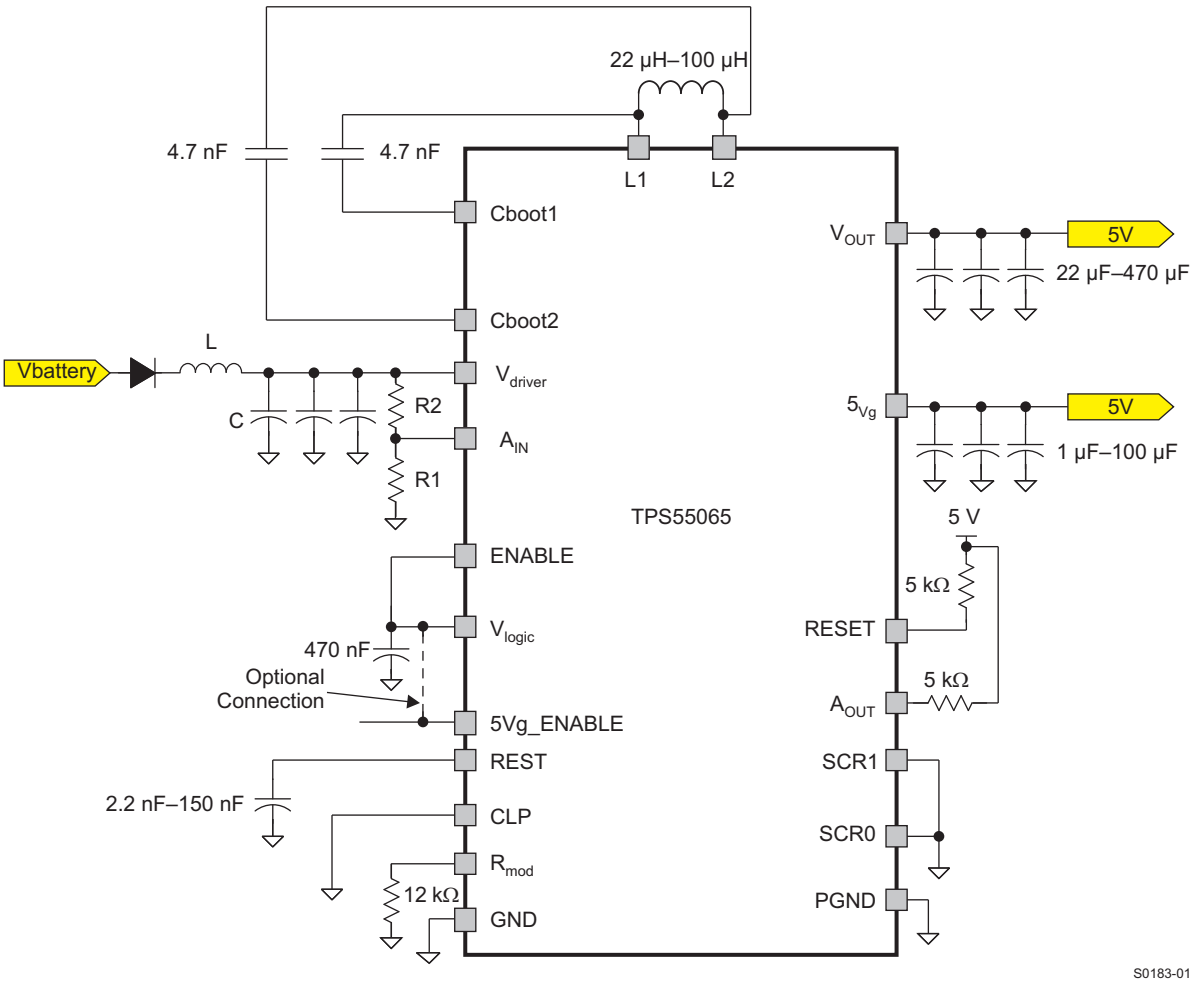
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS55065 can be operated in a buck boost configuration with voltage mode control. The device is capable of monitoring the output as well as the input supply rail. The device also offers a frequency modulation scheme for minimizing EMI. The slew rate is set using the SCR0 and the SCR1 terminals. The average converter efficiency varies with the different slew rate controls of the Q1 switching FET. These variations are demonstrated using this design example at an input voltage of 11 V and 17 V.

8.2 Typical Application



A. To minimize voltage ripple on the output due to transients, it is recommended to use a low-ESR capacitor on the V_{OUT} line.

B. The L and C component values are system application dependent for EMI consideration.

Figure 19. Application Schematic

Typical Application (continued)

NOTE

When this attachment method is not implemented correctly, this product may operate inefficiently. Power dissipation capability may be adversely affected when the device is incorrectly mounted onto the circuit board.

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 4 as the input parameters.

Table 4. Design Parameters

DESIGN PARAMETERS	VALUE
Input voltage V(driver)	11 V to 18 V
Output current (maximum)	500 mA

Four different SCRx settings will be used to analyze the difference in converter efficiency with variations in slew rate (see Figure 20). The Buck equations mentioned in *Buck Mode* will be used to calculate the rest of the design parameters.

8.2.2 Detailed Design Procedure

8.2.2.1 Buck Mode

- Select inductor ripple current ΔI_L: for example, $\Delta I_L = 0.2 \times I_{OUT}$
- Calculate inductor L

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{f_{SW} \times \Delta I_L \times V_{IN}} \ (H) \quad (4)$$

where f_{SW} is the regulator switching frequency.

- Inductor peak current

$$I_{L,max} = I_{OUT} + \frac{\Delta I_L}{2} \ (A) \quad (5)$$

- Output voltage ripple

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right) \left(V_{(p-p)} \right) \quad (6)$$

Usually, the first term is dominant.

$$C_{OUT} = \frac{I_{pk} (t_{ON} + t_{OFF})}{8 \times V_{ripple}} \ (F) \quad (7)$$

Using the previous equations, with Vin (maximum) as 18 V, Vout as 5 V, f_{SW} as 440 kHz, and Inductor ripple current of 0.1 A, the inductance is calculated to be 82.1 µH with inductor peak current as 0.55 A.

8.2.2.2 Boost Mode

- Select inductor ripple current ΔI_L: for example $\Delta I_L = 0.2 \times I_{IN}$
- Calculate inductor L

$$L = \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{f_{SW} \times \Delta I_L \times V_{OUT}} \ (H) \quad (8)$$

where f_{SW} is the regulator switching frequency.

- Inductor peak current

$$I_P = I_{L,max} = I_{IN} + \frac{\Delta I_L}{2} \ (A) \quad (9)$$

- Output voltage ripple

$$\Delta V_{OUT} = I_P \times ESR + \frac{I_{OUT} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)}{f_{SW} \times C_{OUT}} \left(V_{(p-p)}\right) \quad (10)$$

8.2.3 Application Curve

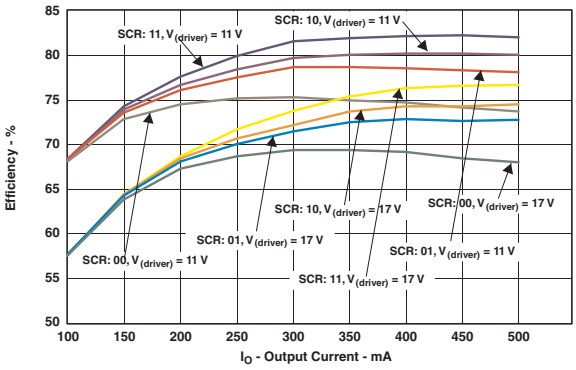


Figure 20. Converter Efficiency

9 Power Supply Recommendations

The TPS55065-Q1 device is designed to operate from an input voltage up to 40 V. Ensure that the input supply is well regulated. Furthermore, if the supply voltage in the application is likely to reach negative voltage (for example, reverse battery), a forward diode must be placed at the input of the supply. For the V_{IN} pin, a good quality ceramic capacitor is recommended. Capacitance de-rating for aging, temperature, and DC bias must be taken into account while determining the capacitor value. The decoupling capacitor must be as close as possible to the Input pin for proper filtering. The use of a low-ESR capacitor at the V_{OUT} line is recommended to minimize the voltage ripple on the output due to transients. The L and C component values can be chosen as per specifications.

10 Layout

10.1 Layout Guidelines

The following guidelines are recommended for PCB layout of the TPS55065 device.

10.1.1 Inductor

Use a low-EMI inductor with a ferrite-type closed core. Other types of inductors may be used; however, they must have low-EMI characteristics and be located away from the low-power traces and components in the circuit.

10.1.2 Filter Capacitors

Input ceramic filter capacitors should be located in the close proximity of the V_{driver} terminal. Surface-mount capacitors are recommended to minimize lead length and reduce noise coupling.

10.1.3 Traces and Ground Plane

All power (high-current) traces should be thick and as short as possible. The inductor and output capacitors should be as close to each other as possible. This reduces EMI radiated by the power traces due to high switching currents.

In a two-sided PCB, it is recommended to have ground planes on both sides of the PCB to help reduce noise and ground-loop errors. The ground connection for the input and output capacitors and IC ground should be connected to this ground plane.

Layout Guidelines (continued)

In a multilayer PCB, the ground plane is used to separate the power plane (where high switching currents and components are placed) from the signal plane (where the feedback trace and components are) for improved performance.

Also, arrange the components such that the switching-current loops curl in the same direction. Place the high-current components such that during conduction, the current path is in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles, helping to reduce radiated EMI.

10.2 Layout Example

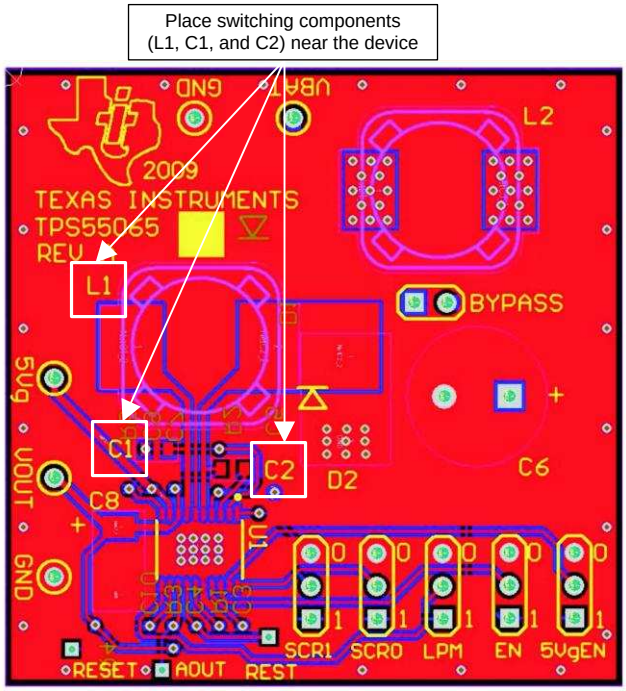


Figure 21. Top Layer

Layout Example (continued)

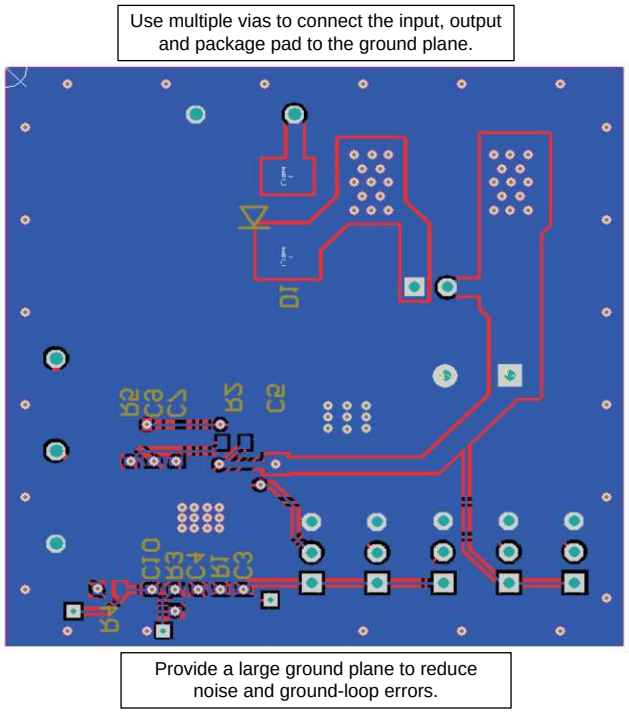


Figure 22. Bottom Layer

To maximize the efficiency of this package for application on a single-layer or multilayer PCB, certain guidelines must be followed when laying out this device on the PCB.

The following information is to be used as a guideline only.

For further information see the *PowerPAD Thermally Enhanced Package* technical brief (SLMA002).

The following are guidelines for mounting the PowerPAD™ IC on a multilayer PCB with a ground plane.

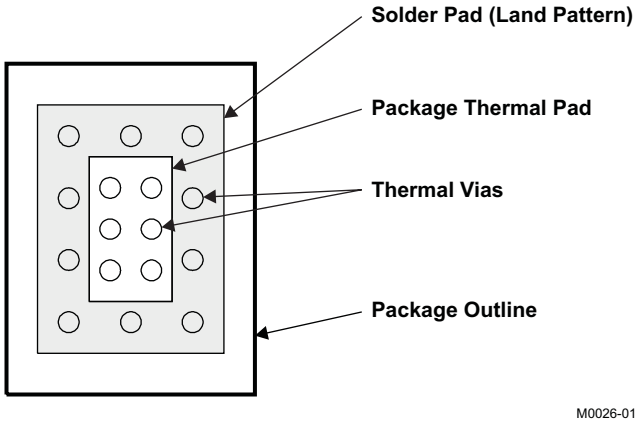


Figure 23. Package and PCB Land Configuration for a Multilayer PCB

Layout Example (continued)

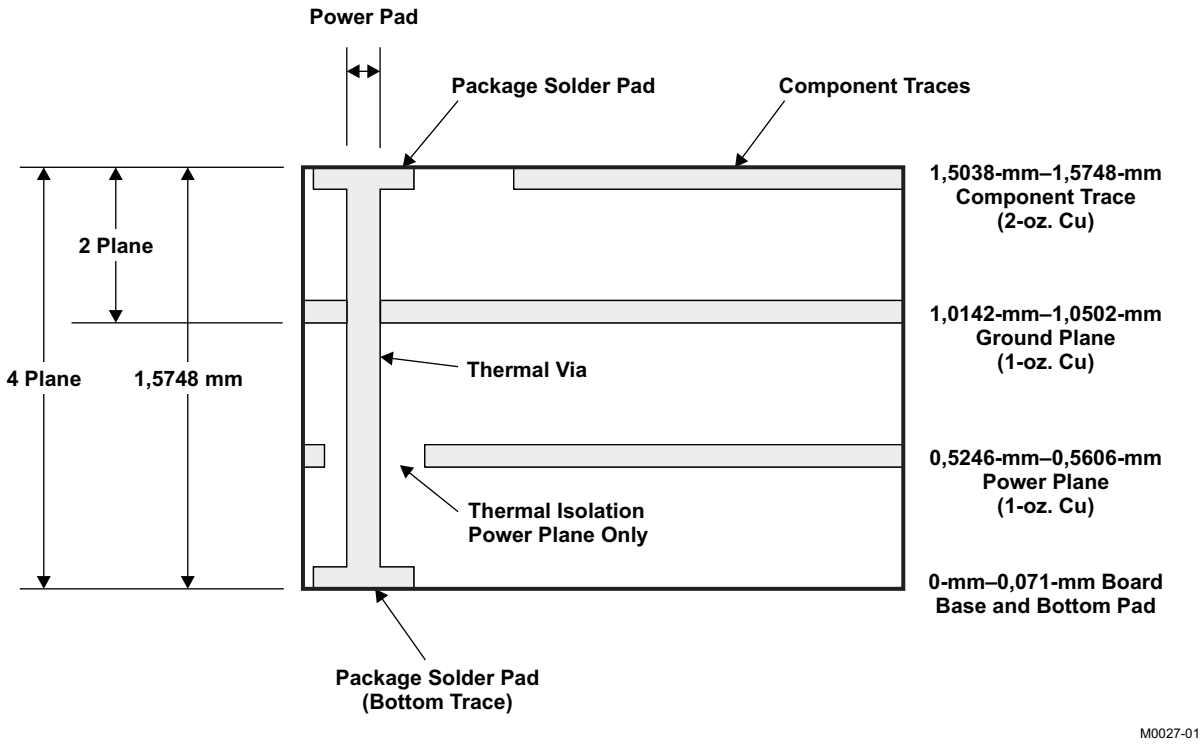


Figure 24. Multilayer Board (Side View)

In a multilayer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane.

The efficiency of this method depends on several factors (die area, number of thermal vias, thickness of copper, and so forth). See the *PowerPAD Thermally Enhanced Package* technical brief (SLMA002).

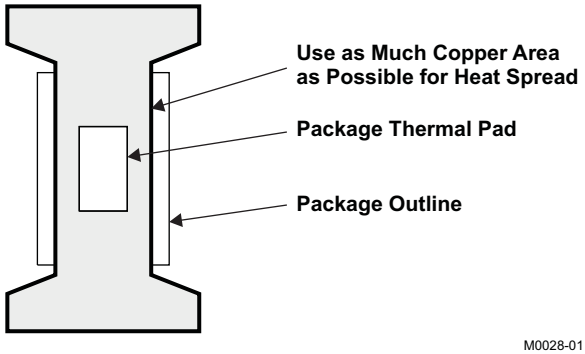


Figure 25. Land Configuration for Single-Layer PCB

Layout recommendation is to use as much copper area for the power-management section of a single-layer board as possible. In a single-layer board application, the thermal pad is attached to a heat spreader (copper areas) by using a low-thermal-impedance attachment method (solder paste or thermal-conductive epoxy). In both of these cases, it is advisable to use as much copper and as many traces as possible to dissipate the heat.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *PowerPAD Thermally Enhanced Package*, SLMA002

11.2 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS55065QPWPRQ1	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	55065Q
TPS55065QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	55065Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

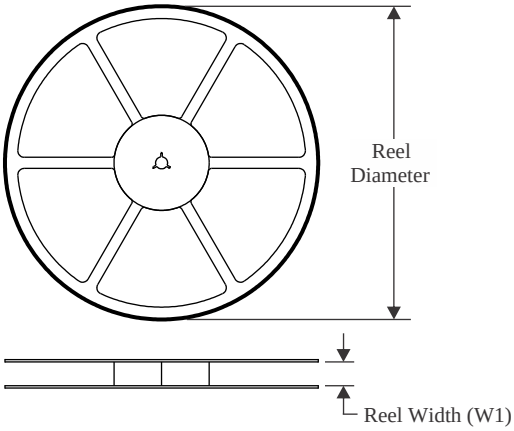
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

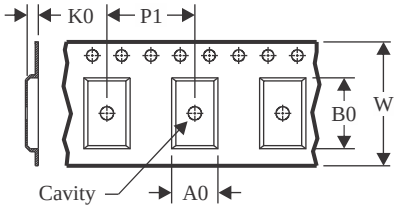
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

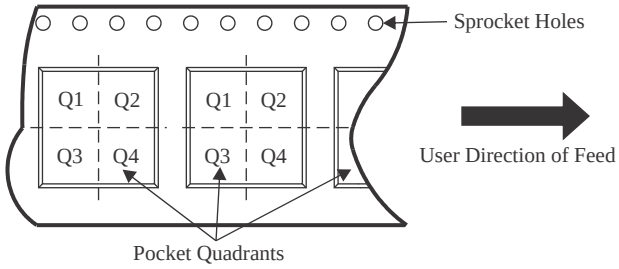


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

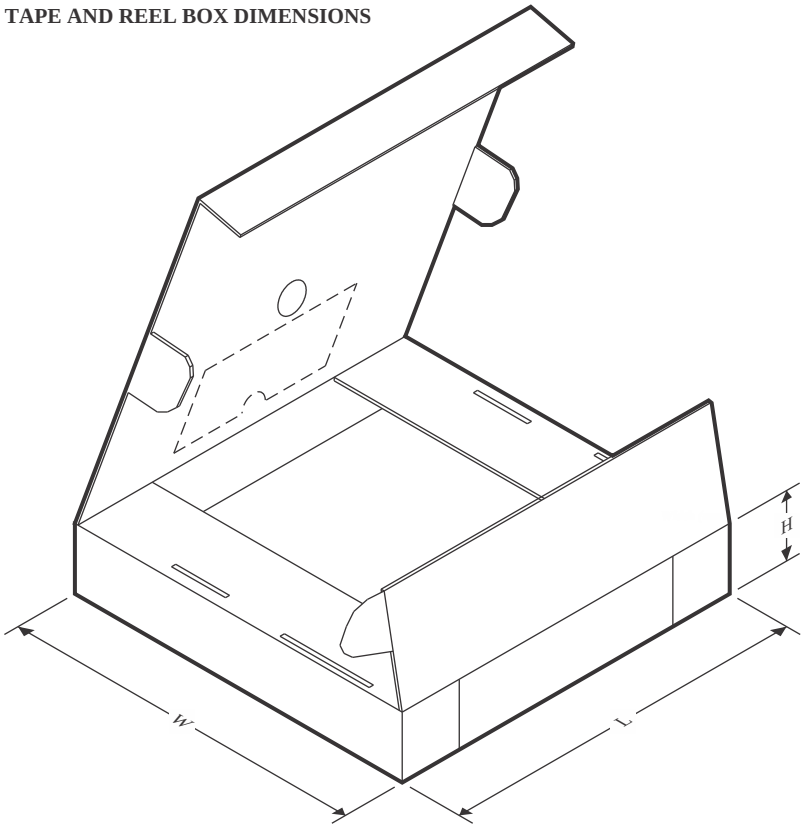
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS55065QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS55065QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

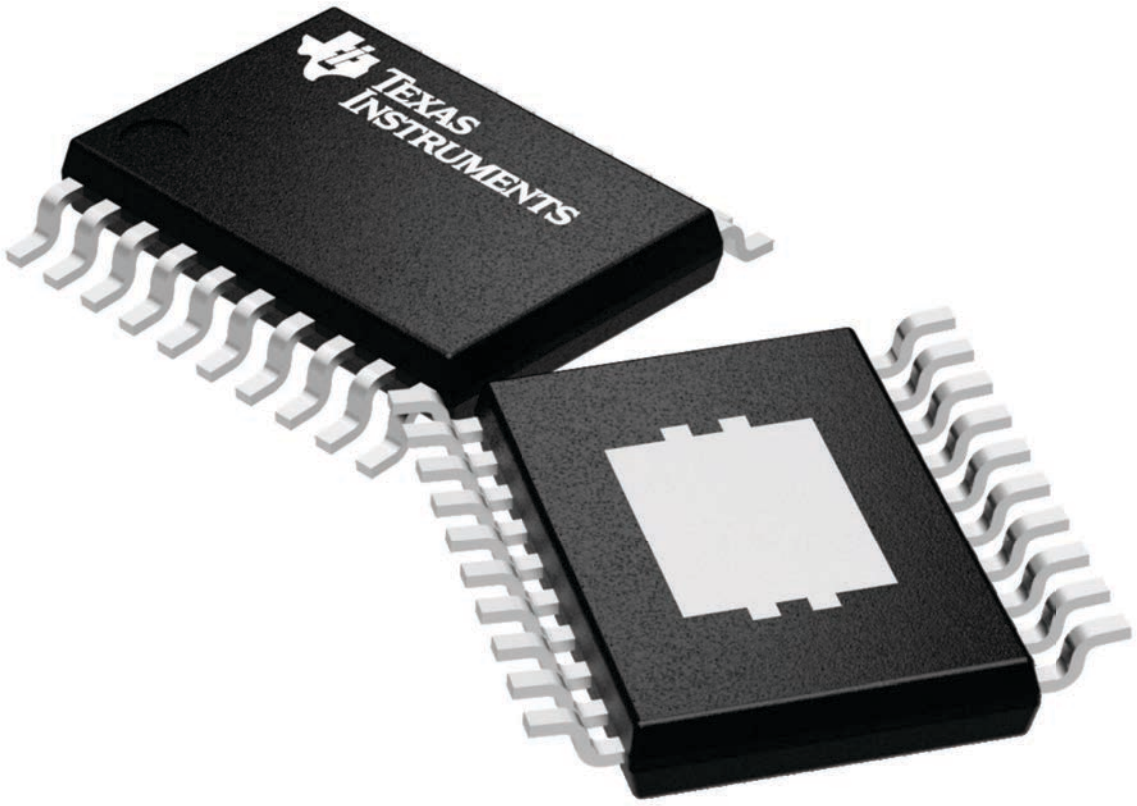
PWP 20

HTSSOP - 1.2 mm max height

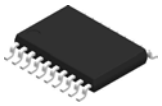
6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

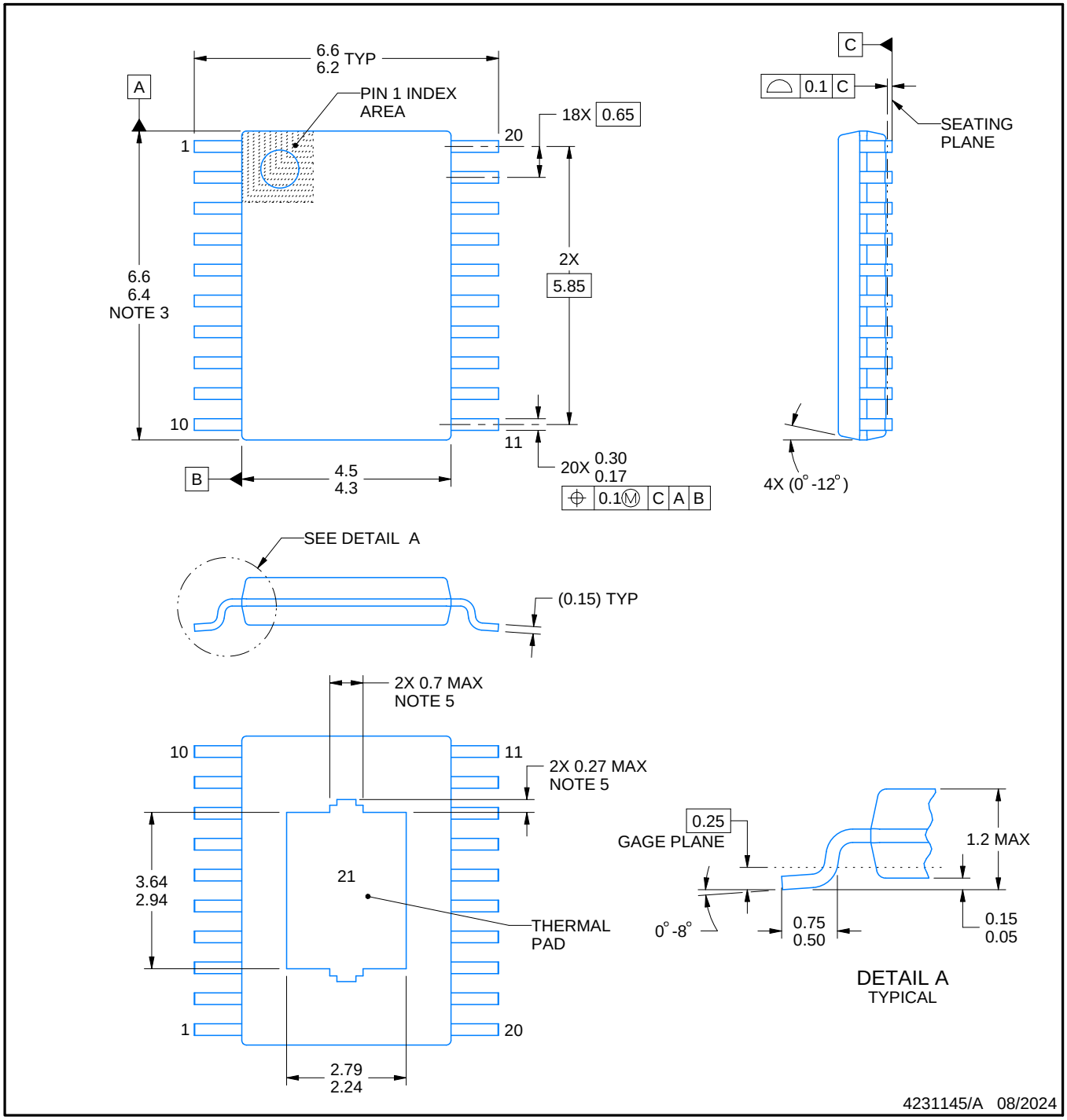


PACKAGE OUTLINE

PWP0020W

PowerPAD™ TSSOP - 1.2 mm max height

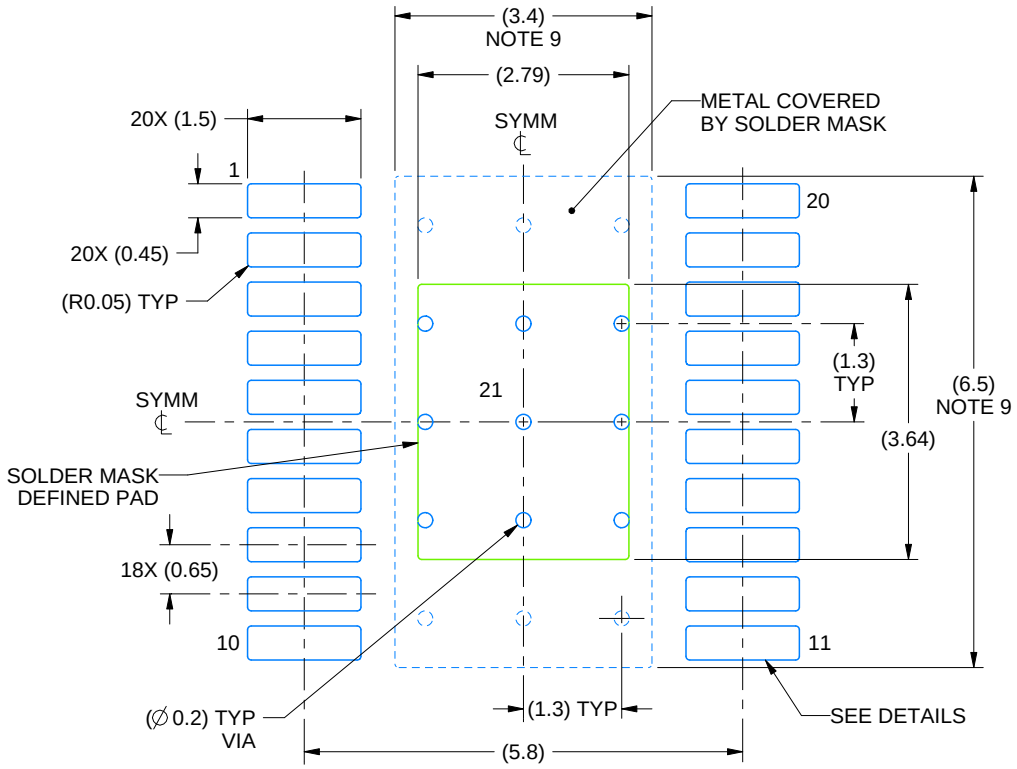
SMALL OUTLINE PACKAGE



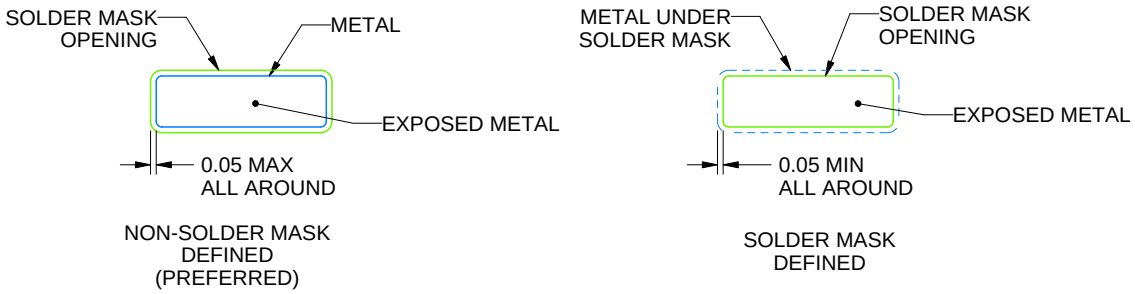
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

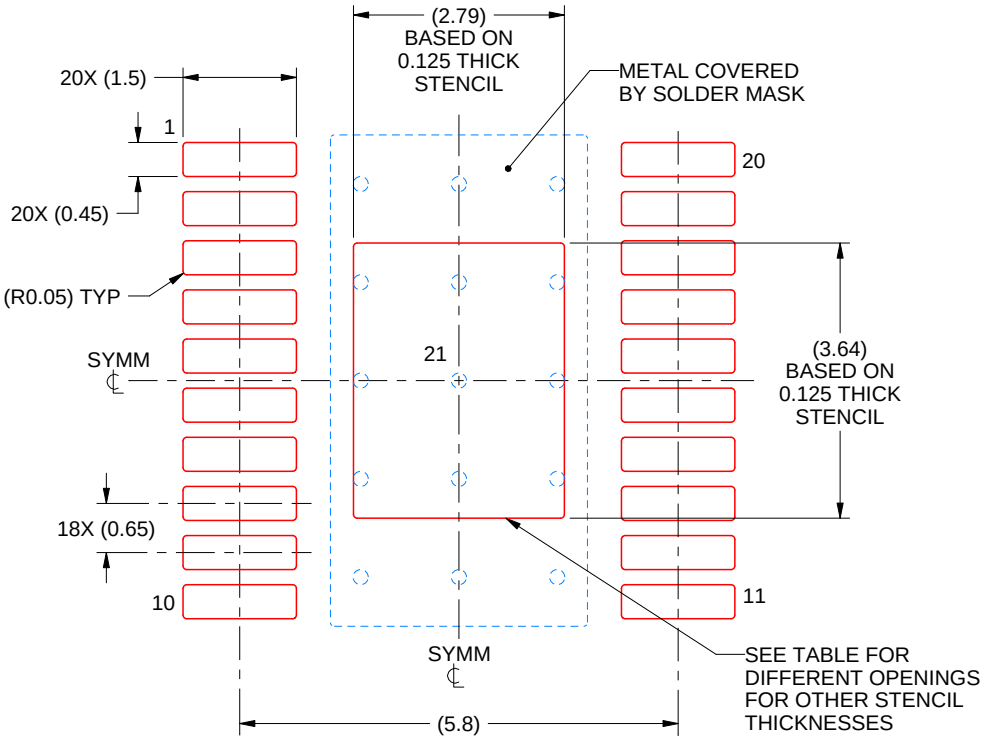


SOLDER MASK DETAILS

4231145/A 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

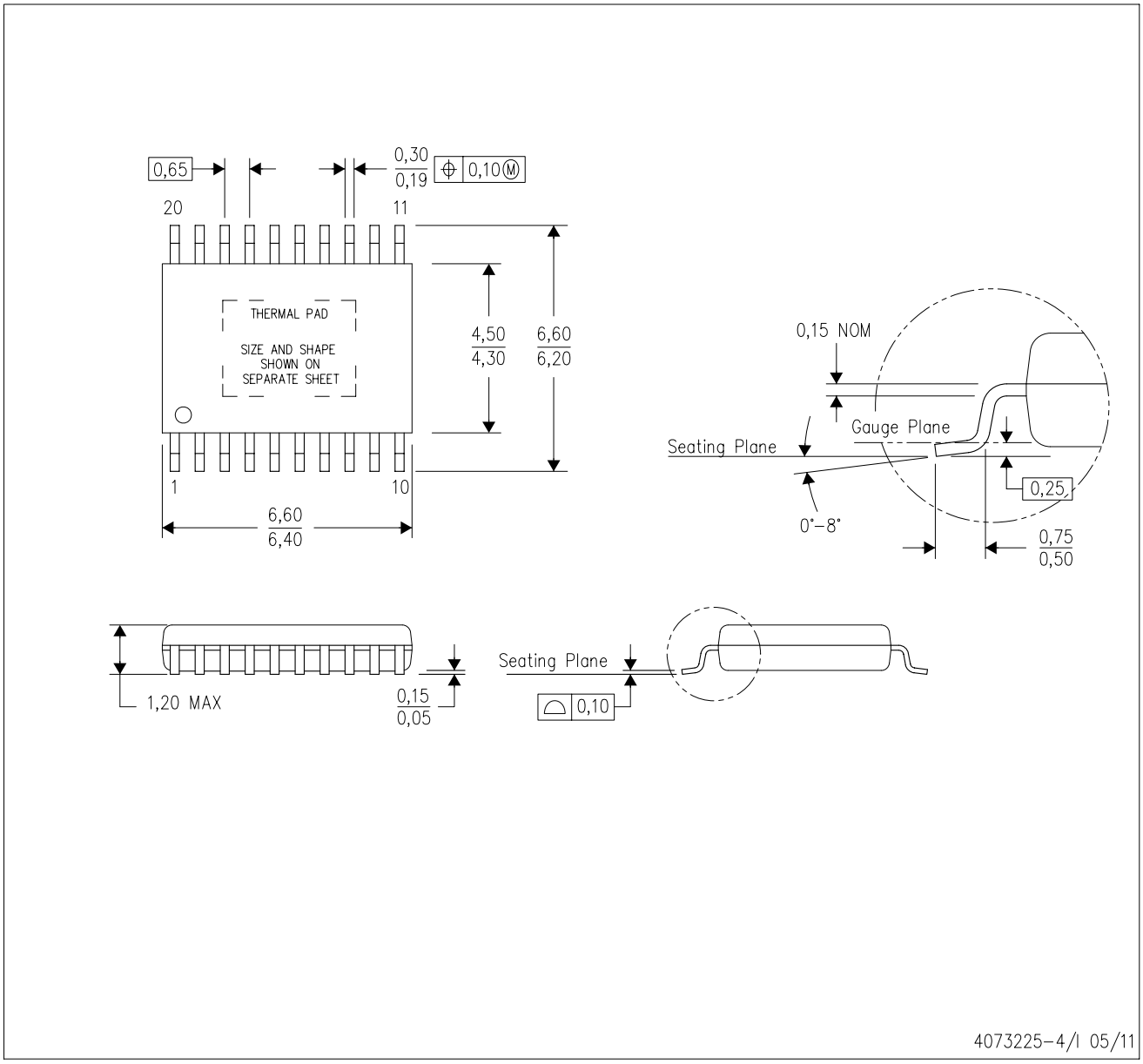
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.12 X 4.07
0.125	2.79 X 3.64 (SHOWN)
0.15	2.55 X 3.32
0.175	2.36 X 3.08

4231145/A 08/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

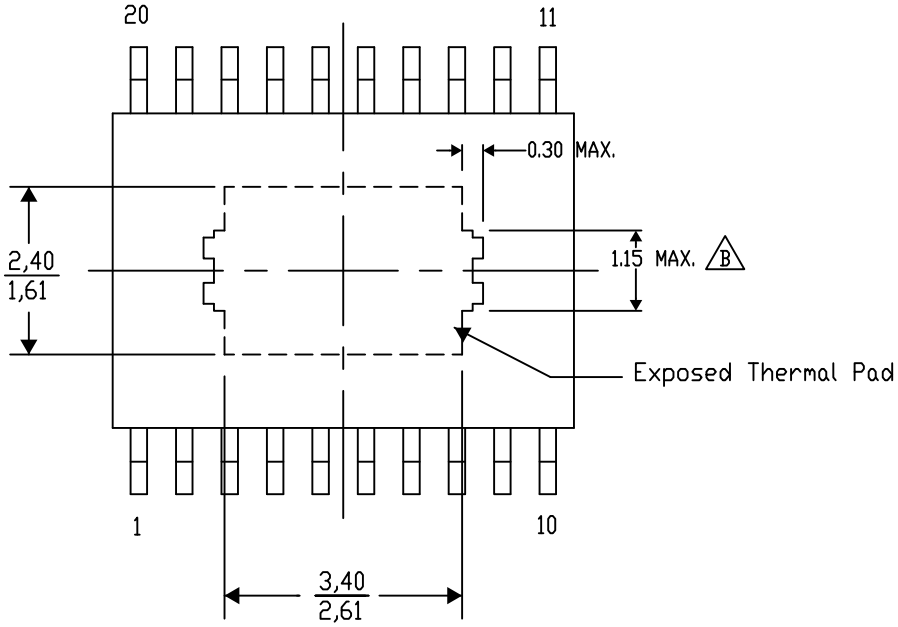
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

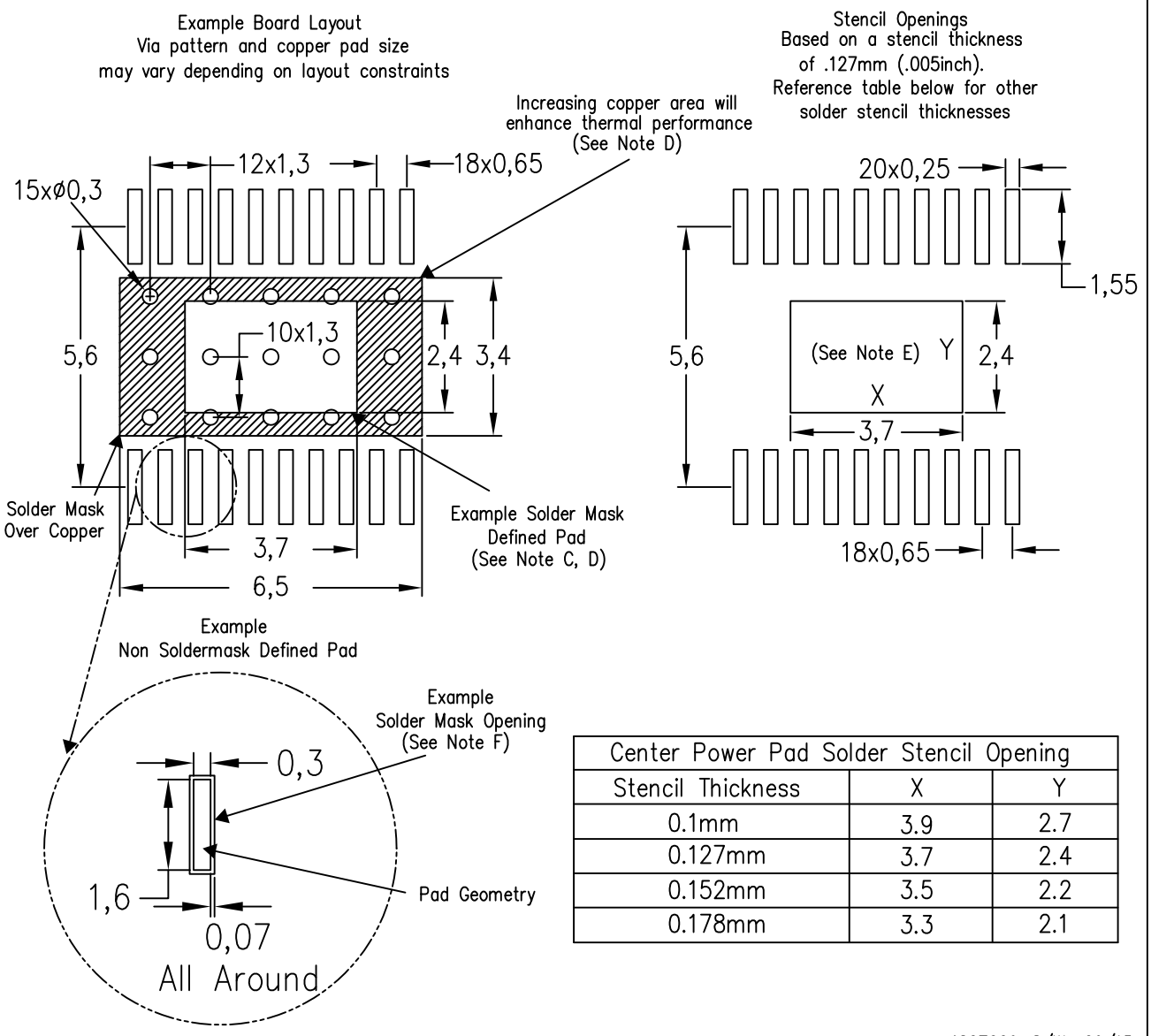
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265