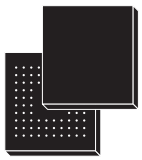
STLC2500A

Bluetooth™ Single Chip

Preliminary Data

Features

- Lowest power consumption
- Efficient support for WLAN coexistence in collocated scenario
- Auto calibration (VCO, Filters)
  - No need for calibration of the RF part
- Total number of external components limited to 7 (6 decoupling capacitors and 1 filter)
- Bluetooth™ specification compliance: V1.1 and V1.2
- Ericsson Technology Licensing Baseband Core (EBC)
- Point-to-point, point-to-multi-point (up to 7 slaves) and scatternet capability
- Asynchronous Connection Oriented (ACL) logical transport link
- Synchronous Connection Oriented (SCO) link: 2 simultaneous SCO channels
- Supports Pitch-Period Error Concealment (PPEC)
- Adaptive Frequency Hopping (AFH): hopping kernel, channel assessment (master & slave)
- Faster connection: Interlaced scan for Page and Inquiry scan, first FHS without random back off, RSSI used to limit range
- Extended SCO (eSCO) links
- HW support for ACL, SCO and eSCO packet types (see *Overview*)
- Clock support for all cellular standards: system clock input and low power clock
- ARM7TDMI CPU with 32-bit core and AMBA (AHB-APB) bus configuration
- Patch RAM capability
- Memory organization: on-chip RAM & ROM
- Communication interfaces: UART, PCM and I2C interfaces and 4 programmable GPIOs



Standard TFBGA 84 pins package

- Ciphering support up to 128 bits key
- Software support up to HCI stack
  - H4 HCI Transport Layer
  - HCI proprietary commands and single HCI command for patch/upgrade download
- Single power supply with internal regulators
- Supports 1.65 to 2.85 Volts IO systems
- Timer and watchdog
- Power class 2. Power class 1 compatible (with external power amplifier)
- Ultra low power architecture with 3 different low power modes: sleep , deep sleep, complete power down
- Dual Wake-up mechanism: initiated by the Host or by the Bluetooth device

Description

The STLC2500A is a single chip ROM-based Bluetooth solution implemented in 0.13 µm ultra low power, low leakage CMOS technology for mobile terminal applications requiring integration up to HCI level. Patch RAM is available, enabling multiple patches/upgrades. The STLC2500A offers multiple interface options. The radio has been designed for single chip requirements and minimal power consumption.

Order codes

Part number	Package	Packing
STLC2500A	TFBGA84	Tray
STLC2500ATR	TFBGA84	Tape on Reel

Contents

1 Overview

The STLC2500A is a single chip ROM-based Bluetooth solution implemented in 0.13 µm ultra low power, low leakage CMOS technology for mobile terminak applications requiring integration up to HCI level. Patch RAM is available enabling multiple patches/upgrades. The STLC2500A main interfaces are UART for HCI transport, PCM for voice and GPIOs for control purposes. The Radio is designed for the single chip requirement and for drastic power consumption reduction.

Features

- Bluetooth™ specification compliance: V1.1 and V1.2
- Ericsson Technology Licensing Baseband Core (EBC)
- Point-to-point, point-to-multi-point (up to 7 slaves) and scatternet capability
- Asynchronous Connection Oriented (ACL) logical transport link
- Synchronous Connection Oriented (SCO) link: 2 simultaneous SCO channels
- Supports Pitch-Period Error Concealment (PPEC)
  - Improves speech quality in the vicinity of interference like e.g. WLAN
  - Used with CVSD air coding
  - Works at receiver, no Bluetooth implication
- Adaptive Frequency Hopping (AFH): hopping kernel, channel assessment as Master and as Slave
- Faster Connection: Interlaced scan for Page and Inquiry scan, first FHS without random back off, RSSI used to limit range
- Extended SCO (eSCO) links
- HW support for packet types
  - ACL: DM1, 3, 5 and DH1, 3, 5
  - SCO: HV1, 3 and DV
  - eSCO: EV3, 5
- Clock support
  - System clock input (digital or sine wave) at 13, 26, 19.2 or 38.4 MHz
  - LPO clock input at 3.2, 16.384, 32 or 32.768 kHz
- ARM7TDMI CPU
  - 32-bit Core
  - AMBA (AHB-APB) bus configuration
- Patch RAM capability
- Memory organization
  - On chip RAM, including provision for patches
  - On chip ROM, preloaded with SW up to HCI
- Communication interfaces
  - Fast UART
  - PCM interface
  - 4 programmable GPIOs
  - External interrupts possible through the GPIOs

  - Fast master I2C interface
- Efficient support for WLAN coexistence in collocated scenario
- Ciphering support up to 128 bits key
- Software support
  - Lower level stack (up to HCI)
  - HCI Transport Layer: H4 (including proprietary extensions)
  - HCI proprietary commands (e.g. peripherals control)
  - Single HCI command for patch/upgrade download
- Single power supply with internal regulators for core voltage generation
- Supports 1.65 to 2.85 Volts IO systems
- Total number of external components limited to 7 (6 decoupling capacitors and 1 filter) thanks to:
  - Fully integrated synthesizer (VCO and loop filter)
  - Integrated antenna switch
  - Low IF receiver
- Auto calibration (VCO, Filters)
- No need for calibration of the RF part
- Timer and watchdog
- Power class 2. Power class 1 compatible (with external power amplifier)
- Ultra low power architecture with 3 different low power levels:
  - Sleep Mode
  - Deep Sleep Mode
  - Complete Power Down Mode
- Initiated Deep Sleep Modes
- Dual Wake-up mechanism: initiated by the Host or by the Bluetooth device
- Standard TFBGA-84 pins package

2 Electrical characteristics

VDD_IO_x means VDD_IO_A, VDD_IO_B. (See also *Table 12*, subsection *Power supply*).

2.1 Absolute maximum ratings

The Absolute Maximum Rating (AMR) corresponds to the maximum value that can be applied without leading to instantaneous or very short-term unrecoverable hard failure (destructive breakdown).

Table 1. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
VDD_HV	Regulator input supply voltage	V_{ss} - 0.3	4.0	V
VDD_IO_x	Supply voltage I/O	V_{ss} - 0.3	4.0	V
V_{ssdiff}	Maximum voltage difference between different types of V_{SS} pins(1)	-0.3	0.3	V
V_{in}	Input voltage of any digital pin	V_{ss} - 0.3	4.0	V
T_{stg}	Storage temperature	-65	+150	°C
T_{lead}	Lead temperature <10s		+250	°C

1. V_{SS} can be any VSS_xxx pin

2.2 Operating ranges

Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not implied.

Table 2. Operating ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{amb}	Operating ambient temperature	-40		+85	°C
VDD_HV	Regulator input supply voltage	2.65(*)	2.75	2.85(1)	V
VDD_IO_A	Supply voltage for I/O	1.65		2.85(2)	V
VDD_IO_B	Supply voltage for I/O	1.35		2.85(2)	V

1. The chip will be characterized from 2.62 [V] up to 2.9 [V]
2. The chip will be characterized up to 2.9 [V].

2.3 I/O specifications

The I/Os comply with the EIA/JEDEC standard JESD8-B.

Table 3. DC input specification (all digital I/Os except system clock)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level input voltage			0.35 * VDD_IO_x	V
V_{IH}	High Level input voltage	0.65 * VDD_IO_x			V
V_{hyst}	Schmitt trigger hysteresis	0.4	0.5	0.6	V

Table 4. DC output specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Low Level output voltage	I_d = X mA		0.15	V
V_{OH}	High Level output voltage	I_d = X mA	VDD_IO_x - 0.15		

Note: X is the source/sink current under worst-case conditions according to the drive capabilities (see Chapter 6)

2.4 Clock specifications

The STLC2500A supports, on the same input pin, the system clock both as a sine wave clock and as a digital clock (see *Table 14* for selection). The system clock section is powered by VDD_CLD (G08 and H09). The voltage range for VDD_CLD is the same as for VDD_IO_A.

Table 5. System clock supported frequencies

Symbol	Parameter	Values	Unit
F_{IN}	Clock input frequency list	13, 26, 19.2, 38.4	MHz

Table 6. System clock overall specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{INTOL}	Tolerance on input frequency	-20		20	ppm

Table 7. System clock, sine wave specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{PP}	Peak to peak voltage range	0.2	0.5	1.6	V
N_H	Total harmonic content of input signal			-25	dBc
Z_{INRe}	Real part of parallel input impedance at pin	30	60	90	KΩ

Table 8. System clock, digital clock DC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low Level input voltage			0.22 * VDD_IO_A	V
V_{IH}	High Level input voltage	0.85 * VDD_IO_A			V

Table 9. System clock, digital clock AC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{RISE}	10%-90% rise time		1.5	6	ns
T_{FALL}	90%-10% fall time		1,5	6	ns
D_{CYCLE}	Duty Cycle	45	50	55	%

Low power clock specifications

The low power clock pin is powered by connecting VDD_IO_B to the wanted supply.

Table 10. Low power clock specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Duty cycle	30		70	%
	Accuracy	-250		250	ppm

2.5 Current consumption

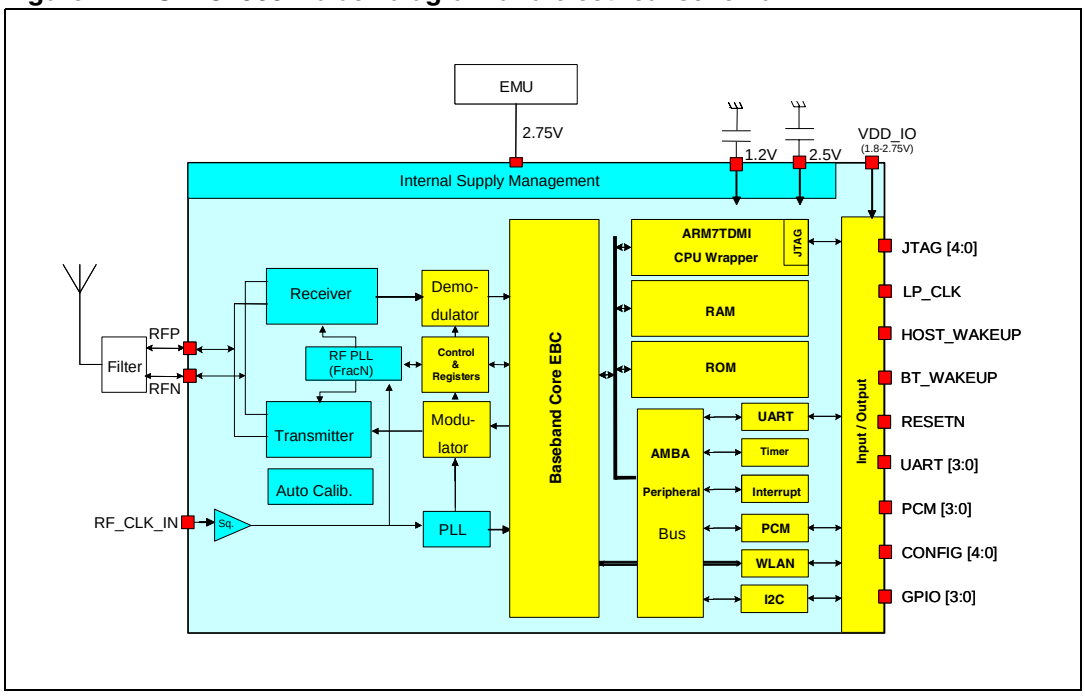
Table 11. Typical current consumption(1)

STLC2500A state	Value	Unit
Complete power down	6	µA
Deep sleep mode	25	µA
Sleep Mode	1.4	mA
Sniff mode (1.28 s, 2 attempts, 0 time outs)	0.056	mA
Page/Inquiry scan (1,28 seconds period), combined with Deep Sleep Mode 2	0.4	mA
Active: audio (HV3)	10.9	mA
Active: data (DH1) (172,8 Kbps symmetrical)	21.8	mA
Active: audio eSCO (EV3), (64 Kbps symmetrical TSCO=6)	11.3	mA
Active: audio eSCO (EV5), (64 Kbps symmetrical TSCO=12)	9.6	mA
Active: audio eSCO (EV5), (64 Kbps symmetrical TSCO=18)	9.1	mA
Active: audio eSCO (EV5), (64 Kbps symmetrical TSCO=24)	8.9	mA
Active: audio eSCO (EV5), (64 Kbps symmetrical TSCO=36)	8.5	mA
Continuous RX, RF sub chip only.	34	mA
Continuous TX, RF sub chip only at 2.5 dBm output power.	32	mA

1. T_{amb} = 25°C, 26 MHz digital clock, 1.8 Volts at I/Os

3 Block diagram

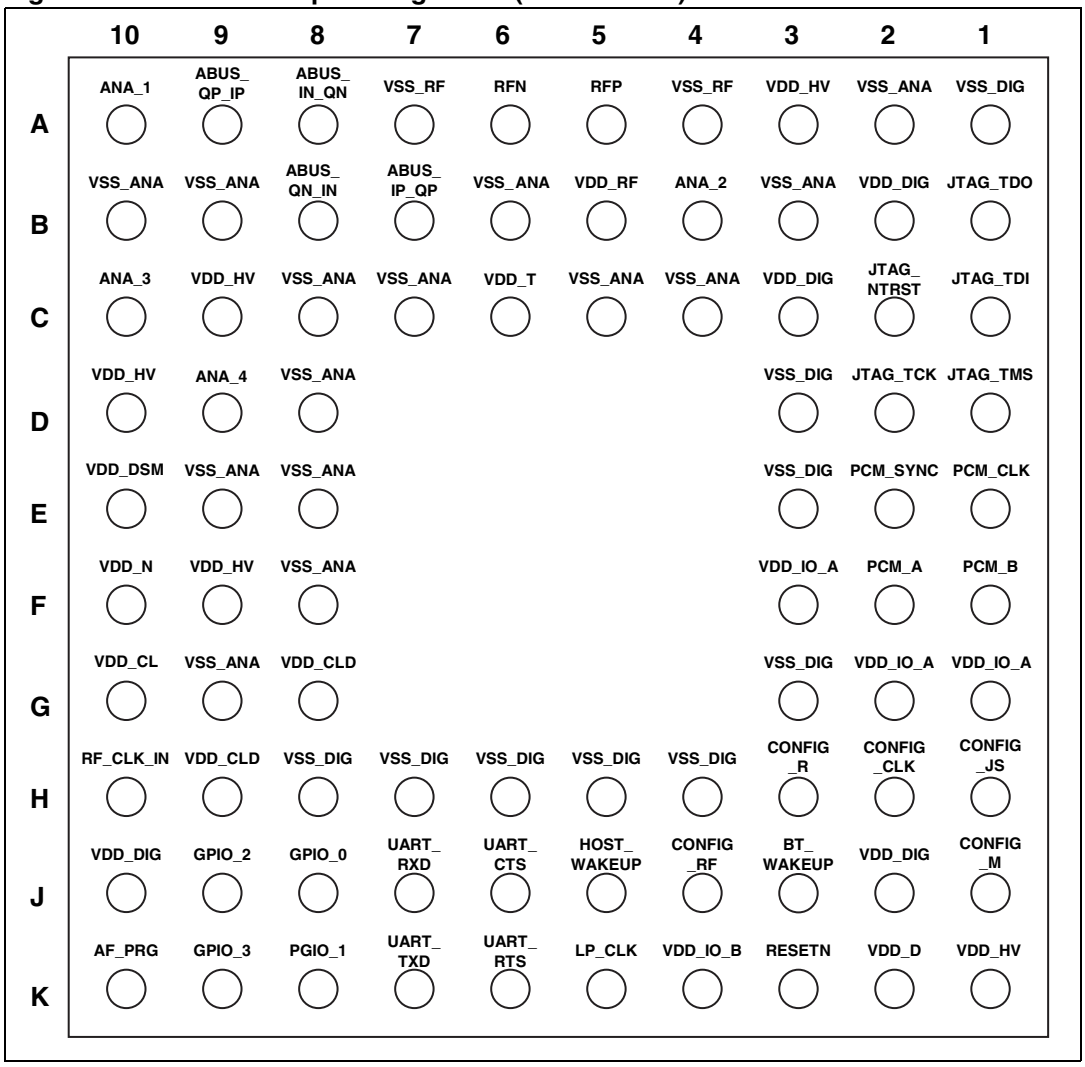
Figure 1. STLC2500A block diagram and electrical schema



4 Pinout

4.1 Pin assignment

Figure 2. STLC2500A pin assignment (bottom view)



4.2 Pin description and assignment

Table 12 shows the pin list of the STLC2500A.The column "PU/PD" shows the pads implementing a pull-down/up. The column "DIR" describes the pin directions:

- I for inputs
- O for outputs
- I/O for input/output
- O/t for tri-state outputs

The column Reset and Default show the state of the pins in reset and the default value after reset. For the output pin the default drive capability is 2 mA.

Table 12. STLC2500A pin list (functional and supply)

Name	Pin #	Description	DIR	Reset	Default after reset	VDD_IO_x
Clock and reset pins						
RESETN	K03	Global reset - active low	I	Input	Input	A
RF_CLK_IN	H10	Reference clock input	I	Input	Input	(1)
LP_CLK	K05	Low power clock input	I	Input	Input	B
SW initiated low power mode						
HOST_WAKEUP	J05	Wake-up signal to host (Open drain output)	I/O	Input PD	Output high	A
BT_WAKEUP	J03	Wake-up signal to Bluetooth	I	Input(2)	Input	A
UART interface						
UART_RXD	J07	UART receive data	I	Input PD	Input	A
UART_TXD	K07	UART transmit data	O/t (I/O)	Tri-state PD	Output high	A
UART_CTS	J06	UART clear to send	I	Input PU (2)	Input	A
UART_RTS	K06	UART Request to send	O/t (I/O)	Tri-state PU	Output low	A
PCM interface						
PCM_SYNC	E02	PCM frame signal	I/O	Input PD	Input PD	A
PCM_CLK	E01	PCM clock signal	I/O	Input PD	Input PD	A
PCM_A	F02	PCM data	I/O	Input PD	Input PD	A
PCM_B	F01	PCM data	I/O	Input PD	Input PD	A
JTAG interface						
JTAG_TDI	C01	JTAG data input	I	Input PU	Input PU	A
JTAG_TDO	B01	JTAG data output	O/t	Tri-state	Tri-state	A
JTAG_TMS	D01	JTAG mode signal	I	Input PU	Input PU	A
JTAG_NTRST	C02	JTAG reset active low	I	Input PD	Input PD	A
JTAG_TCK	D02	JTAG clock input	I	Input(3)	Input	A
General purpose Input/Output pins						
GPIO_0	J08	General purpose IO	I/O	Input PD	Input PD	A
GPIO_1	K08	General purpose IO	I/O	Input PD	Input PD	A
GPIO_2	J09	General purpose IO	I/O	Input PD	Input PD	A
GPIO_3	K09	General purpose IO	I/O	Input PD	Input PD	A

Table 12. STLC2500A pin list (functional and supply)

Name	Pin #	Description	DIR	Reset	Default after reset	VDD_IO_x
Configuration pins						
CONFIG_JS	H01	Configuration signal	I	Input	Input	A
CONFIG_CLK	H02	Configuration signal	I	Input	Input	A
CONFIG_R	H03	Configuration signal	I	Input	Input	A
CONFIG_M	J01	Configuration signal	I	Input	Input	A
CONFIG_RF	J04	Configuration signal	I	Input	Input	A
RF signals						
RFP	A05	Differential RF port	I/O			
RFN	A06		I/O			
Power supply						
VDD_HV	A03	Power supply (Connect all to 2.75V)				
	C09					
	D10					
	F09					
	K01					
VDD_D	K02	Output regulator for core logic (Connect to VDD_DIG)				
VDD_DIG	B02	Core logic supply (Connect all to VDD_D)				
	C03					
	J02					
	J10					
VDD_IO_A	F03	1.65V to 2.85V I/Os supply (Connect all)				
	G02					
	G01					
VDD_IO_B	K04	1.35V to 2.85V I/Os supply				
VDD_CLD	G08	System clock supply 1.65V to 2.85V (Connect all to VDD_IO_A in case of a digital reference clock input, to VSS_ANA in case of an analogue reference clock input)				
	H09					
VDD_DSM	E10	Internal supply decoupling				
VDD_N	F10	Internal supply decoupling				
VDD_CL	G10	Internal supply decoupling				

Table 12. STLC2500A pin list (functional and supply)

Name	Pin #	Description	DIR	Reset	Default after reset	VDD_IO_x
VDD_RF	B05	Internal supply decoupling				
VSS_DIG	A01	Digital ground				
	D03					
	E03					
	G03					
	H04					
	H05					
	H06					
	H07					
	H08					
VSS_ANA	A02	Analogue ground				
	B03					
	B06					
	B09					
	B10					
	C04					
	C05					
	C07					
	C08					
	D08					
	E08					
	E09					
	F08					
	G09					
VSS_RF	A04	RF ground				
	A07					

1. See also pin VDD_CLD in *Table*
2. Should be strapped to VDD_IO_A if not used
3. Should be strapped to VSS_DIG if not used

Table 13. STLC2500A pin list (test)

Name	Pin #	Description	DIR	Reset	Default	V_{DDIO}
Analogue test pin						
VDD_T	C06	Test supply				
ABUS_IN_QN	A08	Test pin	I/O	Input(1)	Input (1)	
ABUS_QP_IP	A09	Test pin	I/O	Input (1)	Input (1)	
ABUS_IP_QP	B07	Test pin	I/O	Input (1)	Input (1)	
ABUS_QN_IN	B08	Test pin	I/O	Input (1)	Input (1)	
ANA_1	A10	Analogue test pin (Leave unconnected)				
ANA_2	B04	Analogue test pin (Leave unconnected)				
ANA_3	C10	Analogue test pin (Leave unconnected)				
ANA_4	D09	Analogue test pin (Leave unconnected)				
AF_PRG	K10	Test pin (Leave unconnected)	I/O	Open	Open	

1. To be strapped to VSS_ANA

Configuration pins

The configuration pins are used to select different modes of operation for the chip:

Table 14. STLC2500A configuration pins

Configuration	Description
Digital or analogue incoming system clock	
CONFIG_CLK =’1’	The incoming system clock is a digital square signal. (See *Section 2.4*)
CONFIG_CLK =’0’	The incoming system clock is a sine wave signal. (See *Section 2.4*)
Initiated deep sleep modes	
CONFIG_JS =’0’ AND CONFIG_M = ‘0’	Reserved
CONFIG_JS =’0’ AND CONFIG_M = ‘1’	Initiated Deep Sleep, mode 1. (See *Section 6.8*)
CONFIG_JS =’1’ AND CONFIG_M = ‘0’	Initiated Deep Sleep, mode 2. (See *Section 6.8*)
CONFIG_JS =’1’ AND CONFIG_M = ‘1’	Reserved

Where '1' means VDD_IO_A and '0' means VSS_DIG.

The other two configuration pins, CONFIG_RF and CONFIG_R have to be strapped to VSS_DIG.

5 Functional description

5.1 Transmitter

The transmitter uses the serial transmit data from the Bluetooth Controller. The transmitter modulator converts this data into GFSK modulated I and Q digital signals. These signals are then converted to analogue signals that are low pass filtered before up-conversion. The carrier frequency drift is limited by a closed loop PLL.

5.2 Receiver

The STLC2500A implements a low-IF receiver for Bluetooth modulated input signals. The radio signal is taken from a balanced RF input and amplified by an LNA. The mixers are driven by two quadrature LO signals, which are locally generated from a VCO signal running at twice the frequency. The I and Q mixer output signals are band pass filtered by a poly-phase filter for channel filtering and image rejection. The output of the band pass filter is amplified by a VGA to the optimal input range for the A/D converter. Further channel filtering is done in the digital part. The digital part demodulates the GFSK coded bit stream by evaluating the phase information in the digital I and Q signals. RSSI data is extracted. Overall automatic gain amplification in the receive path is controlled digitally. The RC time constants for the analogue filters are automatically calibrated on chip.

5.3 PLL

The on-chip VCO is part of a PLL. The tank resonator circuitry for the VCO is completely integrated without need of external components. Variations in the VCO centre frequency are calibrated out automatically.

5.4 Bluetooth controller 1.1 features

The Bluetooth Controller is based on Ericsson Technology Licensing Baseband Core (EBC) and it is compliant with the Bluetooth specification 1.1:

- Point to multipoint (up to 7 Slaves)
- Asynchronous Connection Less (ACL) link support giving data rates up to 721 kbps
- Synchronous Connection Oriented (SCO) link with support for 2 voice channels over the air interface
- Flexible voice format to Host and over the air (CVSD, PCM 13/16 bits, A-law, µ-law)
- HW support for packet types: DM1, 3, 5; DH1, 3, 5; HV1, 3; DV
- Scatternet capabilities (Master in one piconet and Slave in the other one; Slave in two piconets). All scatternet v.1.1 errata supported
- Ciphering support up to 128 bits key
- Paging modes R0, R1, R2
- Channel Quality Driven Data Rate
- Full Bluetooth software stack available
- Low-level link controller
- Fully v.1.1 compatible via restricted mode (e.g.: add_SCO_connection, read_local_supported_features, read_country_code)

5.5 Bluetooth controller 1.2 features

The Bluetooth Controller is also compliant with the Bluetooth specification 1.2:

- Adaptive Frequency Hopping (AFH): hopping kernel, channel assessment as Master and as Slave
- Faster connection: Interlaced scan for Page and Inquiry scan, answer FHS at first reception, RSSI used to limit range
- Extended SCO (eSCO) links: supports EV3 and EV5 packets
- QoS Flush
- Synchronization: BT clocks are available at HCI level for synchronization of parallel applications on different slaves
- L2CAP Flow & Error control
- LMP improvements
- LMP SCO handling
- Parameter ranges update

5.5.1 V1.2 detailed functionality - Extended SCO

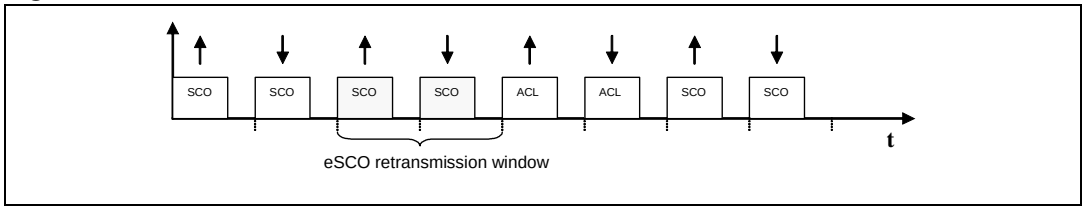
- User Perspective - Extended SCO

This function gives improved voice quality since it enables the possibility to retransmit lost or corrupted voice packets in both directions.

- Technical perspective - Extended SCO

eSCO incorporates CRC, negotiable data rate, negotiable retransmission window and multi-slot packets. Retransmission of lost or corrupted packets during the retransmission window guarantees on-time delivery.

Figure 3. eSCO



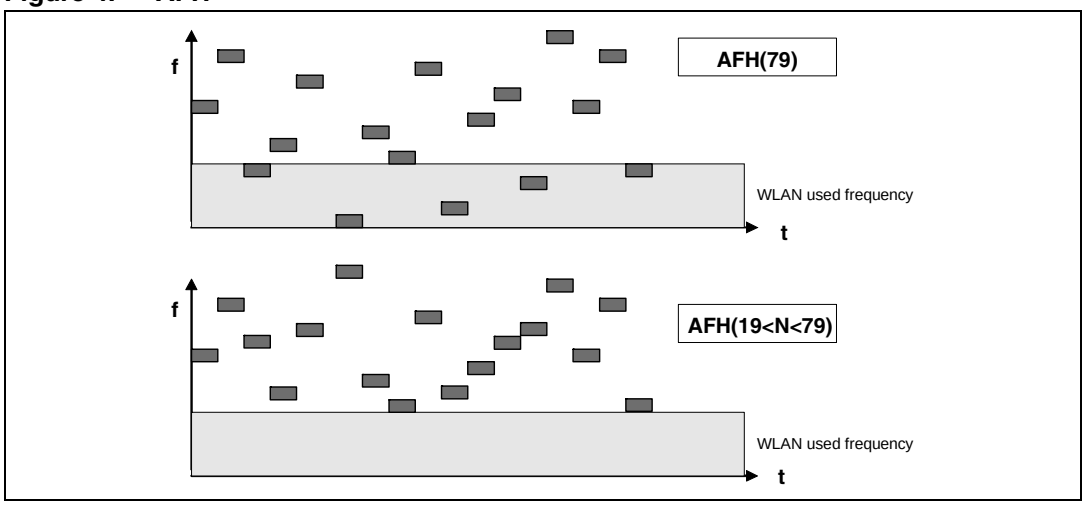
5.5.2 V1.2 detailed functionality - Adaptive Frequency Hopping

- User Perspective - Adaptive Frequency Hopping

In the Bluetooth spec 1.1, the Bluetooth devices hop in the 2.4 GHz band over 79-channels. As WLAN 802.11 has become popular, there are improvements in the Bluetooth spec 1.2 specifying how Bluetooth units can avoid jammed bands and provide an improved co-existence with WLAN.

- Technical perspective - Adaptive Frequency Hopping

Figure 4. AFH



First the Master and/or the Slaves identify the jammed channels. The Master decides on the channel distribution and informs the involved slaves. The Master and the Slaves, at a predefined instant, switch to the new channel distribution scheme.

No longer jammed channels are re-inserted into the channel distribution scheme. AFH uses the same hop frequency for transmission as for reception.

5.5.3 V1.2 detailed functionality - Faster connection

- User perspective - Faster connection

This feature gives the User about 65% faster connection on average when enabled compared to Bluetooth spec 1.1 connection procedure.

- Technical perspective - Faster connection

The Faster Inquiry Functionality is based on a removed/shortened random back off and also a new Interlaced Inquiry Scan scheme.

The Faster Page functionality is based on Interlaced Page Scan.

5.5.4 V1.2 detailed functionality - Quality of service

- User perspective - Quality of service

Small changes to the BT1.1 spec regarding Quality of Service make a large difference.

Allowing all QoS parameters to be communicated over HCI to the link manager enables efficient bandwidth management.

Here after a short list of user perspectives:

1. **Flush timeout** enables time-bounded traffic such as video streaming to become more robust when the channel degrades. It sets the maximum delay of an L2CAP frame. It does not enable multiple streams in one piconet, or heavy data transfer at the same time.
2. **Simple latency control** allows the Host to set the poll interval. This provides support for HID devices mixed with other traffic in the piconet.

5.6 Processor and memory

- ARM7TDMI
- On chip RAM, including provision for patches
- On chip ROM, preloaded with SW up to HCI

6 General specification

All the provided values are specified over the operational conditions (VDD and temperature) according to the Bluetooth 1.1 and 1.2 specifications unless otherwise specified.

6.1 Receiver

To be compliant with the Bluetooth norm, an external RF filter is required to provide minimum -17dB of attenuation in the band: 30MHz - 2000MHz and 3000MHz - 12.75GHz. All specifications below are given at pin level and over temperature unless otherwise specified.

Table 15. Receiver parameters(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
RFin	Input frequency range		2402		2480	MHz
RXsens	Receiver Sensitivity (Clean transmitter)	@ BER 0.1%		-85		dBm
RXmax	Maximum useable input signal level	@ BER 0.1%		+15		dBm
Receiver interferer performance @BER 0.1%						
$C/I_{co\text{-}channel}$	Co-channel interference	@ Input signal strength = -60dBm			9	dB
C/I_{1MHz}	Adjacent (±1MHz) interference	@ Input signal strength = -60dBm			-2	dB
C/I_{+2MHz}	Adjacent (+2MHz) interference	@ Input signal strength = -60dBm		-35		dB
C/I_{-2MHz}	Adjacent (-2MHz) interference	@ Input signal strength = -67dBm		-25		dB
C/I_{+3MHz}	Adjacent (+3MHz) interference	@ Input signal strength = -67dBm		-44		dB
C/I_{-3MHz}	Adjacent (-3MHz) interference	@ Input signal strength = -67dBm		-37		dB
$C/I_{\geq 4MHz}$	Adjacent (≥±4MHz) interference	@ Input signal strength = -67dBm		-46		dB
Receiver inter-modulation						
IMD	Inter-modulation	Measured as defined in BT test specification.		-35		dBm

1. T_{amb} = 25°C, VDD_HV = 2.75V, parameters are given at device pin.

6.2 Transmitter

All output power specifications are given at the pin level and over temperature range unless otherwise specified.

Table 16. Transmitter parameters(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
RFout	Output frequency range		2402		2480	MHz
TXpout	Nominal Output power	@2402-2480 MHz	0	3	5	dBm
In-band spurious emission						
FCC	FCC's 20 dB BW			932		kHz
TX_SE2	Channel offset=2			-51		dBm
TX_SE3	Channel offset=3			-55		dBm
TX_SE4	Channel offset≥4 (except 13)			-57		dBm
Initial carrier frequency tolerance (for an exact reference)						
ΔF	|f_TX-f0|		-75		75	kHz
Carrier Frequency Drift						
|Δf_p1|	One slot packet				25	kHz
|Δf_p3|	Three slots packet				40	kHz
|Δf_p5|	Five slots packet				40	kHz
Carrier Frequency Drift rate						
|Δf/50us|	Frequency drift rate				20	kHz/µs

1. T_{amb} = 25°C, VDD_HV = 2.75V, parameters are given at device pin.

6.3 System clock

The STLC2500A works with a single clock (sine wave or digital) provided on the RF_CLK_IN pin. Precision of this clock should be 20 ppm. The external STLC2500A clock could be 13 or 26 MHz (for GSM application), 19.2 MHz and 38.4 MHz (for 2.5 & 3G & CDMA platforms).

6.4 Low power clock

The low power clock is used by the Bluetooth Controller as reference clock during the low power modes. It requires an accuracy of 250ppm. The external STLC2500A clock, provided on the LP_CLK digital pin could be 3.2 kHz, 16.384 kHz, 32 kHz and 32.768 kHz.

After power-up, the low power clock must be available before the reset is released. It must remain active all the time until the chip is powered off.

6.5 Clock detection

The system and low power clocks can be selected by specific HCI commands (16.384 KHz or 32 KHz) or by an integrated automatic detection algorithm.

The clock detection routine steps are:

- Identification of the system clock frequency (13 MHz, 26MHz, 19.2 MHz or 38.4 MHz)
- Identification of the low power clock (3.2 KHz or 32.768 KHz)

6.6 Interrupts

The user can program the GPIOs as external interrupt sources.

6.7 Low power modes

To save power, three low power modes are supported as described in table 18.

Depending of the Bluetooth and of the Host's activity, the STLC2500A decides to use sleep mode or deep sleep mode.

Complete power down is entered only after an explicit command from the Host.

Table 17. Low power modes

Low power modes	Description
Sleep mode	The STLC2500A: – Accepts HCI commands from the Host. – Supports all types of Bluetooth links. – Can transfer data over Bluetooth links. – Dynamically switches between sleep and active mode when needed. – The system clock is still active in part of the design. – Parts of the chip can be dynamically powered off depending on the Bluetooth activity.

Table 17. Low power modes

Low power modes	Description
Deep sleep mode	The STLC2500A: – Does not accept HCI commands from the Host. – Supports page- and inquiry scans. – Supports Bluetooth links that are in Sniff, Hold or Park. – Does not transfer data over Bluetooth links. – Dynamically switches between deep sleep and active mode during Bluetooth activity. – The system clock is not active in any part of the design. – Parts of the chip can be dynamically powered off depending on the Bluetooth activity.
Complete power down	The STLC2500A is effectively powered down: – No Bluetooth activity is supported. – The HCI interface is shut down. – The system clock is not active in any part of the design. – Most parts of the chip are completely powered off. – RAM content is not maintained (initialisation is required at wakeup).

The following sections describe examples for the usage of the low power modes.

6.7.1 SNIFF or PARK

The STLC2500A is in active mode with a Bluetooth connection. Once the transmission is concluded, SNIFF or PARK is programmed. When one of these two states is entered, the STLC2500A goes into Sleep Mode. After that, the Host may decide to place the STLC2500A in Deep Sleep Mode as described in *Section 6.8*. The Deep Sleep Mode allows for lower power consumption. When the STLC2500A needs to send or receive a packet (e.g. at TSNIFF or at the beacon instant), it requires the system clock and enters active mode for the needed transmission/reception. Immediately afterwards, it will go back to Deep Sleep Mode. If some HCI transmission is needed, the UART link will be reactivated, using one of the two ways explained in *Section 6.8*, and the STLC2500A will move from Deep Sleep Mode to Sleep Mode.

6.7.2 Inquiry/Page scan

When only inquiry scan or page scan is enabled, the STLC2500A will go in Sleep Mode or Deep Sleep Mode outside the receiver activity. The selection between Sleep Mode and Deep Sleep Mode depends on the UART activity like in SNIFF or PARK.

6.7.3 No connection

If the Host allows Deep Sleep Mode (as described in section 7.8) and there is no activity, then the STLC2500A is placed in Deep Sleep Mode. In this mode (no connection), the Host can also decide to put the STLC2500A in Complete Power Down to further reduce the power consumption. In this case some part of the STLC2500A will be completely powered off. It's possible to exit the Deep Sleep Mode by using one of the two methods explained in *Section 6.8*. The request to quit the Complete Power Down is done either by using the same methods as to exit Deep Sleep Mode, either with an HW reset, e.g. triggered by the Host.

6.7.4 Active link

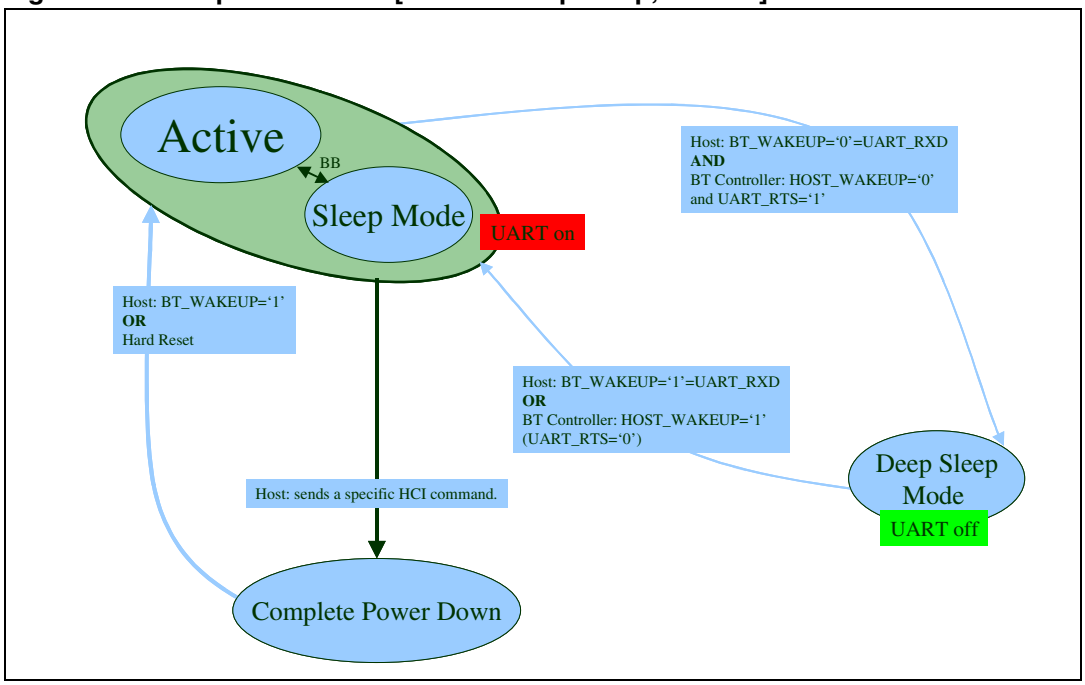
When there is an active link ((e)SCO or ACL), the Bluetooth Controller will not go in Deep Sleep Mode and not in Complete Power Down. But the Bluetooth Controller is made in such a way that whenever it is possible, depending on the scheduled activity (number of link, type of link, amount of data exchanged), it goes in Sleep Mode.

6.8 Initiated deep sleep modes

During periods of no activity on the Bluetooth and on the Host side, the chip can be placed in Deep Sleep Mode. Two modes to initiate deep sleep mode and to wake up are supported (selection is done through pin configuration, see *Table 14*):

1. **[Initiated Deep Sleep, mode 1]**
   It requires HOST_WAKEUP, UART_RXD (connected with BT_WAKEUP, the two paths will be physically connected on the board) and UART_RTS. The UART_RXD is used as wakeup signal from the host, the HOST_WAKEUP requires the clock from the Host and the UART_RTS indicates when the Bluetooth Controller is available. In this mode, the break function (UART_RXD is low for more than 1 word) is used to distinguish between normal operation and low power mode usage.
   - The system goes in low power mode in this way:
     the Host tells the Bluetooth Controller that it can go in low power by forcing the UART_RXD of the Bluetooth Controller to '0' for more than 1 word. The Bluetooth Controller decides to go in low power mode, or not, depending on its scheduled activity. In case it decides to go in low power mode, it signals it by forcing UART_RTS high; then it asserts HOST_WAKEUP low to tell the Host that it does not need the clock anymore. The Bluetooth Controller cannot go in Deep Sleep Mode by itself. This is a logical consequence of the fact that the system clock is needed to receive characters on the UART and only the Host can stop the UART link.
   - The system wakes up in this way:
     the Bluetooth Controller first asks the Host to restart the system clock by setting HOST_WAKEUP to '1'. When the clock is available, the Bluetooth Controller sets UART_RTS low, and then the Host can give confirmation by releasing the UART_RXD of the Bluetooth Controller. In case the Host wants to wake up the Bluetooth Controller, it sets the UART_RXD pin of the Bluetooth Controller to '1'. The Bluetooth Controller confirms it is awake by releasing UART_RTS to '0'.

Figure 5. Low power modes [Initiated deep sleep, mode 1]



2. **[Initiated Deep Sleep, mode 2]**
In this mode, the clock request and the host wake-up signalling have been decoupled. These functions are now covered by 2 independant signals: the HOST_WAKEUP pin only covers the clock request functionality, GPIO3 is used as a wakeup signal to the Host.
This mode uses the following signals: HOST_WAKEUP (only used as a clock request signal), BT_WAKEUP and GPIO3 (used as host wakeup signal). UART_RTS, UART_CTS are only used to stop/allow UART activity.

   – The Host wakeup procedure
   A Bluetooth Controller initiated wakeup of the Host is always initiated by GPIO3. GPIO3 signals whether the Bluetooth Controller needs the Hosts attention: only if there are data or HCI events to be sent over the UART interface, the Bluetooth Controller will assert GPIO3 (requesting the Hosts attention).
   When the Host sees a high level on GPIO3, it must wakeup (when asleep) and assert the UART_CTS signal, allowing the Bluetooth Controller to send data or HCI events. When asserting GPIO3, the Bluetooth Controller will make sure the UART is open and that the UART_RTS signal is asserted.
   Note that the UART will be closed (and the UART_RTS will be deasserted) by the Bluetooth Controller when BT_WAKEUP is low and there is no data to be sent to the Host. In that case, GPIO3 will also be low.

   – The wakeup/fall-asleep procedures for the Bluetooth Controller.
   The wakeup/fall-asleep procedures for the Bluetooth Controller are always initiated by the HOST_WAKEUP (i.e.clock request) or BT_WAKEUP signal.

   – *The system goes into low power as follows:*
   the Host sets BT_WAKEUP to '0', telling the Bluetooth Controller that it can go in low power. The Bluetooth Controller decides to enter low power mode or not, depending on its scheduled activity and on the number of events or data packets to be sent to the Host. When it decides to enter low power mode (meaning that there is no scheduled activity and that there are no data or HCI events to be sent -

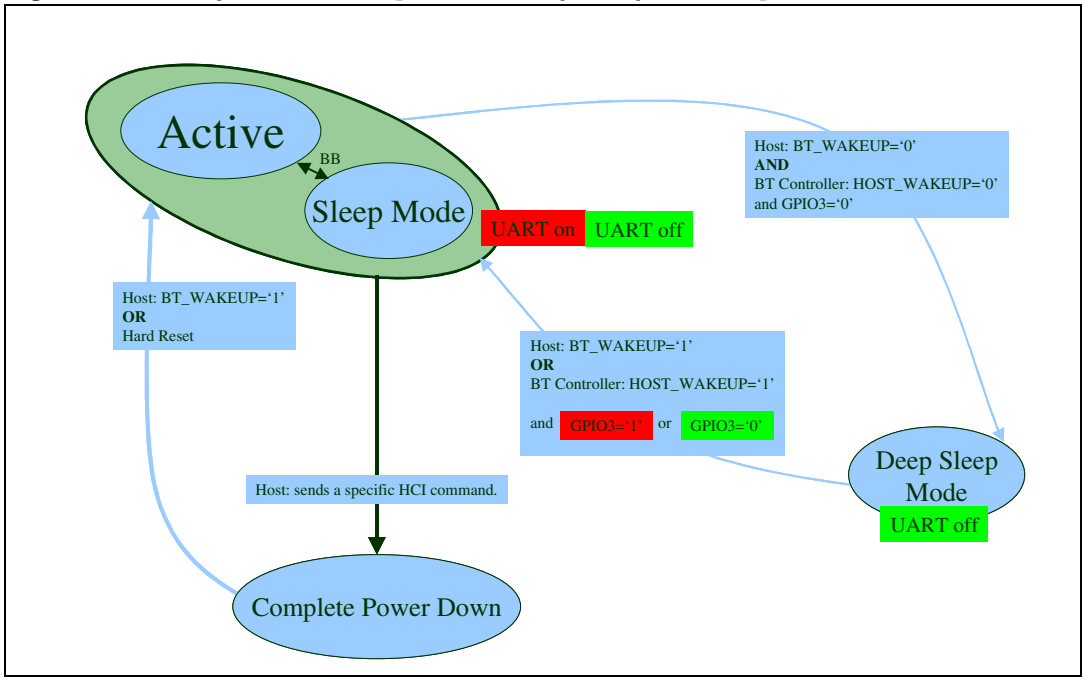
i.e. GPIO3 is low) it sets HOST_WAKEUP to '0', telling the Host that the system clock is not needed any more.

Note: Note that in this case, the UART will be closed (as described above).

– An autonomous wakeup (i.e. initiated by the Bluetooth Controller) goes as follows: the Bluetooth Controller sets the HOST_WAKEUP signal to '1' to request the system clock. Initially, GPIO3 is unaffected. GPIO3 will only be asserted when and if there are data or HCI events to be sent. In that case the UART will be opened (and UART_RTS will be asserted).

– Wakeup initiated by the Host:
the Hosts sets BT_WAKEUP to '1'. The Bluetooth Controller then asserts the HOST_WAKEUP signal to request the system clock. The Bluetooth Controller will also open the UART (and assert UART_RTS). Initially, GPIO3 is unaffected. GPIO3 will only be asserted when and if there are data or HCI events to be sent.

Figure 6. Low power modes [Initiated deep sleep, mode 2]



6.9 Patch RAM

The STLC2500A includes a HW block that allows patching of the ROM code.

Additionally, a SW patch mechanism allows replacing complete SW functions without changing the ROM image.

A part of the RAM memory is used for HW and SW patches.

6.10 Download of SW parameters

To change the device configuration a set of customizable parameters have been defined and put together in one file. This file is downloaded at start-up into the STLC2500A.

Examples of parameters are: radio configuration, PCM settings etc.

The same HCI command is used to download the file containing the patches (both those for the SW and HW mechanism).

A more detailed description of the SW parameters is available upon request.

6.11 Bluetooth - WLAN coexistence in collocated scenario

The coexistence interface uses up to 4 GPIO pins, the unused ones can be used as GPIOs.

Bluetooth and WLAN 802.11 b/g technologies occupy the same 2.4 GHz ISM band. STLC2500A implements a set of mechanisms to avoid interference in a collocated scenario.

The STLC2500A supports 5 different algorithms in order to provide efficient and flexible simultaneous functionality between the two technologies in collocated scenarios:

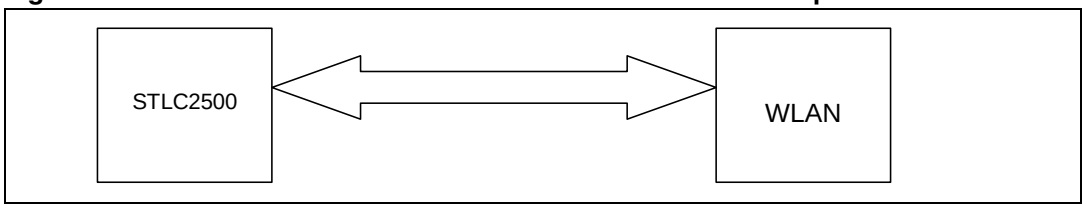
- **Algorithm 1:** PTA (Packet Traffic Arbitration) based coexistence algorithm defined in accordance with the IEEE 802.15.2 recommended practice.
- **Algorithm 2:** the WLAN is the master and it indicates to the STLC2500A when not to operate in case of simultaneous use of the air interface.
- **Algorithm 3:** the STLC2500A is the master and it indicates to the WLAN chip when not to operate in case of simultaneous use of the air interface.
- **Algorithm 4:** Two-wire mechanism
- **Algorithm 5:** Alternating Wireless Medium Access (AWMA), defined in accordance with the WLAN 802.11 b/g technologies.

The algorithm is selected via HCI command. The default algorithm is algorithm 1.

6.11.1 Algorithm 1: PTA (Packet Traffic Arbitration)

The Algorithm is based on a bus connection between the STLC2500A and the WLAN chip.

Figure 7. Bus connection between STLC2500A and WLAN chip



By using this coexistence interface it is possible to dynamically allocate bandwidth to the two devices when simultaneous operations are required while the full bandwidth can be allocated to one of them in case the other one does not require activity. The algorithm involves a priority mechanism, which allows preserving the quality of certain types of link. A typical application would be to guarantee optimal quality to the Bluetooth voice communication while an intensive WLAN communication is ongoing.

Several algorithms have been implemented in order to provide a maximum of flexibility and efficiency for the priority handling. Those algorithms can be activated via specific HCI commands.

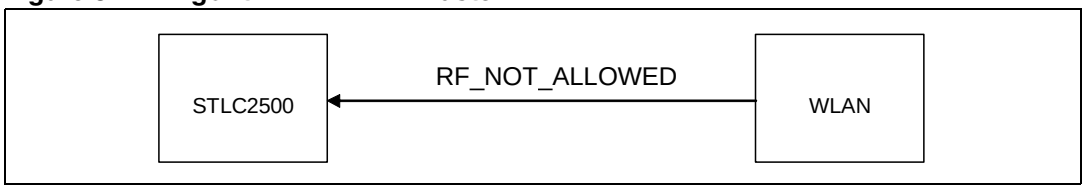
The combination of a time division multiplexing techniques to share the bandwidth in case of simultaneous operations and of the priority mechanism avoid the interference due to packet

collision and it allows the maximization of the 2.4 GHz ISM bandwidth usage for both devices while preserving the quality of some critical types of link.

6.11.2 Algorithm 2: WLAN master

In case the STLC2500A has to cooperate in a collocated scenario with a WLAN chip that does not support a PTA based algorithm, a simpler mechanism can be put in place. The interface is reduced to 1 line.

Figure 8. ALgorithm 2: WLAN master



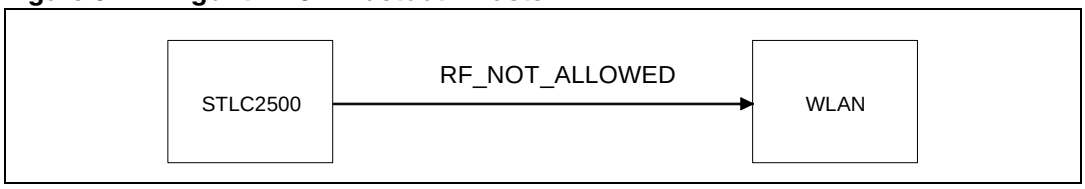
When the WLAN has to operate, it alerts HIGH the RF_NOT_ALLOWED signal and the STLC2500A will not operate while this signals stays HIGH.

This mechanism permits to avoid packet collision in order to make an efficient use of the bandwidth but cannot provide guaranteed quality over the Bluetooth links.

6.11.3 Algorithm 3: Bluetooth master

This algorithm represents the symmetrical case of *Section 6.11.2*. Also in this case the interface is reduced to 1 line.

Figure 9. ALgorithm 3 - Bluetooth master



When the STLC2500A has to operate it alerts HIGH the RF_NOT_ALLOWED signal and the WLAN will not operate while this signals stays HIGH.

This mechanism permits to avoid packet collision in order to make an efficient use of the bandwidth, it provides high quality for all Bluetooth links but cannot provide guaranteed quality over the WLAN links.

6.11.4 Algorithm 4: Two-wire mechanism

Based on algorithm 2 and 3, the Host decides, on a case-by-case basis, whether WLAN or Bluetooth is master.

6.11.5 Algorithm 5: Alternating Wireless Medium Access (AWMA)

AWMA utilizes a portion of the WLAN beacon interval for Bluetooth operations. From a timing perspective, the medium assignment alternates between usage following WLAN procedures and usage following Bluetooth procedures.
The timing synchronization between the WLAN and the STLC2500A is done by the HW signal MEDIUM_FREE.

Table 18. WLAN HW signal assignment

WLAN[1]	Scenario 1: PTA	Scenario 2: WLAN master	Scenario 3: BT master	Scenario 4: 2-wire	Scenario 5: AWMA
WLAN 1	TX_ CONFIRM	BT_RF_NOT_ ALLOWED	Not used	BT_RF_NOT_ ALLOWED	MEDIUM_ FREE
WLAN 2	TX_ REQUEST	Not used	WLAN_RF_ NOT_ ALLOWED	WLAN_RF_ NOT_ ALLOWED	Not used
WLAN 3	STATUS	Not used	Not used	Not used	Not used
WLAN 4	OPTIONAL_ SIGNAL	Not used	Not used	Not used	Not used

1. See also *Table 22*

7 Digital interfaces

7.1 The UART interface

The STLC2500A contains a 4-pin (UART_RXD, UART_TXD, UART_RTS, and UART_CTS) UART compatible with 16450, 16550 and 16750 standards. It is running up to 1842 kbps (+1.5%/-1%).

The configuration is 8 data bits, 1 start bit, 1 stop bit, and no parity bit. 128-byte FIFO with configurable threshold interrupts for low CPU load and high throughput. Auto RTS/CTS is implemented in HW, controllable by SW.

The UART accepts all HCI commands as described in the Bluetooth specification, it supports H4 proprietary commands and the 4-wire UART sleep mode. The complete list of supported proprietary HCI commands is available in the STLC2500A Software Interface document.

Table 19 contains the list of supported baud rates selectable by HCI commands. The default baud rate is 115200 [bps].

Table 19. List of supported baud rates

Baud rate	Baud rate (contined)	Baud rate (contined)
1842 k	57.6 k	4800
921.6 k	38.4 k	2400
460.8 k	28.8 k	1800
230.4 k	19.2 k	1200
153.6 k	14.4 k	900
115.2 k (default)	9600	600
76.8 k	7200	300

7.2 The PCM interface

The chip contains a 4-pin (PCM_CLK, PCM_SYNC, PCM_A, and PCM_B) direct voice interface to connect to standard CODEC including internal decimator and interpolator filters. The implementation is compliant with the MP-PCM requirements for voice transfer (8 kHz PCM_SYNC and 8 or 16 bits data).

The four signals of the PCM interface are:

- PCM_CLK: PCM clock
- PCM_SYNC: PCM 8 kHz sync (every 125 µs)
- PCM_A: PCM data
- PCM_B: PCM data

The data can be linear PCM (13-16 bit), µ-Law (8 bit) or A-Law (8bit). The interface can be programmed as Master or as Slave via specific HCI commands.

Two additional PCM_SYNC signals can be provided via the GPIOs. See *Section 7.4* for more details.

Figure 10. PCM (A-law, μ-law) standard mode

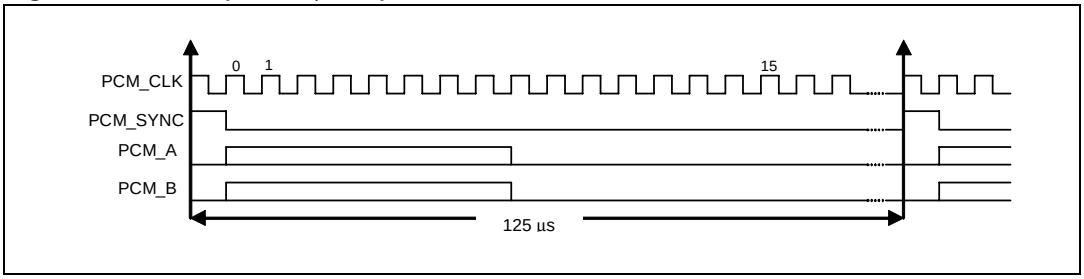


Figure 11. Linear mode

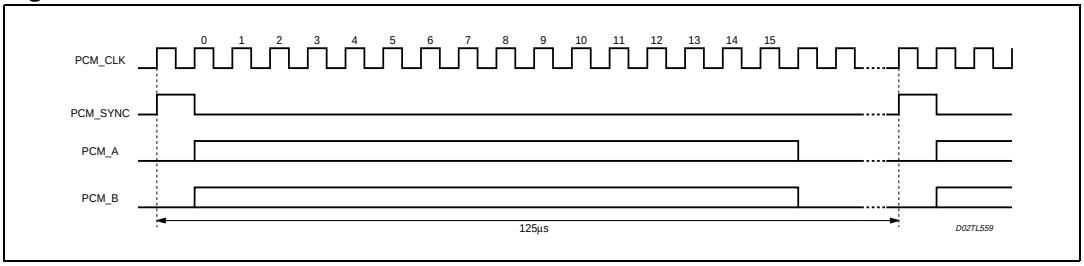
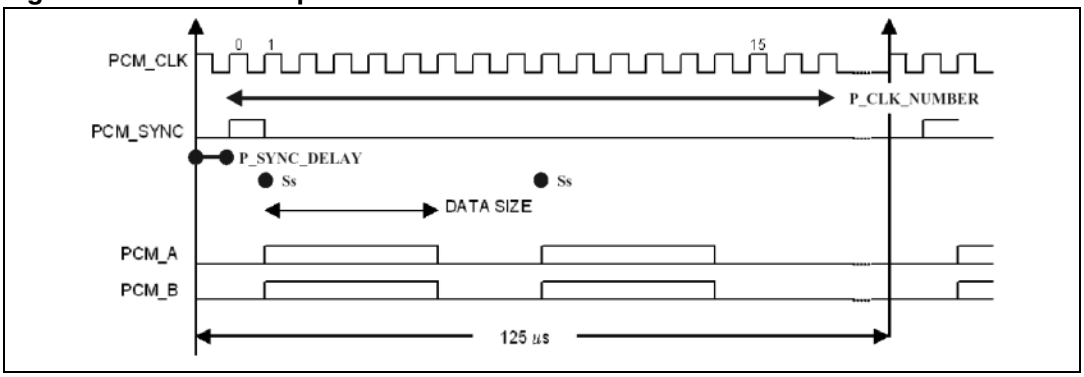


Figure 12. Multi-slot operation



The PCM implementation supports from 1 up to 3 slots per frame with the following parameters:

Table 20. PCM interface parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
PCM interfaces					
F_{PCM_CLK}	Frequency of PCM_CLK	140 (1)	2048	4000	kHz
F_{PCM_SYNC}	Frequency of PCM_SYNC		8		kHz
P_{sync_delay}	Delay of the starting of the first slot	0		255	cycles
P_{clk_number}	PCM_CLK is available during this number of clock cycles	0		255	cycles

Table 20. PCM interface parameters

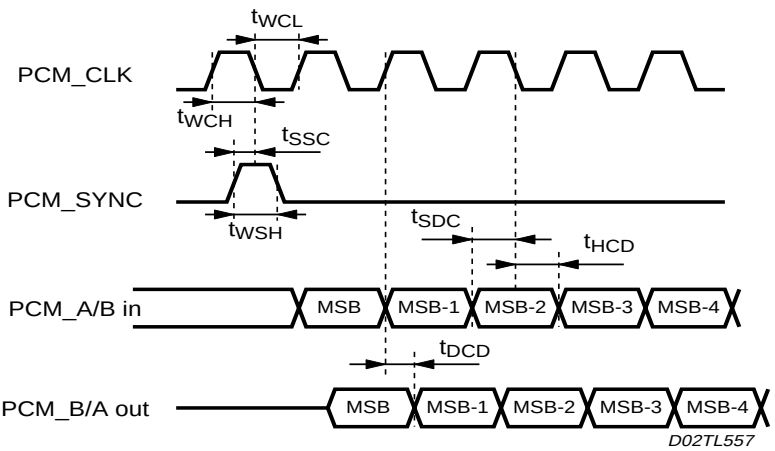
Symbol	Parameter	Min.	Typ.	Max.	Unit
S_s	Slot start (programmable for every slot)	0		255	cycles
D	Data size	8		16	bit
N	Number of slots per frame	1		3	

1. In master mode, the minimum frequency is 2 MHz

Table 21. PCM interface timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WCH}	High period of PCM_CLK	200			ns
t_{WCL}	Low period of PCM_CLK	200			ns
t_{WSH}	High period of PCM_SYNC	200			ns
t_{SSC}	Setup time, PCM_SYNC high to PCM_CLK low	100			ns
t_{SDC}	Setup time, PCM_A/B input valid to PCM_CLK low	100			ns
t_{HCD}	Hold time, PCM_CLK low to PCM_A/B input valid	100			ns
t_{DCD}	Delay time, PCM_CLK high to PCM_A/B output valid			150	ns

Figure 13. PCM interface timing



7.3 JTAG interface

The JTAG interface is compliant with the JTAG IEEE Standard 1149.1. It allows both the boundary scan of the digital pins and the debug of the ARM7TDMI application when connected with the standard ARM7 developments tools. It is also used for the industrial test of the device.

7.4 GPIOs

The STLC2500A has 4 GPIO pins. They are fully programmable via specific HCI commands. They can be configured as input, output, interrupt with asynchronous or synchronous edge or level detection and/or wake-up.

Also other functions are multiplexed on the GPIO pins.

The alternative functions are:

- WLAN co-existence control
- I2C interface
- PCM synchronization
- GPIOs

Some functions are mutually exclusive, as per *Table 22*.

Table 22. GPIO multiplexing - Multiplexed GPIOs

WLAN(1)	I2C	PCM	Order 1 (Order 2)
WLAN 1	I2C clock	[I2C or GPIO]	GPIO 0 (GPIO 3)
WLAN 2	I2C data	[I2C or GPIO]	GPIO 1 (GPIO 2)
WLAN 3	[PCM or GPIO]	PCM sync 1	GPIO 2 (GPIO 1)
WLAN 4	[PCM or GPIO]	PCM sync 2	GPIO 3 (GPIO 0)

1. See also *Table 18*

7.5 I2C interface

The I2C interface is used to access I2C peripherals.

The interface is a fast master I2C; it has full control of the interface at all times. I2C slave functionality is not supported.

8 HCI UART transport layer

The UART transport Layer has been specified by the Bluetooth SIG and allows HCI level communication between a Bluetooth Controller (STLC2500A) and a Host (e.g. a GSM), via a serial line.

The objective of this HCI UART Transport Layer is to make possible to use Bluetooth HCI over a serial interface between two UARTs on the same PCB. The HCI UART Transport Layer assumes that the UART communication is free from line errors.

UART Settings

The HCI UART Transport Layer uses the following settings for RS232:

- Baud rate: configurable (default baud rate 115.2 [kbps])
- Number of data bits: 8
- Parity bit: no parity
- Stop bit: 1 stop bit
- Flow control: RTS/CTS
- Flow-off response time: 3ms

The flow-off response time defines the maximum time from setting RTS low until the byte flow actually stops.

RTS/CTS flow control is used to prevent temporary UART buffer overrun between the Bluetooth Controller and the Host.
It should not be used for flow control of HCI, as HCI has its own flow control mechanism for commands, events and data.

The RS232 signals should be connected in a null-modem fashion, i.e. the Bluetooth Controller TXD output should be connected to the Host RXD input and the Bluetooth Controller RTS output should be connected to the Host CTS input and vice versa.

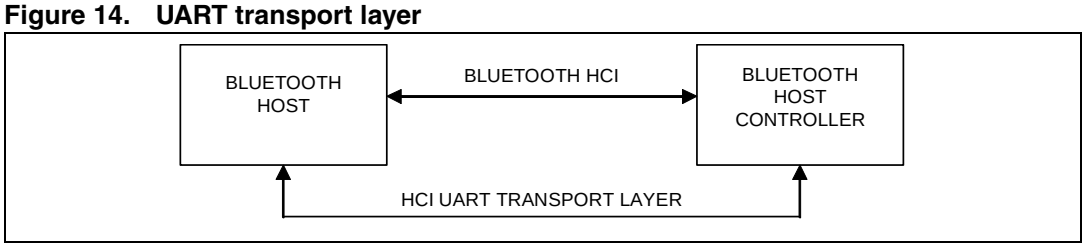
If the Bluetooth Controller RTS output (connected to the Host CTS input) is high, then the Host is allowed to send.

If the Bluetooth Controller RTS output (connected to the Host CTS input) is low, then the Host is not allowed to send.

If the Bluetooth Controller CTS input (connected to the Host RTS output) is high, then the Bluetooth Controller is allowed to send.

If the Bluetooth Controller CTS input (connected to the Host RTS output) is low, then the Bluetooth Controller is not allowed to send.

Figure 14. UART transport layer

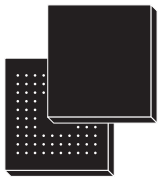


9 Package machanical data

Figure 15. TFBGA84 mechanical data & package dimensions

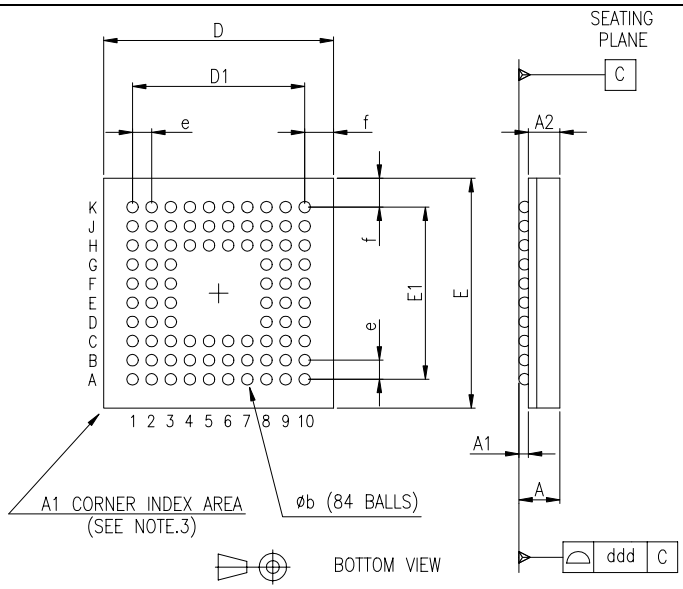
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.010		1.200	0.040		0.047
A1	0.150			0.006		
A2		0.820			0.032	
b	0.250	0.300	0.350	0.010	0.012	0.014
D	5.750	6.000	6.150	0.226	0.236	0.242
D1		4.500			0.177	
E	5.750	6.000	6.150	0.226	0.236	0.242
E1		4.500			0.177	
e	0.450	0.500	0.550	0.018	0.020	0.022
f	0.600	0.750	0.900	0.024	0.029	0.035
ddd			0.080			0.003

OUTLINE AND MECHANICAL DATA



Body: 6 x 6 x 1.20mm

TFBGA84
Thin Profile Fine Pitch Ball Grid Array



10 Revision history

Table 23. Document revision history

Date	Revision	Changes
3-Feb-2006	1	Initial release.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZE REPRESENTATIVE OF ST, ST PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS, WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com