19-4193; Rev 2; 5/94

MAXIM

Octal, 8-Bit, Serial DACs with Output Buffer

General Description

The MAX528/MAX529 are monolithic devices combining an octal 8-bit, digital-to-analog converter (DAC), 8 output buffers, and serial-interface logic in a space-saving shrink small outline package (SSOP). The MAX528 operates from a single supply up to 15V or from split supplies totaling up to 20V, including +5V/-15V, +12V/-5V, and +15V/-5V. The MAX529 operates from a single +5V supply or from ±5V split supplies. For both parts, a shutdown pin reduces current consumption to under 50µA, while retaining all internal DAC data.

Three output modes are serially programmable for each pair of 8 analog outputs. An unbuffered mode connects the internal R-2R DAC network directly to the output pin, reducing power consumption and avoiding the buffer's DC errors. A full-buffered mode inserts a buffer between the R-2R network and the output, providing +5mA/-2mA output drive. Half-buffered output mode is similar, but uses less power while still providing up to 15mA of output drive in a unipolar output configuration.

Serial data can be "daisy-chained" from one device to another. On power-up, all data bits are reset to 0, and analog outputs enter the unbuffered mode.

Applications

Digital Gain and Offset Adjustment
Digital Calibration
Multiple Trim Pot Replacement
Microcontrolled Analog Outputs

Features

- ♦ **Now Available in Space-Saving SSOP**
- ♦ **8 Buffered Noninverting Outputs**
- ♦ **Buffer Disable Control**
- ♦ **2 Pairs of Differential Reference Inputs**
- ♦ **3-Wire Serial Interface**
- ♦ **Single +5V or Dual ±5V Supply Operation (MAX529)**
- ♦ **Low-Power Shutdown**
- ♦ **Stable Driving Output Capacitance Loads**

Ordering Information

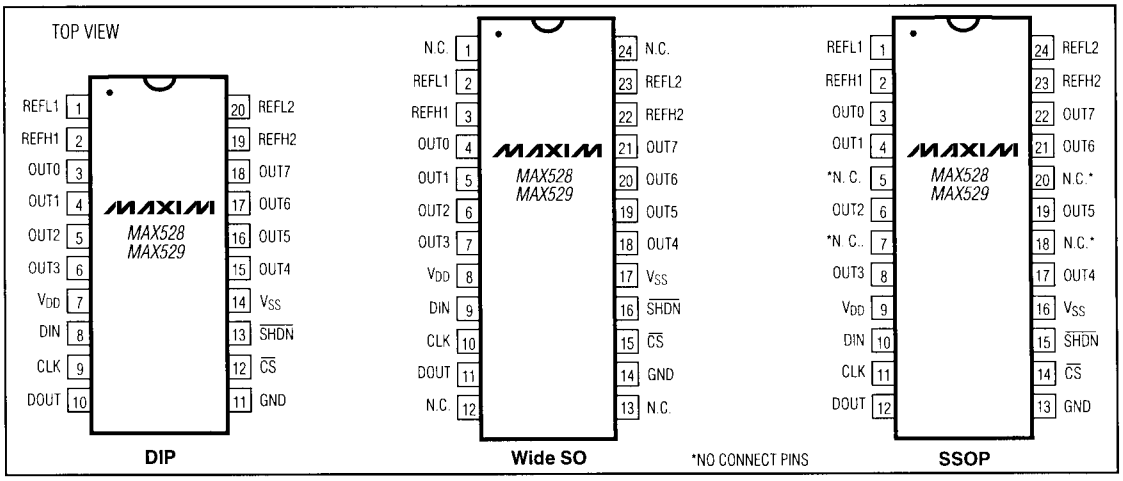
PART	TEMP. RANGE	PIN-PACKAGE
MAX528CPP	0°C to +70°C	20 Plastic DIP
MAX528CWG	0°C to +70°C	24 Wide SO
MAX528CAG	0°C to +70°C	24 SSOP
MAX528C/D	0°C to +70°C	Dice*
MAX528EPP	-40°C to +85°C	20 Plastic DIP
MAX528EWG	-40°C to +85°C	24 Wide SO
MAX528EAG	-40°C to +85°C	24 SSOP
MAX528MJP	-55°C to +125°C	20 CERDIP**

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



Octal 8-Bit Serial DACs with Output Buffer

ABSOLUTE MAXIMUM RATINGS - MAX528

V_{DD} to GND ..... -0.3V to +17V
V_{DD} to V_{SS} ..... -0.3V to +22V
V_{SS} to GND ..... -17V to +0.3V
REFH1 - REFL1, REFH2 - REFL2 ..... -0.3V to +12V
REFH1 - V_{SS}, REFH2 - V_{SS} ..... +17V
REFH1, REFH2 ..... REFL_ - 0.3V to V_{DD} + 0.3V
REFL1, REFL2 ..... V_{SS} - 0.3V to REFH_ + 0.3V
OUT(1-8) ..... V_{SS} - 0.3V to V_{DD} + 0.3V
OUT(1-8) to V_{SS} ..... +17V
OUT(1-8) Current ..... ±20mA
DIN, CLK, $\overline{CS}$, DOUT ..... -0.3V to V_{DD} + 0.3V
$\overline{SHDN}$ ..... V_{SS} - 0.3V to V_{DD} + 0.3V
DOUT Current ..... ±20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
Wide SO (derate 11.76mW/°C above +70°C) 941mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX528C_ _ ..... 0°C to +70°C
MAX528E_ _ ..... -40°C to +85°C
MAX528MJP ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS - MAX528

(Unbuffered Mode: V_{DD} = +12V, V_{SS} = 0V; Full-Buffered Mode: V_{DD} = +12V, V_{SS} = -5V; GND = 0V, REFH = +5V, REFL = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	UNBUFFERED MODE (Note 1)			FULL-BUFFERED MODE (Note 2)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC PERFORMANCE									
Resolution			8			8			Bits
Relative Accuracy (Note 3)	RLE			±0.3	±1.0		±0.3	±1.0	LSB
Differential Nonlinearity (Note 4)	DNL	Guaranteed monotonic		±0.3	±1.0		±0.3	±1.0	LSB
Full-Scale Error	FSE	R_{LOAD} = open			±1/2				LSB
Gain Error (Note 5)		R_{LOAD} = open					-0.2		%
		R_{LOAD} = 5kΩ				0.0	-1.3	-2.5	%
Zero-Code Error					±5			±60	mV
Zero-Code Tempco				±5			±100		µV/°C
DAC Output Resistance	R_{OUT}		8.5k	13k	20k		55	100	Ω
DAC Output Resistance Match	$\Delta R_{OUT}/R_{OUT}$			0.5			5.0		%
V_{DD} Supply Rejection Ratio (Note 6)	PSRR--V_{DD}	DAC code = 55 (hex)		0.1	1.0		0.3	2.0	mV/V
V_{SS} Supply Rejection Ratio (Notes 4,6)	PSRR--V_{SS}	DAC code = 55 (hex)		0.1	1.0		0.8	5.0	mV/V
REFERENCE INPUT									
Voltage Range (Note 7)	REFH	REFH - REFL = 11V max	REFL		V_{DD}-3	REFL		V_{DD}-3	V
	REFL		V_{SS}		REFH	V_{SS}+1.5		REFH	
Input Resistance (Note 8)	REFH1/REFL1, or REFH2/REFL2	DAC code = 55 (hex)	2.0	3.4		2.0	3.4		kΩ
Input Capacitance	C_{REFH}	DAC loaded with 0s		40			40		pF
		DAC loaded with 1s		250			125		
AC Feedthrough		REFH=10kHz, 0-10V_{p-p} sinewave, all DACs at code 00 (hex)		-70			-70		dB

ELECTRICAL CHARACTERISTICS - MAX528 (continued)

(Unbuffered Mode: V_{DD} = +12V, V_{SS} = 0V; Full-Buffered Mode: V_{DD} = +12V, V_{SS} = -5V; GND = 0V, REFH = +5V, REFL = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	UNBUFFERED MODE (Note 1)			FULL-BUFFERED MODE (Note 2)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER REQUIREMENTS									
Positive Supply Range	V_{DD}		10.8		16.5	10.8		16.5	V
Negative Supply Range	V_{SS}		0		-5.5	-1.5		-5.5	V
Positve Supply Current	I_{DD}	DIN = CLK = 0V, $\overline{CS}$ = $\overline{SHDN}$ = 5V		0.3	1.0		5.5	9.0	mA
Negative Supply Current	I_{SS}	DIN = CLK = 0V, $\overline{CS}$ = $\overline{SHDN}$ = 5V		0.1	0.5		5.5	9.0	mA
I_{DD} at Shutdown	I_{DD}	$\overline{SHDN}$ = low			50			50	µA
I_{SS} at Shutdown	I_{SS}	$\overline{SHDN}$ = low			50			50	µA
DYNAMIC PERFORMANCE (Note 7)									
V_{OUT} Settling Time		To ±1/2LSB; C_{LOAD} = 20pF, from rising edge of $\overline{CS}$		1	3		0.6	2.0	µs
Digital Coupling		Serial input: 1MHz CLK, DIN alternating 1s and 0s (0.5MHz), C_L = 20pF, 0V to 5V input levels at CLK, DIN		20			20		mVp-p
Crosstalk		Full-scale output transition on all 7 other channels ($\overline{CS}$ high)		40			20		nV-s
		1LSB output transition on all 7 other channels ($\overline{CS}$ high)		2			10		

DIGITAL AND SWITCHING CHARACTERISTICS - MAX528

(V_{DD} = +12V, V_{SS} = -5V, REFH = +5V, REFL = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS DIN, CLK, $\overline{CS}$, $\overline{SHDN}$						
Input High Voltage	V_{INH}	DIN, CLK, $\overline{CS}$	2.4			V
Input Low Voltage	V_{INL}	DIN, CLK, $\overline{CS}$			0.8	V
Input High Voltage	V_{INH}	$\overline{SHDN}$	3.0			V
Input Low Voltage	V_{INL}	$\overline{SHDN}$			0.5	V
Input Hysteresis		DIN, CLK, $\overline{CS}$		0.1		V
Input Leakage Current		V_{IN} = 0V or V_{DD}			±1	µA
Input Capacitance (Note 7)					10	pF
DIGITAL OUTPUT, DOUT, open drain output, 1kΩ pull-up resistor to +5V						
Output Low Voltage	V_{OL}	I_{SINK} = 5mA			0.4	V
Output High Leakage	I_{LKG}	V_{OUT} = 0V to V_{DD}			±10	µA
Output High Capacitance (Note 7)	C_{OUT}				15	pF

DIGITAL AND SWITCHING CHARACTERISTICS - MAX528 (continued)

(V_{DD} = +12V, V_{SS} = -5V, REFH = +5V, REFL = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
CLK Pulse Width High	t_{CH}		80			ns
CLK Pulse Width Low	t_{CL}		80			ns
DIN to CLK High Setup	t_{DS}		40			ns
DIN to CLK High Hold	t_{DH}		15			ns
$\overline{CS}$ Low to CLK High Setup	t_{CSS0}		50			ns
$\overline{CS}$ High to CLK High Setup	t_{CSS1}		50			ns
Delay, CLK Low to Low $\overline{CS}$	t_{CSH0}		0			ns
Delay, CLK High to High $\overline{CS}$	t_{CSH1}		50			ns
$\overline{CS}$ Pulse Width	t_{CSW}		130			ns
CLK High to DOUT Data Valid (Note 9)	t_{DO}	C_{LOAD} = 20pF, Rpullup = 1kΩ to 5V	15 (Note 7)		130	ns
$\overline{CS}$ Low to DOUT Enable (Note 10)	t_{DV}	C_{LOAD} = 20pF, Rpullup = 1kΩ to 5V			90	ns
$\overline{CS}$ High to DOUT Disable (Note 10)	t_{TR}	C_{LOAD} = 20pF, Rpullup = 1kΩ to 5V			90	ns

Note 1: Unbuffered mode – buffers disabled. No output load.
Note 2: Full-buffered mode - buffers enabled; bipolar output mode; R_{LOAD} = 5kΩ.
Note 3: Relative accuracy in unbuffered mode guaranteed by relative accuracy test in full-buffered mode.
Note 4: Specification in Unbuffered Mode column guaranteed by design only. Not subject to test.
Note 5: Gain error with full-buffered mode enabled = no-load gain error - (DAC output resistance/R_{LOAD}). Example: -0.2% typ no-load error - (55Ω/5kΩ) = -1.3% typ error for 5kΩ load.
Note 6: PSRR tested over supply range specified under power requirements; PSRR = (V_{OUT1} - V_{OUT2})/($V_{SUPPLY1}$ - $V_{SUPPLY2}$).
Note 7: Guaranteed by design, not subject to test.
Note 8: Input resistance tested only under Unbuffered Mode conditions in Note1 above.
Note 9: V_{OH} = 2.4V, V_{OL} = 0.8V.
Note 10: t_{DV} and t_{TR} are defined as the time required for DOUT to change 0.5V.

ABSOLUTE MAXIMUM RATINGS - MAX529

V_{DD} to GND ..... -0.3V to +7V
V_{DD} to V_{SS} ..... -0.3V to +12V
V_{SS} to GND ..... -7V to +0.3V
REFH1 - REFL1, REFH2 - REFL2 ..... -0.3V to +12V
REFH1 - V_{SS}, REFH2 - V_{SS} ..... +12V
REFH1, REFH2 ..... REFL_ - 0.3V to V_{DD} + 0.3V
REFL1, REFL2 ..... V_{SS} - 0.3V to REFH_ + 0.3V
OUT(1-8) ..... V_{SS} - 0.3V to V_{DD} + 0.3V
OUT(1-8) to V_{SS} ..... +12V
OUT(1-8) Current ..... ±20mA
DIN, CLK, CS, DOUT ..... -0.3V to V_{DD} + 0.3V
SHDN ..... V_{SS} - 0.3V to V_{DD} + 0.3V

DOUT Current ..... ±20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
Wide SO (derate 11.76mW/°C above +70°C) 941mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX528C_ _ ..... 0°C to +70°C
MAX528E_ _ ..... -40°C to +85°C
MAX528MJP ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS - MAX529

(Unbuffered Mode: V_{DD} = +5V, V_{SS} = GND = 0V, REFH = +2.5V, REFL = 0V; Full-Buffered Mode: V_{DD} = +5V, V_{SS} = -5V, GND = 0V, REFH = +2.5V, REFL = -2.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	UNBUFFERED MODE (Note 1)			FULL-BUFFERED MODE (Note 2)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC PERFORMANCE									
Resolution			8			8			Bits
Relative Accuracy (Note 3)	RLE			±0.3	±1.0		±0.3	±1.0	LSB
Differential Nonlinearity (Note 4)	DNL	Guaranteed monotonic		±0.3	±1.0		±0.3	±1.0	LSB
Full-Scale Error	FSE	R_{LOAD} = open			±1/2				LSB
Gain Error (Note 5)		R_{LOAD} = open					-0.2		%
		R_{LOAD} = 5kΩ				0.0	-1.3	-2.5	%
Unipolar Offset Error		DAC code = 00 (hex)			±5				mV
Bipolar Offset Error		DAC code = 80 (hex)						±60	mV
Offset Error Tempco				±5			±100		µV/°C
DAC Output Resistance	R_{OUT}		8.5k	13k	20k		55	100	Ω
DAC Output Resistance Match	$\Delta R_{OUT}/R_{OUT}$			0.5			5.0		%
V_{DD} Supply Rejection Ratio (Note 6)	PSRR--V_{DD}	DAC code = 55 (hex)		1.5	5		3	10	mV/V
V_{SS} Supply Rejection Ratio (Notes 4,6)	PSRR--V_{SS}	DAC code = 55 (hex)		0.3	2		1	5	mV/V
REFERENCE INPUT									
Voltage Range (Note 7)	REFH		REFL		V_{DD} - 2.25	REFL		V_{DD} - 2.25	V
	REFL		V_{SS}		REFH	V_{SS} + 1.5		REFH	
Input Resistance (Note 8)	REFH1/REFL1, or REFH2/REFL2	DAC code = 55 (hex)	2.0	3.4		2.0	3.4		kΩ
Input Capacitance	C_{REFH}	DAC loaded with 0s		40			40		pF
		DAC loaded with 1s		250			125		

Octal 8-Bit Serial DACs with Output Buffer

ELECTRICAL CHARACTERISTICS - MAX529 (continued)

(Unbuffered Mode: V_{DD} = +5V, V_{SS} = GND = ON, REFH = +2.5V, REFL = 0V; Full-Buffered Mode: V_{DD} = +5V, V_{SS} = -5V, GND = 0V, REFH = +2.5V, REFL = -2.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	UNBUFFERED MODE (Note 1)			FULL-BUFFERED MODE (Note 2)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC Feedthrough		REFH=10kHz, 0-2.5V_{p-p} sinewave, all DACs at code 00 (hex)		-70			-70		dB
POWER REQUIREMENTS									
Positive Supply Range	V_{DD}		4.75		5.25	4.75		5.25	V
Negative Supply Range	V_{SS}		0		-5.5	-4.5		-5.5	V
Positve Supply Current	I_{DD}	DIN = CLK = 0V, $\overline{CS}$ = $\overline{SHDN}$ = 5V		0.3	1.0		5.5	9.0	mA
Negative Supply Current	I_{SS}	DIN = CLK = 0V, $\overline{CS}$ = $\overline{SHDN}$ = 5V		0.1	0.5		5.5	9.0	mA
I_{DD} at Shutdown	I_{DD}	$\overline{SHDN}$ = low			50			50	µA
I_{SS} at Shutdown	I_{SS}	$\overline{SHDN}$ = low			50			50	µA
DYNAMIC PERFORMANCE (Note 7)									
V_{OUT} Settling Time		To ±1/2LSB; C_{LOAD} = 20pF, from rising edge of $\overline{CS}$		1	3		0.6	2.0	µs
Digital Coupling		Serial input: 1MHz CLK, DIN alternating 1s and 0s (0.5MHz), C_L = 20pF, 0V to 5V input levels at CLK, DIN		20			20		mVp-p
Crosstalk		Full-scale output transition on all 7 other channels ($\overline{CS}$ high)		40			20		nV-s
		1LSB output transition on all 7 other channels ($\overline{CS}$ high)		2			10		

DIGITAL AND SWITCHING CHARACTERISTICS - MAX529

(V_{DD} = +5V, V_{SS} = -5V, REFH = +2.5V, REFL = -2.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS DIN, CLK, $\overline{CS}$, $\overline{SHDN}$		$\overline{SHDN}$				
Input High Voltage	V_{INH}	DIN, CLK, $\overline{CS}$	2.4			V
Input Low Voltage	V_{INL}	DIN, CLK, $\overline{CS}$			0.8	V
Input High Voltage	V_{INH}	$\overline{SHDN}$	3.0			V
Input Low Voltage	V_{INL}	$\overline{SHDN}$			0.5	V
Input Hysteresis		DIN, CLK, $\overline{CS}$		0.1		V
Input Leakage Current		V_{IN} = 0V or V_{DD}			±1	µA
Input Capacitance (Note 7)					10	pF
DIGITAL OUTPUT, DOUT, open drain output, 1.3kΩ pull-up resistor to +5V						
Output Low Voltage	V_{OL}	I_{SINK} = 3.5mA			0.4	V
Output High Leakage	I_{LKG}	V_{OUT} = 0V to V_{DD}			±10	µA
Output High Capacitance (Note 7)	C_{OUT}				15	pF

DIGITAL AND SWITCHING CHARACTERISTICS - MAX529 (continued)

(V_{DD} = +5V, V_{SS} = -5V, REFH = +2.5V, REFL = -2.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

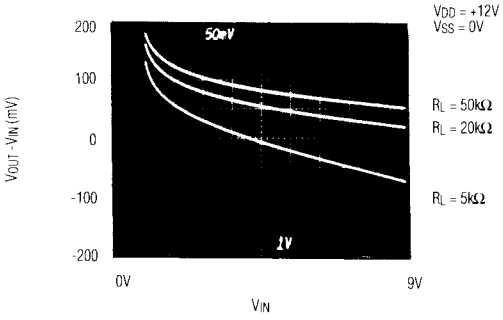
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
CLK Pulse Width High	t_{CH}		125			ns
CLK Pulse Width Low	t_{CL}		125			ns
DIN to CLK High Setup	t_{DS}		50			ns
DIN to CLK High Hold	t_{DH}		20			ns
$\overline{CS}$ Low to CLK High Setup	t_{CS0}		50			ns
$\overline{CS}$ High to CLK High Setup	t_{CS1}		50			ns
Delay, CLK Low to Low $\overline{CS}$	t_{CSH0}		0			ns
Delay, CLK High to High $\overline{CS}$	t_{CSH1}		50			ns
$\overline{CS}$ Pulse Width	t_{CSW}		300			ns
CLK High to DOUT Data Valid (Note 9)	t_{DO}	C_{LOAD} = 20pF, Rpullup = 1kΩ to 5V	20 (Note 7)		200	ns
$\overline{CS}$ Low to DOUT Enable (Note 10)	t_{DV}	C_{LOAD} = 20pF, Rpullup = 1kΩ to 5V			120	ns
$\overline{CS}$ High to DOUT Disable (Note 10)	t_{TR}	C_{LOAD} = 20pF, Rpullup = 1kΩ to 5V			120	ns

Note 1: Unbuffered mode – buffers disabled. No output load.
Note 2: Full-buffered mode – buffers enabled; bipolar output mode; R_{LOAD} = 5kΩ.
Note 3: Relative accuracy in unbuffered mode guaranteed by relative accuracy test in full-buffered mode.
Note 4: Specification in Unbuffered Mode column guaranteed by design only. Not subject to test.
Note 5: Gain error with full-buffered mode enabled = no-load gain error - (DAC output resistance/R_{LOAD}). Example: -0.2% typ no-load error - (55Ω/5kΩ) = -1.3% typ error for 5kΩ load.
Note 6: PSRR tested over supply range specified under power requirements; PSRR = (V_{OUT1} - V_{OUT2})/($V_{SUPPLY1}$ - $V_{SUPPLY2}$).
Note 7: Guaranteed by design, not subject to test.
Note 8: Input resistance tested only under Unbuffered Mode conditions in Note1 above.
Note 9: V_{OH} = 2.4V, V_{OL} = 0.8V.
Note 10: t_{DV} and t_{TR} are defined as the time required for DOUT to change 0.5V.

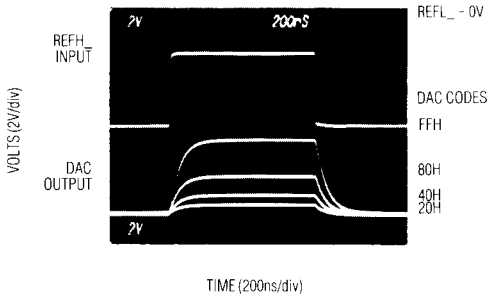
Typical Operating Characterisitics

MAX528

MAX528
HALF-BUFFERED GAIN AND LINEARITY ERROR vs. V_{IN} (OUTPUT VOLTAGE OF R-2R LADDER)



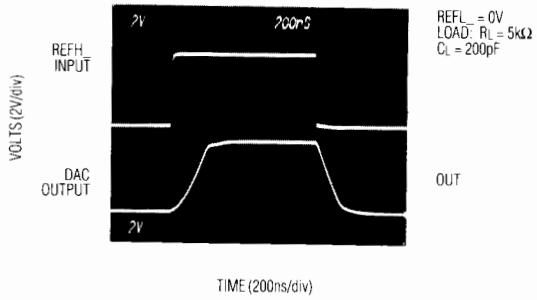
MAX528
FULL-BUFFERED STEP RESPONSE FOR VARIOUS CODES, NO LOAD



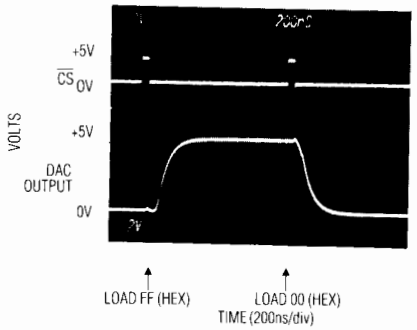
Octal 8-Bit Serial DACs with Output Buffer

Typical Operating Characterisitics (continued)

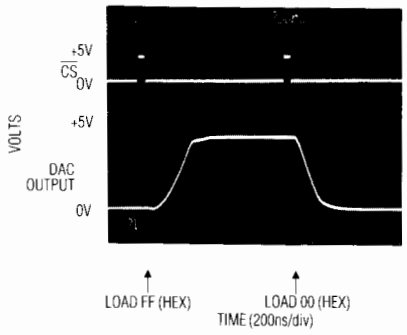
MAX528
FULL-BUFFERED STEP RESPONSE



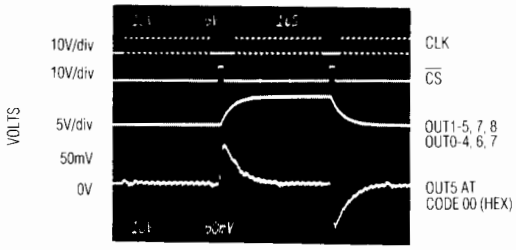
MAX528
FULL-BUFFERED SETTLING TIME
CODE CHANGE (00-FF-00), NO LOAD



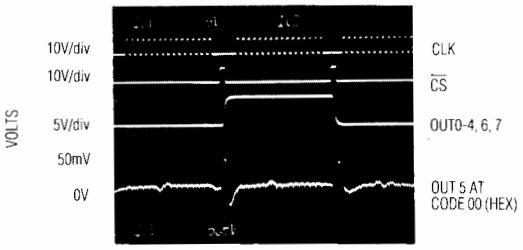
MAX528
FULL-BUFFERED SETTLING TIME
CODE CHANGE (00-FF-00)



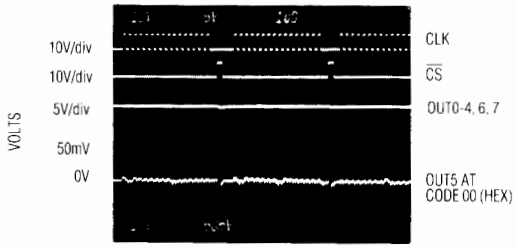
MAX528
UNBUFFERED OFF-CHANNEL GLITCH
CODE CHANGE (00-FF-00), NO LOAD



MAX528
FULL-BUFFERED OFF-CHANNEL GLITCH
CODE CHANGE (00-FF-00), NO LOAD

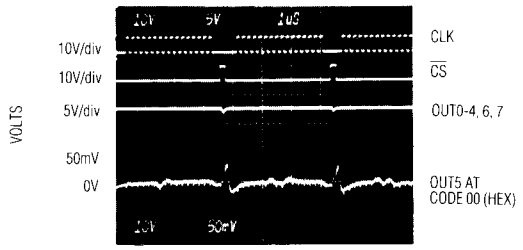


MAX528
UNBUFFERED OFF-CHANNEL GLITCH
CODE CHANGE (7F-80-7F), NO LOAD



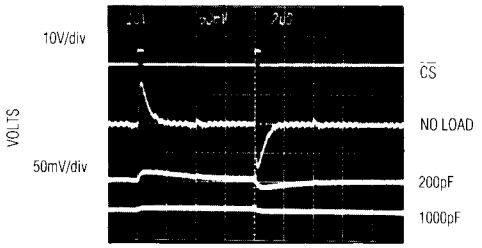
Typical Operating Characteristics (continued)

MAX528
FULL-BUFFERED OFF-CHANNEL GLITCH CODE CHANGE (7F-80-7F), NO LOAD



TIME (1µs/div)

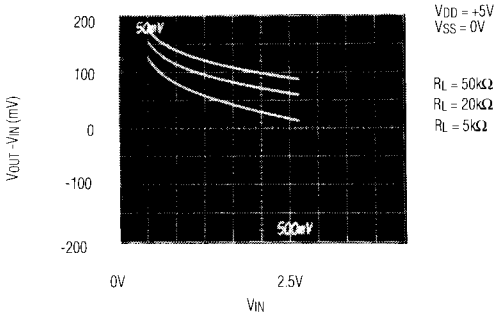
MAX528
UNBUFFERED OUTPUT GLITCH FILTERING



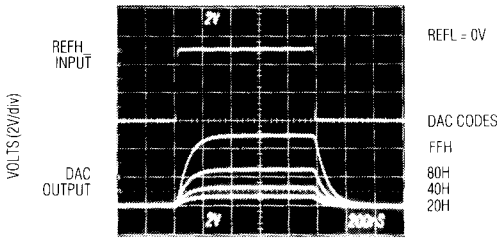
TIME (2µs/div)

MAX529

MAX529
HALF-BUFFERED GAIN AND LINEARITY ERROR vs. V_{IN} (OUTPUT VOLTAGE OF R-2R LADDER)

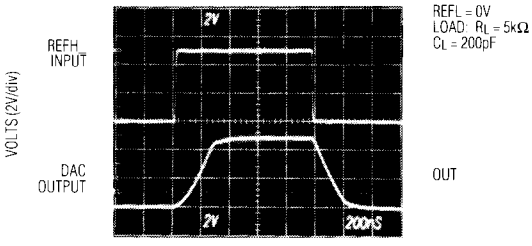


MAX529
FULL-BUFFERED STEP RESPONSE FOR VARIOUS CODES, NO LOAD



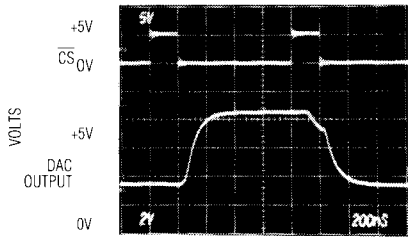
TIME (200ns/div)

MAX529
FULL-BUFFERED STEP RESPONSE



TIME (200ns/div)

MAX529
FULL-BUFFERED SETTLING TIME CODE CHANGE (00-FF-00), NO LOAD

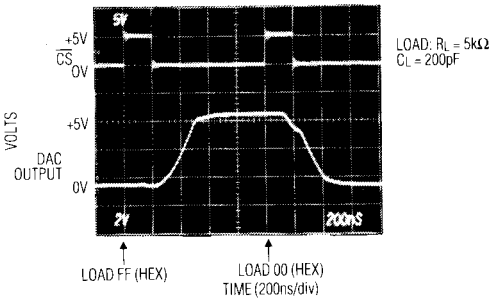


TIME (200ns/div)

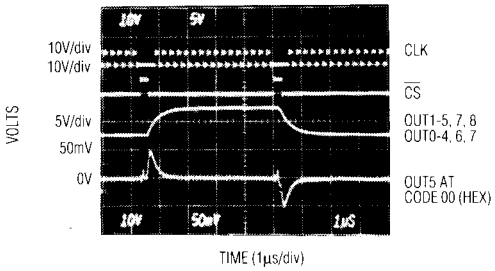
Octal 8-Bit Serial DACs with Output Buffer

Typical Operating Characteristics (continued)

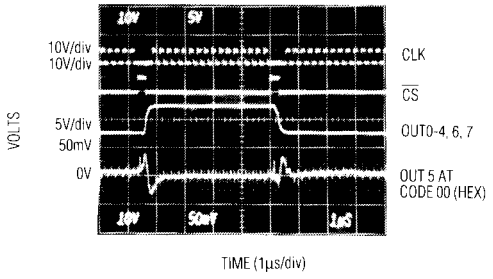
MAX529
FULL-BUFFERED SETTLING TIME
CODE CHANGE (00-FF-00)



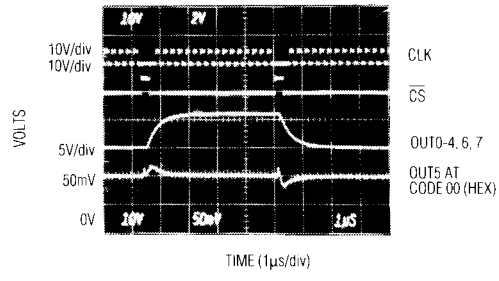
MAX529
UNBUFFERED OFF-CHANNEL GLITCH
CODE CHANGE (00-FF-00), NO LOAD



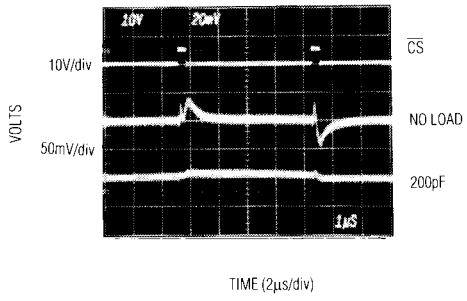
MAX529
FULL-BUFFERED OFF-CHANNEL GLITCH
CODE CHANGE (00-FF-00), NO LOAD



MAX529
UNBUFFERED OFF-CHANNEL GLITCH
CODE CHANGE (00-FF-00), NO LOAD



MAX529
UNBUFFERED OUTPUT
GLITCH FILTERING



Pin Description

PIN			NAME	FUNCTION
SSOP	DIP	SO		
5, 7, 18, 20	–	1, 12, 13, 24	N.C.	No Connect. These pins are not internally connected.
1	1	2	REFL1	Reference 1 Input Low. Must be more negative than REFH1 and more positive than V_{SS}.
2	2	3	REFH1	Reference 1 Input High. Must be more positive than REFL1 and more negative than V_{DD}.
3	3	4	OUT0	Output Voltage 0. The product of the digital code for channel 0 and (REFH1 - REFL1), referenced to REFL1.
4	4	5	OUT1	Output Voltage 1. The product of the digital code for channel 1 and (REFH1 - REFL1), referenced to REFL1.
6	5	6	OUT2	Output Voltage 2. The product of the digital code for channel 2 and (REFH1 - REFL1), referenced to REFL1.
8	6	7	OUT3	Output Voltage 3. The product of the digital code for channel 3 and (REFH1 - REFL1), referenced to REFL1.
9	7	8	V_{DD}	Positive Analog and Digital Supply.
10	8	9	DIN	Digital Input. CMOS and TTL compatible serial programming input.
11	9	10	CLK	Clock Input. CMOS and TTL compatible clock input.
12	10	11	DOUT	Digital Output. Open-drain, N-channel, FET output, requires external pull-up resistor; serial data output, shifted 16 bits from DIN.
13	11	14	GND	Digital Ground. Connect to 0V. (Analog signals are referenced to their respective REFL voltage,not GND).
14	12	15	$\overline{CS}$	$\overline{CHIP\ SELECT}$. Connect to logic low to program serially. Connect to logic high to latch data and turn off internal shift register. Rising edge of $\overline{CS}$ transfers new data into data registers and changes DAC output.
15	13	16	$\overline{SHDN}$	$\overline{SHUTDOWN}$. Connect to logic high for normal operation, to GND for shutdown mode.
16	14	17	V_{SS}	Negative Analog Supply. Connect to GND for single-supply operation. Connect to negative supply for bipolar DAC outputs.
17	15	18	OUT4	Output Voltage 4. The product of the digital code for channel 4 and (REFH2 - REFL2), referenced to REFL2.
19	16	19	OUT5	Output Voltage 5. The product of the digital code for channel 5 and (REFH2 - REFL2), referenced to REFL2.
21	17	20	OUT6	Output Voltage 6. The product of the digital code for channel 6 and (REFH2 - REFL2), referenced to REFL2.
22	18	21	OUT7	Output Voltage 7. The product of the digital code for channel 7 and (REFH2 - REFL2), referenced to REFL2.
23	19	22	REFH2	Reference 2 Input High. Must be more positive than REFL2 and more negative than V_{DD}.
24	20	23	REFL2	Reference 2 Input Low. Must be more negative than REFH2 and more positive than V_{SS}.

Octal 8-Bit Serial DACs with Output Buffer

Detailed Description

Circuit Operation

The MAX528/MAX529 contain 8 latched digital-to-analog converters (DACs), 8 buffer amplifiers, 2 reference inputs, and serial control logic. Buffer amplifiers may also be bypassed by internal switches, allowing three output modes: unbuffered, full-buffered, and half-buffered.

Any or all of the 8 voltage outputs can be programmed with 16 serial data bits.

DAC Output Range

The MAX528/MAX529 provide 8 voltage outputs (OUT0-OUT7) from 2 reference inputs. Each reference voltage has 2 input pins, REFH and REFL. The OUT0-OUT3 output voltages are derived from REFH1 and REFL1 while OUT4-OUT7 are derived from REFH2 and REFL2. For each reference, REFH must be more positive than REFL. A DAC output voltage is the product of its programmed 8-bit code and its reference input voltage. For example, the output voltage of OUT5 is:

$$OUT5 = (REFH2 - REFL2)\ (nn/256 + REFL2),$$

where nn = 8-bit code for OUT5, with a range of 0-255 (00 to FF hex.)

The reference inputs are independent of one another. REFH can range within 3V of V_{DD}. REFL can be as low as V_{SS} in unbuffered and half-buffered modes, but must be at least 1.5V above V_{SS} in full-buffered mode. For the MAX528, V_{SS} can be any negative voltage from -15V to 0V, provided that V_{DD}-V_{SS} is no more than 20V. For the MAX529, V_{SS} can be any negative voltage from 0V to -5V. In all modes, REFH must be no more than 12V greater than REFL.

Although the MAX528/MAX529 have a digital ground (GND) pin, they contain no internal analog ground. The upper and lower limits of any DAC output are the voltages to which REFH and REFL are connected.

Shutdown

To conserve power, the MAX528/MAX529 can be shut down by pulling $\overline{SHDN}$ low. V_{CC} and V_{SS} supply currents drop to less than 50µA, but reference current will still be drawn. Reference current is code dependent and can be reduced to nearly 0 (leakage only) by writing 0s to all DACs.

Note: To ensure that register data is retained during shutdown, $\overline{CS}$ must be high when entering or leaving shutdown mode.

Buffer Output Modes

DAC outputs can be programmed for one of three buffer modes: unbuffered, full-buffered, and half-buffered. Buffers must be activated in pairs, and full- or half-buffered mode must be selected in banks of four as shown in Table 1 (see *Digital Interface* section).

Table 1. Buffer Output-Mode Selection Codes (Address 00 hex, D6 = X, D7 = 1)

Mode	OUT0, 1	OUT2, 3	OUT4, 5	OUT5, 6
Unbuffered (D0, D3=X)	D5 = 0	D4 = 0	D2 = 0	D1 = 0
Full-Buffered	D5 = 1	D4 = 1	D2 = 1	D1 = 1
	D3 = 1		D0 = 1	
Half-Buffered	D5 = 1	D4 = 1	D2 = 1	D1 = 1
	D3 = 0		D0 = 0	

Unbuffered Mode

Unbuffered mode connects the internal 20kΩ R-2R DAC network (Figure 1) directly to OUT. Buffer circuitry is disabled, reducing power consumption as well as offset errors contributed by the internal buffer amplifier (see *Electrical Characteristics*). Driving high-resistance loads (1MΩ and up) improves accuracy. Output range in unbuffered mode is from the negative supply rail (V_{SS}) to V_{DD} - 3V for the MAX528 (V_{SS} to V_{DD} -2.25V for MAX529).

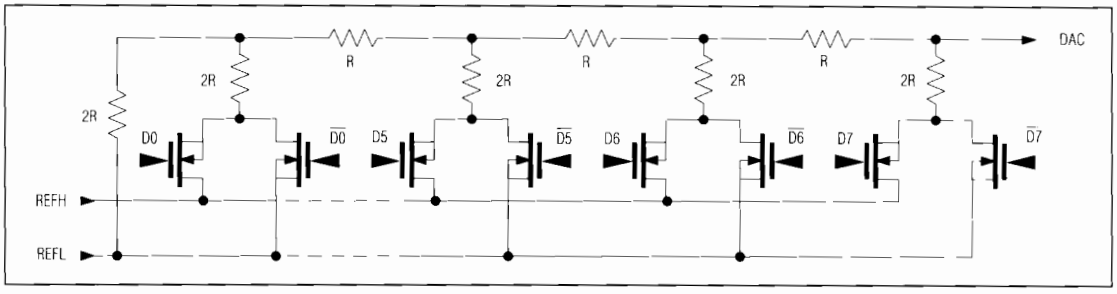


Figure 1. R-2R Inverted Ladder DAC Structure

Unbuffered mode also operates effectively with lower resistance loads, but output loading may generate gain (full-scale) error. This will not affect linearity because DAC output resistance (between 8.5kΩ and 20kΩ) does not change with code. The magnitude of the expected gain error is the ratio of the DAC output impedance (typically 13kΩ) to the DC load resistance at the output.

Another advantage of unbuffered operation is that output filtering uses small capacitors and no resistors. The Unbuffered Output Glitch Filtering photos in the *Typical Operating Characteristics* show the feedthrough effect of changing all channels but one from full-scale to zero. On the rising edge of $\overline{CS}$ (top trace), energy is coupled into the unchanged channel (2nd trace, unfiltered), producing a 70mV, 1µs pulse for the MAX528, and a 40mV, 5µs pulse for the MAX529. The third and fourth traces of the MAX528 photo show how this pulse is suppressed using 200pF and 1000pF load capacitors with the MAX528. The third trace of the MAX529 photo shows this pulse suppression using a 200pF load capacitor with the MAX529.

Full-Buffered Mode

Full-buffered mode (Figure 2) activates both sections of the buffer amplifer, lowering the output impedance to typically 55Ω and allowing +5mA/-2mA output currents to be supplied. The buffer amplifier output swing is from V_{SS} + 1.5V to V_{DD} - 3V (V_{SS} = +1.5V to V_{DD} - 2.25V for MAX529). The key advantage of this mode is that changes in load current cause minimal output change.

Half-Buffered Mode

Half-buffered mode (Figure 3) activates only the top half of the output stage, and therefore sources current only. Its advantage is that it maintains output swing to V_{SS} while providing a buffered output. Output swing is from V_{SS} to V_{DD} - 3V (V_{SS} = +1.5V to V_{DD} - 2.25V for MAX529). Current consumption is reduced to typically 1.7mA (compared to 5.5mA for full-buffered) if all buffers use half-buffered mode.

Using an AC Reference with the MAX528

In applications where the reference has AC signal components, the MAX528 has multiplying capability within the REFH and REFL specifications. Figure 4 shows a technique for attenuating an AC signal by superimposing it on a DC voltage prior to REFH. As the DAC code changes, the AC output changes, as does the DC level. The output DC level is removed by capacitively coupling to the next stage. Note that the peak negative voltage at REFH must not swing below REFL.

Digital Interface

Serial Interface

Serial data at DIN is clocked in on the rising edge of CLK, while $\overline{CS}$ is low and $\overline{SHDN}$ is high (Figure 5). Data can be loaded at clock rates up to 6.25MHz (4MHz for MAX529). Logic inputs are CMOS and TTL compatible. The serial output DOUT is an open-drain N-channel FET that sinks up to 5mA and requires an external pull-up resistor (typically 4.7kΩ) to V_{DD}. Output data changes on the rising edge of CLK.

Any number of MAX528s or MAX529s can be daisy-chained by connecting the DOUT pin of one device (with pullup resistor) to the $\overline{DIN}$ pin of the following device in the chain. CLK and $\overline{CS}$ are bussed together. Clock period and t_{CSS0} ($\overline{CS}$ low to CLK high) must be increased to account for data delays between devices.

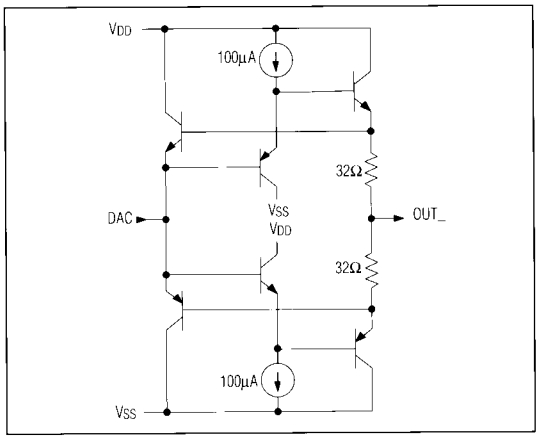


Figure 2. Simplifed Full-Buffered Output Circuit

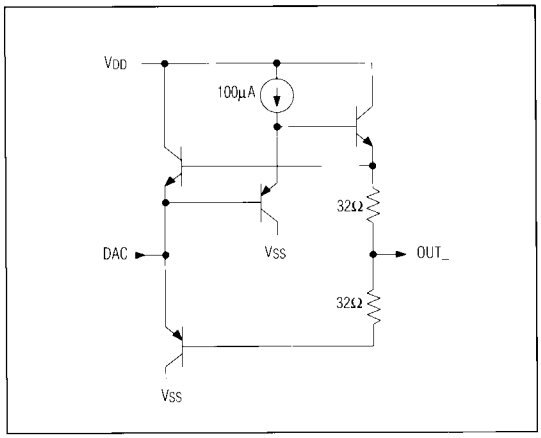


Figure 3. Simplifed Half-Buffered Output Circuit

Octal 8-Bit Serial DACs with Output Buffer

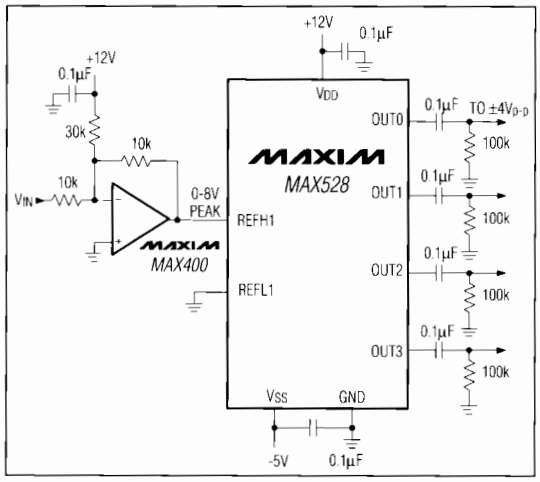


Figure 4. Using an AC Reference with the MAX528

If capacitive loading at the DOUT-to-DIN junction between two devices is 50pF or less, then the required t_{CSS0} becomes the sum of t_{DV} (enable) and t_{DS} (setup times), which is 130ns (90ns + 40ns) for MAX528 and t_{CSS0} 170ns (120ns + 50ns) for the MAX529.

Maximum clock rate is influenced by pullup resistor size as well as capacitive loading: $f_{CLK}max = 1/(t_{DO} + t_{DS} + 0.65t_{RC})$, where t_{DO} = 130ns, t_{DS} = 40ns, and t_{RC} is the pullup resistor and capacitive load product. So for a 1kΩ pullup and 50pF load, the MAX528 $f_{CLK}max$ is 4.7MHz; for a 4.7kΩ pullup with 50pF load, $f_{CLK}max$ drops to 2.8MHz. A similar calculation can be made for the MAX529, using t_{DO} = 200ns, and t_{DS} = 50ns.

DAC Programming

The MAX528/MAX529 are programmed by 16 data bits in two 8-bit bytes, the address pointer bits (A7-A0) followed by the data byte (D7-D0). These bits enter a shift register serially through DIN: A7 first, and D0 last. The data exits DOUT 16 clock cycles later in the same order.

Data at DIN is shifted into the first register (while all 16 register bits shift forward one stage) on a rising CLK edge, while holding $\overline{CS}$ low and $\overline{SHDN}$ high. This must occur 16 times to load all data bits into the shift registers. On the rising edge of $\overline{CS}$, data in the 16 shift registers is transferred as addressed and CLK is disabled.

There are three types of instructions: NOP, SET DAC, and set buffer modes.

No Operation

No Operation (NOP) is implemented when all 8 address pointer bits (A7-A0) and data bit D7 are logic 0. Data in D6-D0 is ignored. When this instruction is clocked in, no registers are updated and the outputs remain unchanged. NOP is a place-saver when multiple MAX528/MAX529s are daisy-chained.

SET DAC

SET DAC is implemented when at least one of the 8 address pointer bits (A7-A0) is logic 1. SET DAC updates the digital code of any or all DAC registers (and their corresponding DAC outputs) to a single new value. The new value is contained in the data byte (D7-D0). Each address pointer bit (A7-A0) selects a DAC output. Any combination of outputs can be updated simultaneously with one 16-bit instruction. Remember that address 0000 0000 is reserved for NOP and set buffer modes.

SET DAC does not change the buffer modes.

Set Buffer Modes

Set buffer modes is implemented when all 8 address pointer bits (A7-A0) are logic 0 and data bit D7 is 1. (see Table 1). Data in D6 is ignored. When this instruction is issued, data bits D5-D0 are transferred to the mode registers only; the DAC registers are unchanged.

Enabling and disabling the 8 buffers is done in four pairs by data bits D1, D2, D4, and D5. D1 controls buffers 6 and 7, D2 controls buffers 4 and 5, D4 controls buffers 2 and 3, and D5 controls buffers 0 and 1. A logic 1 enables a buffer pair (full-buffered or half-buffered mode); a logic 0 disables a buffer pair (unbuffered mode).

Full-buffered and half-buffered modes are set by two data bits, D0 and D3. D0 controls OUT4 through OUT7; D3 controls OUT0 through OUT3. A logic 1 enables full-buffered mode; a logic 0 enables half-buffered mode. These data bits apply only when buffer output pairs are enabled by a 1 in D1, D2, D4, or D5.

The set buffer modes instruction does not update the DAC registers.

Programming Data

Table 2. Programming NOP

Data Direction: First >----------> Last

Function	Address Pointer Bits								Data Byte							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
NOP	0	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X

X = Don't Care

Table 3. Programming SET DAC Outputs

Function	Address Pointer Bits								Data Byte							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
SET DAC Outputs	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

DAC code, 0000 0000 to 1111 1111 (00 Hex through FF Hex) D7 = MSB; D0 = LSB.
AX = set DAC register X to digital value D7-D0. A7 = OUT7...A0 = OUT0. Logic 1 sets the DAC register to new DAC code in D7-D0; logic 0 ignores D7-D0 code and keeps previous code. At least one of theses 8 bits must be 1 (A7-A0 = 01 hex to FF hex).

Table 4. Programming Set Buffer Modes

Function	Address Pointer Bits								Data Byte							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Set Buffer Modes	0	0	0	0	0	0	0	0	1	X	0&1	2&3	0/3	4&5	6&7	4/7

X = Don't Care (D6)
0&1 (D5) = buffer enable for OUT0 and OUT1. Logic 1 = buffers enabled, 0 = buffers disabled (unbuffered mode). Similar remarks apply to 2&3 (D4), 4&5 (D2), and 6&7 (D1).
0/3 (D3) = buffer modes for OUT0-3. Logic 1 = full-buffered mode, 0 = half-buffered mode. D3 has no meaning when D4 and D5 are both 0.
4/7 (D0) = buffer modes for OUT4-7. Logic 1 = full-buffered mode, 0 = half-buffered mode. D0 has no meaning when D1 and D2 are both 0.

Programming Examples

Example 1: Set OUT0, OUT2, OUT7 to binary value 0100 1110 (4E hex). Leave OUT1, OUT3, OUT4, OUT5, and OUT6 unchanged, and leave buffer states unchanged.

Data Direction: First >----------> Last

	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Example 1	1	0	0	0	0	1	0	1	0	1	0	0	1	1	1	0

Example 2: Set all DACs except OUT6 to binary value 0000 0000 (00 hex). Leave OUT6 unchanged, and leave buffer states unchanged.

	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Example 2	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Example 3: Disable all buffers (unbuffered mode). Leave DAC data unchanged.

	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Example 3	0	0	0	0	0	0	0	0	1	X	0	0	X	0	0	X

X = Don't Care

Example 4: (1) Enable OUT0 and OUT1 buffers in full-buffered mode; put OUT2 and OUT3 in unbuffered mode.
(2) Enable OUT6 and OUT7 buffers in half-buffered mode; put OUT4 and OUT5 in unbuffered mode. Leave DAC data unchanged.

	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Example 4	0	0	0	0	0	0	0	0	1	X	1	0	1	0	1	0

X = Don't Care

Octal 8-Bit Serial DACs with Output Buffer

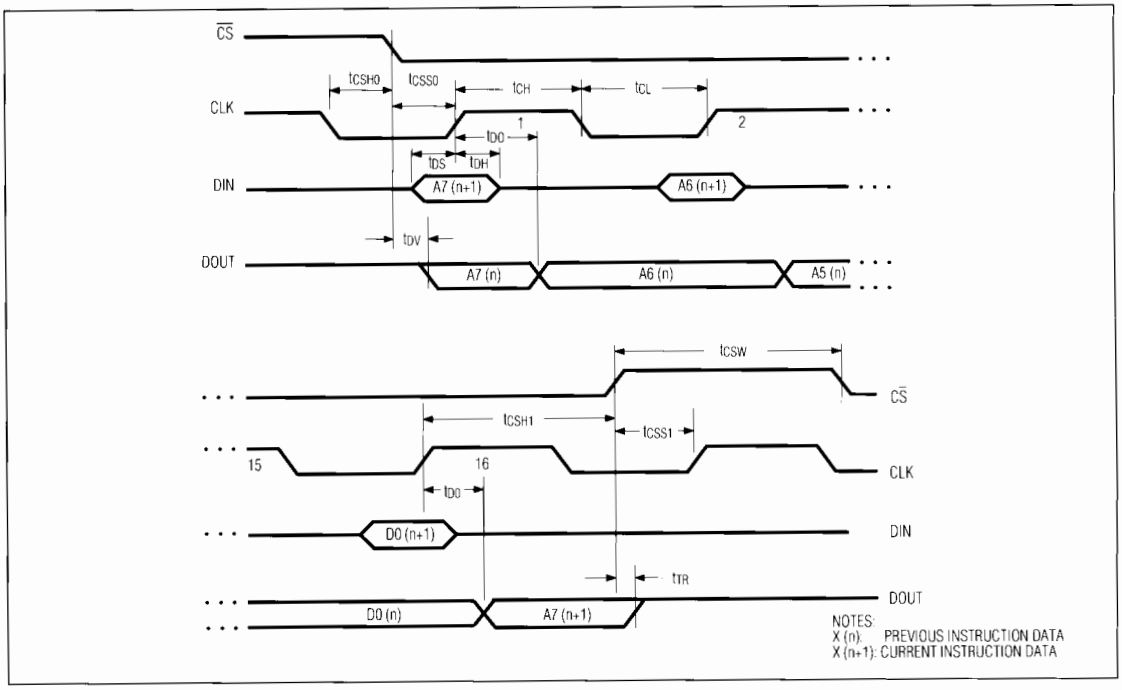


Figure 5. Timing Diagram

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX529CPP	0°C to +70°C	20 Plastic DIP
MAX529CWG	0°C to +70°C	24 Wide SO
MAX529CAG	0°C to +70°C	24 SSOP
MAX529C/D	0°C to +70°C	Dice*
MAX529EPP	-40°C to +85°C	20 Plastic DIP
MAX529EWG	-40°C to +85°C	24 Wide SO
MAX529EAG	-40°C to +85°C	24 SSOP
MAX529MJP	-55°C to +125°C	20 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram