

T.46-23-05

CY7C197

256K x 1 Static R/W RAM

CYPRESS
SEMICONDUCTOR

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
 - 20 ns
- Low active power
 - 880 mW
- Low standby power
 - 220 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C197 is a high-performance CMOS static RAM organized as 256K words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C197 has an automatic power-down feature, reducing the power consumption by 75% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (D_{OUT}) pin.

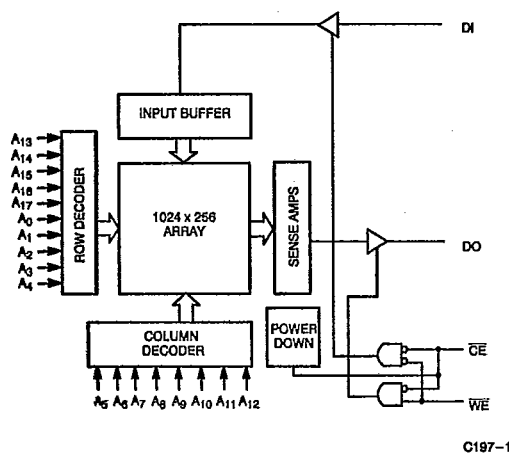
The output pin stays in high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

The 7C197 utilizes a die coat to insure alpha immunity.

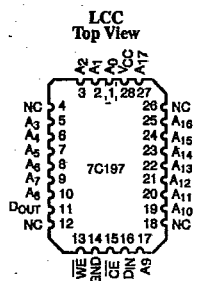
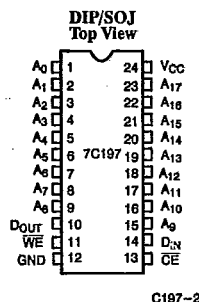


SRAMs

Logic Block Diagram



Pin Configurations



Selection Guide

		7C197-12	7C197-15	7C197-20	7C197-25	7C197-35	7C197-45
Maximum Access Time (ns)		12	15	20	25	35	45
Maximum Operating Current (mA)	Commercial	160	150	140	100	100	100
	Military		160	150	110	110	110
Maximum Standby Current (mA)		40	40	40	35	35	35

Shaded area contains advanced information.

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature - 65°C to +150°C

Ambient Temperature with

Power Applied - 55°C to +125°C

Supply Voltage to Ground Potential

(Pin 24 to Pin 12) - 0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State - 0.5V to +7.0V

DC Input Voltage - 3.0V to +7.0V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[1]	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	- 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[2]

Parameters	Description	Test Conditions	7C197-12		7C197-15		Units
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 12.0 mA				0.4	V
		I _{OL} = 8.0 mA				0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		- 0.5	0.8	- 3.0	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	- 10	+ 10	- 10	+ 10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	- 10	+ 10	- 10	+ 10	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		- 350		- 350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		160		150	mA
						160	
I _{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs ^[4]	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		40		40	mA
I _{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs ^[4]	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} < 0.3V		20		20	mA

Shaded area contains advanced information.

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Electrical Characteristics Over the Operating Range^[2] (continued)

Parameters	Description	Test Conditions	7C197-20		7C197-20, 25, 35, 45		Units
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
		I _{OL} = 12.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		- 0.5	0.8	- 3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	- 10	+ 10	- 10	+ 10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	- 10	+ 10	- 10	+ 10	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		- 350		- 350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com'l	140		100	mA
			Mil	150		110	
I _{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs ^[4]	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		40		35	mA
I _{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs ^[4]	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} < 0.3V		20		20	mA

Shaded area contains advanced information.

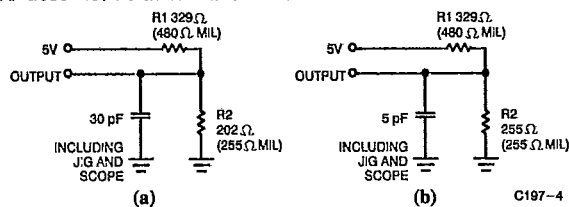
Capacitance^[5]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

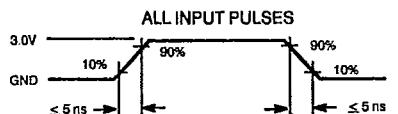
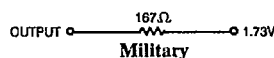
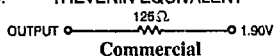
Notes:

5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT



C197-5

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Switching Characteristics Over the Operating Range^[2,6]

Parameters	Description	7C197-12		7C197-15		7C197-20		7C197-25		7C197-35		7C197-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t _{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t _{AA}	Address to Data Valid		12		15		20		25		35		45	ns
t _{OHA}	Output Hold from Address Change	3		3		3		3		3		3		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35		45	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[7]	3		3		3		3		3		3		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[7, 8]		7		8	0	10	0	13	0	15	0	20	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		20		25		30	ns
WRITE CYCLE ^[9]														
t _{WC}	Write Cycle Time	12		15		20		25		35		45		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	9		10		15		20		30		40		ns
t _{AW}	Address Set-Up to Write End	9		10		15		20		30		40		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	9		10		15		20		25		30		ns
t _{SD}	Data Set-Up to Write End	7		8		10		15		17		20		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[7]	2		2		3		3		3		3		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[7, 8]		7		7	0	10	0	13	0	15	0	20	ns

Shaded area contains advanced information.

Notes:

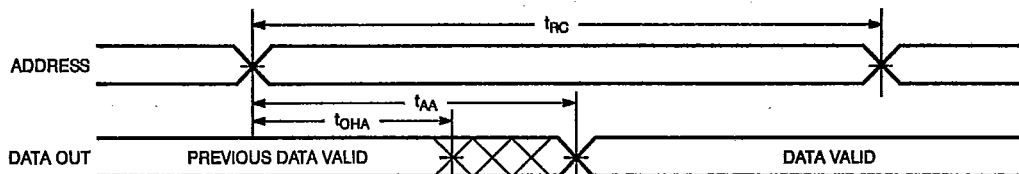
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads and Waveforms. Transition is measured ± 500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.



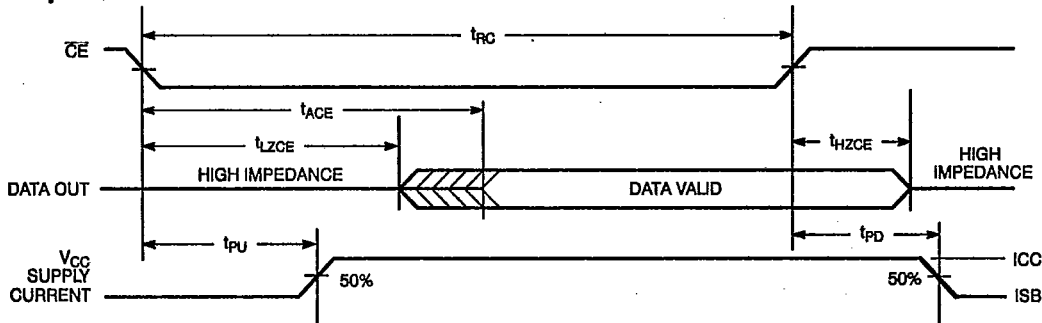
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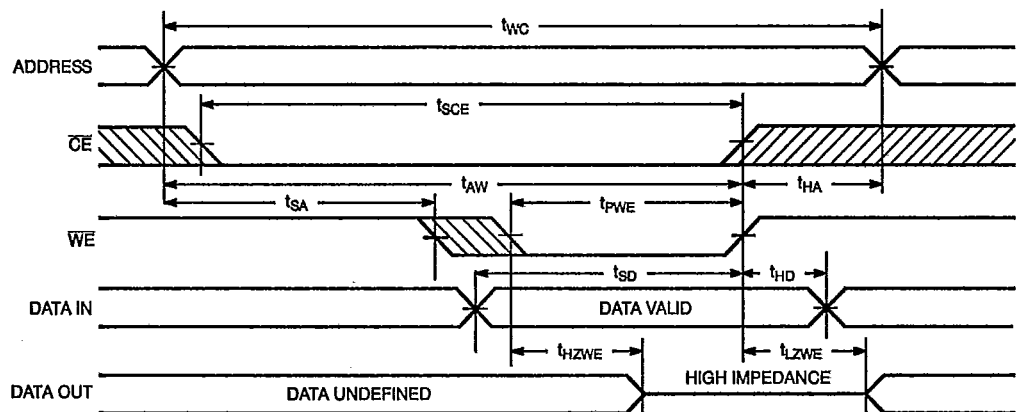
Switching Waveforms

Read Cycle No. 1^[10, 11]

C197-6

Read Cycle No. 2^[11]

C197-7

Write Cycle No. 1 ($\overline{WE}$ Controlled)^[10]

C197-8

Notes:

10. $\overline{WE}$ is HIGH for read cycle.11. Device is continuously selected, $\overline{CE} = V_{IL}$.12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

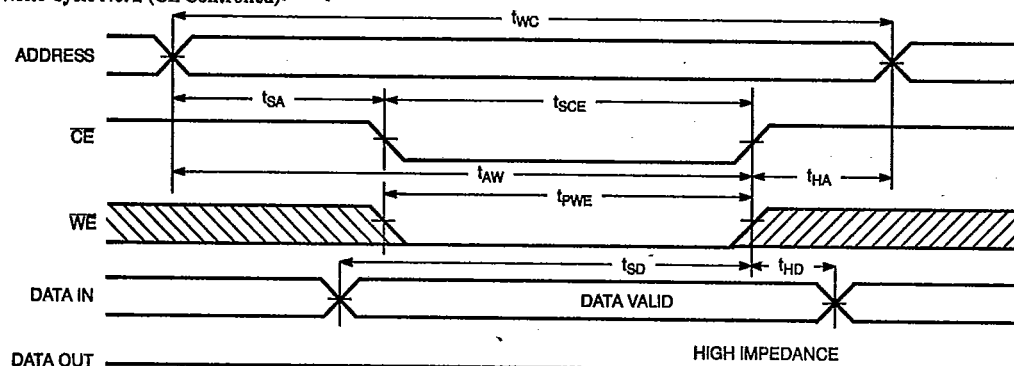
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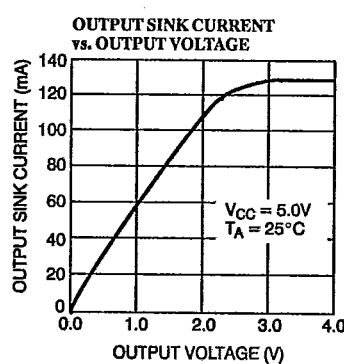
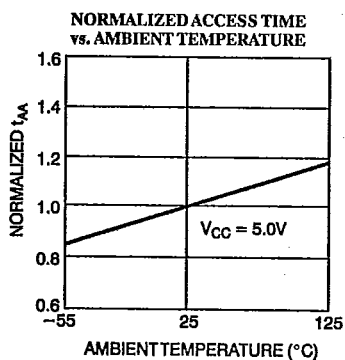
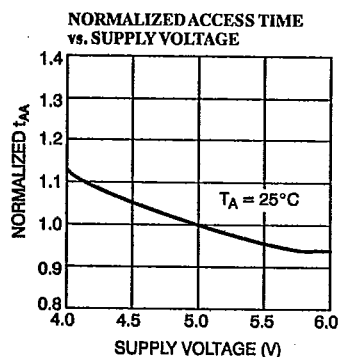
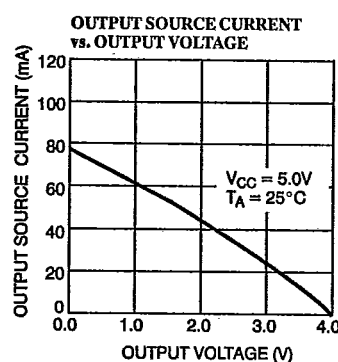
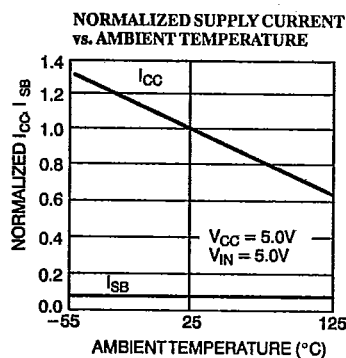
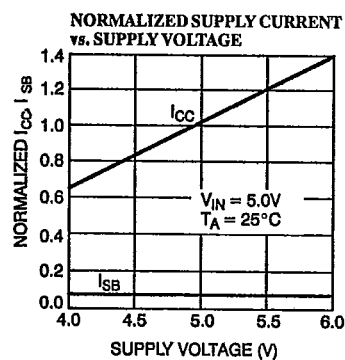
Switching Waveforms (continued)

Write Cycle No. 2 (CE Controlled)[10, 12]



C197-9

Typical DC and AC Characteristics

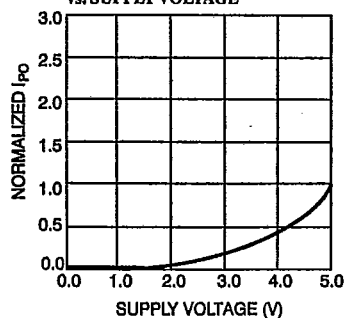
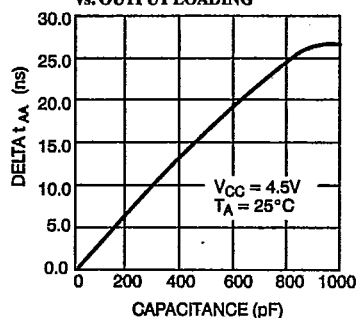
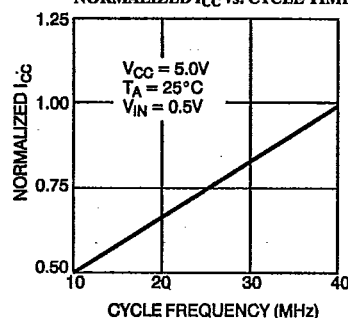


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Typical DC and AC Characteristics (continued)

TYPICAL POWER-ON CURRENT
vs. SUPPLY VOLTAGETYPICAL ACCESS TIME CHANGE
vs. OUTPUT LOADINGNORMALIZED I_{CC} vs. CYCLE TIME

SRAMS

7C197 Truth Table

CE	WE	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

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Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C197-12DC	D14	Commercial
	CY7C197-12LC	L54	
	CY7C197-12PC	P13	
	CY7C197-12VC	V13	
15	CY7C197-15DC	D14	Commercial
	CY7C197-15LC	L54	
	CY7C197-15PC	P13	
	CY7C197-15VC	V13	
	CY7C197-15DMB	D14	Military
	CY7C197-15KMB	K73	
	CY7C197-15LMB	L54	
20	CY7C197-20PC	P13	Commercial
	CY7C197-20VC	V13	
	CY7C197-20DMB	D14	Military
	CY7C197-20KMB	K73	
	CY7C197-20LMB	L54	
25	CY7C197-25DC	D14	Commercial
	CY7C197-25LC	L54	
	CY7C197-25PC	P13	
	CY7C197-25VC	V13	
	CY7C197-25DMB	D14	Military
	CY7C197-25KMB	K73	
	CY7C197-25LMB	L54	
35	CY7C197-35DC	D14	Commercial
	CY7C197-35LC	L54	
	CY7C197-35PC	P13	
	CY7C197-35VC	V13	
	CY7C197-35DMB	D14	Military
	CY7C197-35KMB	K73	
	CY7C197-35LMB	L54	
45	CY7C197-45DC	D14	Commercial
	CY7C197-45LC	L54	
	CY7C197-45PC	P13	
	CY7C197-45VC	V13	
	CY7C197-45DMB	D14	Military
	CY7C197-45KMB	K73	
	CY7C197-45LMB	L54	

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MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{OS}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

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