BLP7G22-05

LDMOS driver transistor

Rev. 2 — 20 August 2013 Product data sheet

1. Product profile

1.1 General description

A 5 W plastic LDMOS power transistor for base station applications from 700 MHz to 2700 MHz band.

Table 1. Application information

Typical RF performance at T_{case} = 25 °C; in a class-AB application circuit.

Test signal	f (MHz)	I_{Dq} (mA)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
IS-95 [1]	788	60	28	1	23.9	25	–41
2-carrier W-CDMA [2]	2140	55	28	1	16.7	27	–40
Pulsed CW	2700	55	28	5	14.5	45	-

[1] Single carrier IS-95 with pilot, paging, sync and 6 traffic channels (Walsh codes 8 - 13). PAR = 9.7 dB at 0.01 % probability on the CCDF. Channel bandwidth is 1.2288 MHz.

[2] Test signal: 2-carrier W-CDMA: carrier spacing = 5 MHz. PAR = 8.4 dB at 0.01% probability on CCDF; RF performance at V_{DS} = 28 V; I_{Dq} = 55 mA.

1.2 Features and benefits

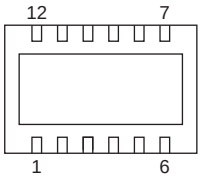
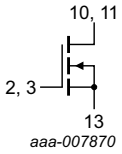
- High efficiency
- Excellent ruggedness
- Designed for broadband operation
- Excellent thermal stability
- High power gain
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- CDMA
- W-CDMA
- GSM EDGE
- MC-GSM
- LTE
- WiMAX

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1, 4, 5, 6, 7, 8, 9, 12	n.c.	 Transparent top view	
2, 3	gate		
10, 11	drain		
13	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP7G22-05	HVSON12	plastic thermal enhanced very thin small outline package; no leads; 12 terminals; body 6 × 4 × 0.85 mm	SOT1179-2

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		−0.5	+13	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		-	150	°C

5. Recommended operating conditions

See application note *AN11198* for more details.

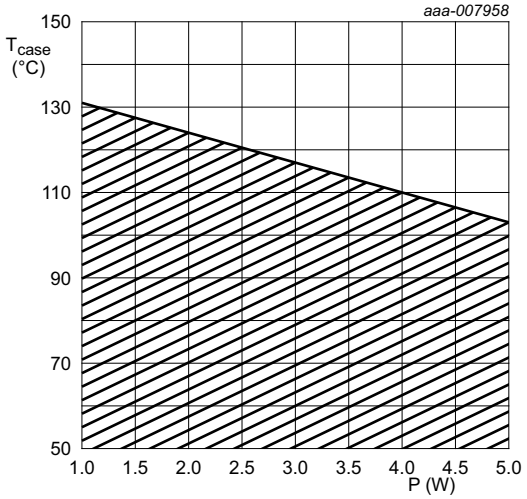


Fig 1. Recommended operating area; case temperature as a function of power dissipation

6. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 5 W	[1]	6.4	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions.

7. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.09 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 9 mA	1.5	1.9	2.3	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 55 mA	1.45	2.0	2.55	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	1.6	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 9 mA	-	80	-	mS
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 315 mA	-	2	-	Ω

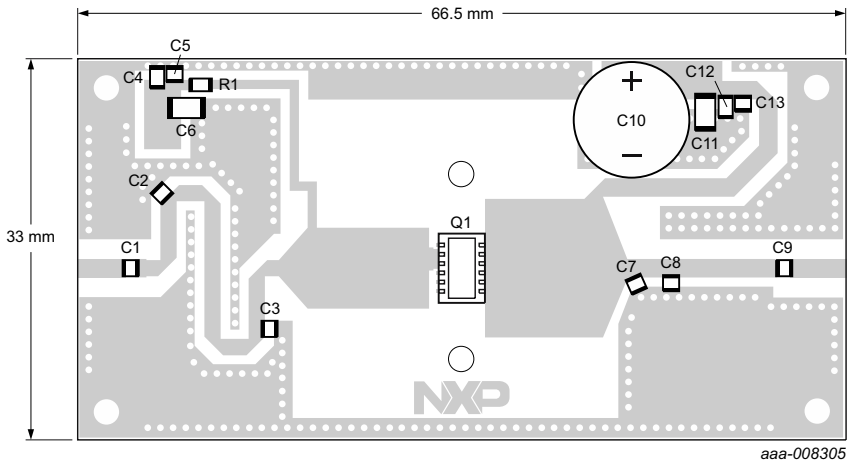
Table 7. RF characteristics

Test signal: 1-tone pulsed; t_p = 50 μs; δ = 10 %; f = 2140 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 55 mA; T_{case} = 25 °C; unless otherwise specified, in a production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 1 W	15	16	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 1 W	20	23	-	%
$P_{L(1dB)}$	output power at 1 dB gain compression		5.5	-	-	W
RL_{in}	input return loss	$P_{L(AV)}$ = 1 W	-	−16	−12	dB

8. Application information

8.1 Application circuit



Printed-Circuit Board (PCB): Rogers RO4350; ε_r = 3.48; thickness = 0.762 mm; thickness copper plating = 35 μm.

See Table 8 for list of components.

Fig 2. Component layout

Table 8. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C9	multilayer ceramic chip capacitor	15 pF	[1]
C2	multilayer ceramic chip capacitor	1.8 pF	[1]
C3	multilayer ceramic chip capacitor	1.6 pF	[1]
C4, C12	multilayer ceramic chip capacitor	100 nF, 50 V	[2]
C5, C13	multilayer ceramic chip capacitor	10 pF	[1]
C6, C11	multilayer ceramic chip capacitor	1 μF, 50 V	[2]
C7	multilayer ceramic chip capacitor	3.0 pF	[1]
C8	multilayer ceramic chip capacitor	1.6 pF	[1]

Table 8. List of components *...continued*

See Figure 2 for component layout.

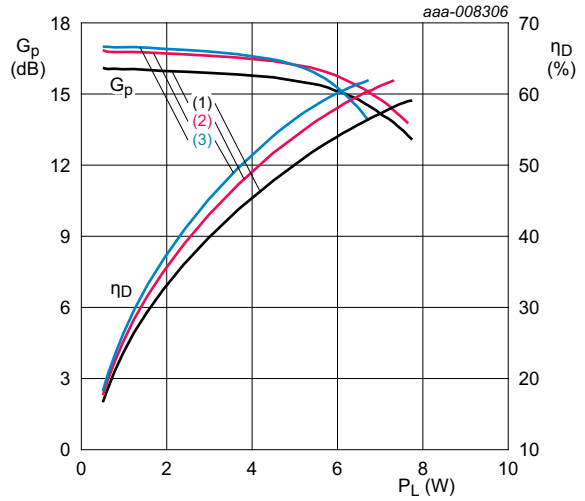
Component	Description	Value	Remarks
C10	electrolytic capacitor	220 μF, 63 V	
R1	chip resistor	4.7 Ω	SMD 0805
Q1	transistor	-	BLP7G22-05

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] Murata GRM32RR71H05KA01L or capacitor of same quality.

8.2 Graphical data

8.2.1 Pulsed CW



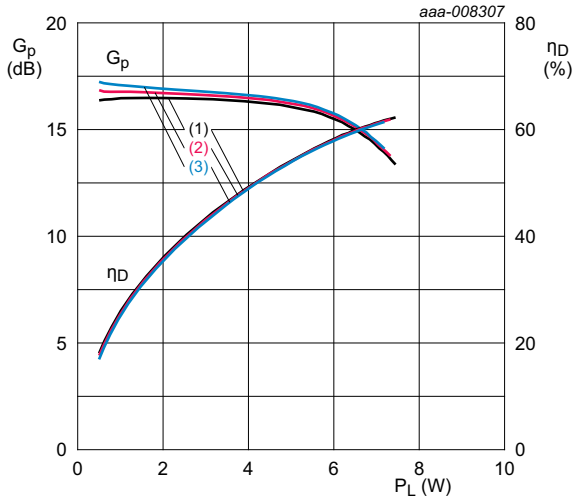
V_{DS} = 28 V; I_{Dq} = 50 mA; T_{case} = 25 °C; δ = 10 %; t_p = 20 μs.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; f = 2140 MHz; T_{case} = 25 °C; δ = 10 %; t_p = 20 μs.

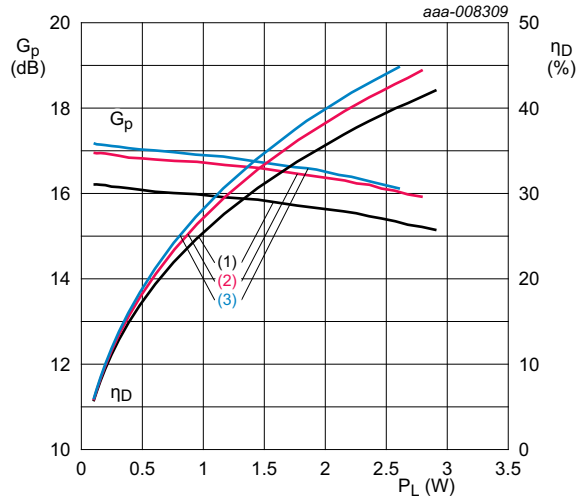
(1) I_{Dq} = 40 mA

(2) I_{Dq} = 50 mA

(3) I_{Dq} = 60 mA

Fig 4. Power gain and drain efficiency as function of output power; typical values

8.2.2 2-Carrier W-CDMA



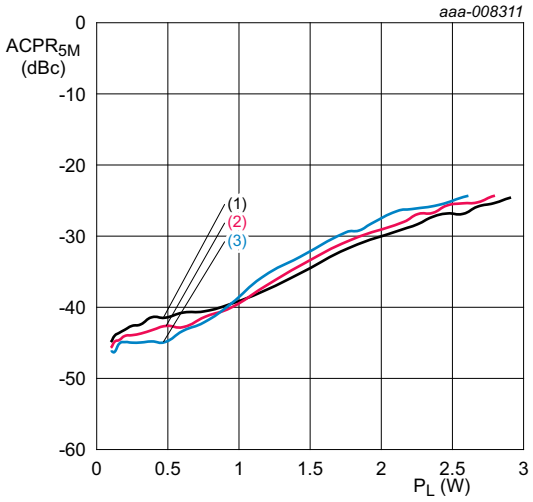
V_{DS} = 28 V; I_{Dq} = 50 mA; T_{case} = 25 °C;
carrier spacing = 5 MHz; 46 % clipping; PAR = 8.4 dB at 0.01 % probability on CCDF.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 50 mA; T_{case} = 25 °C;
carrier spacing = 5 MHz; 46 % clipping; PAR = 8.4 dB at 0.01 % probability on CCDF.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

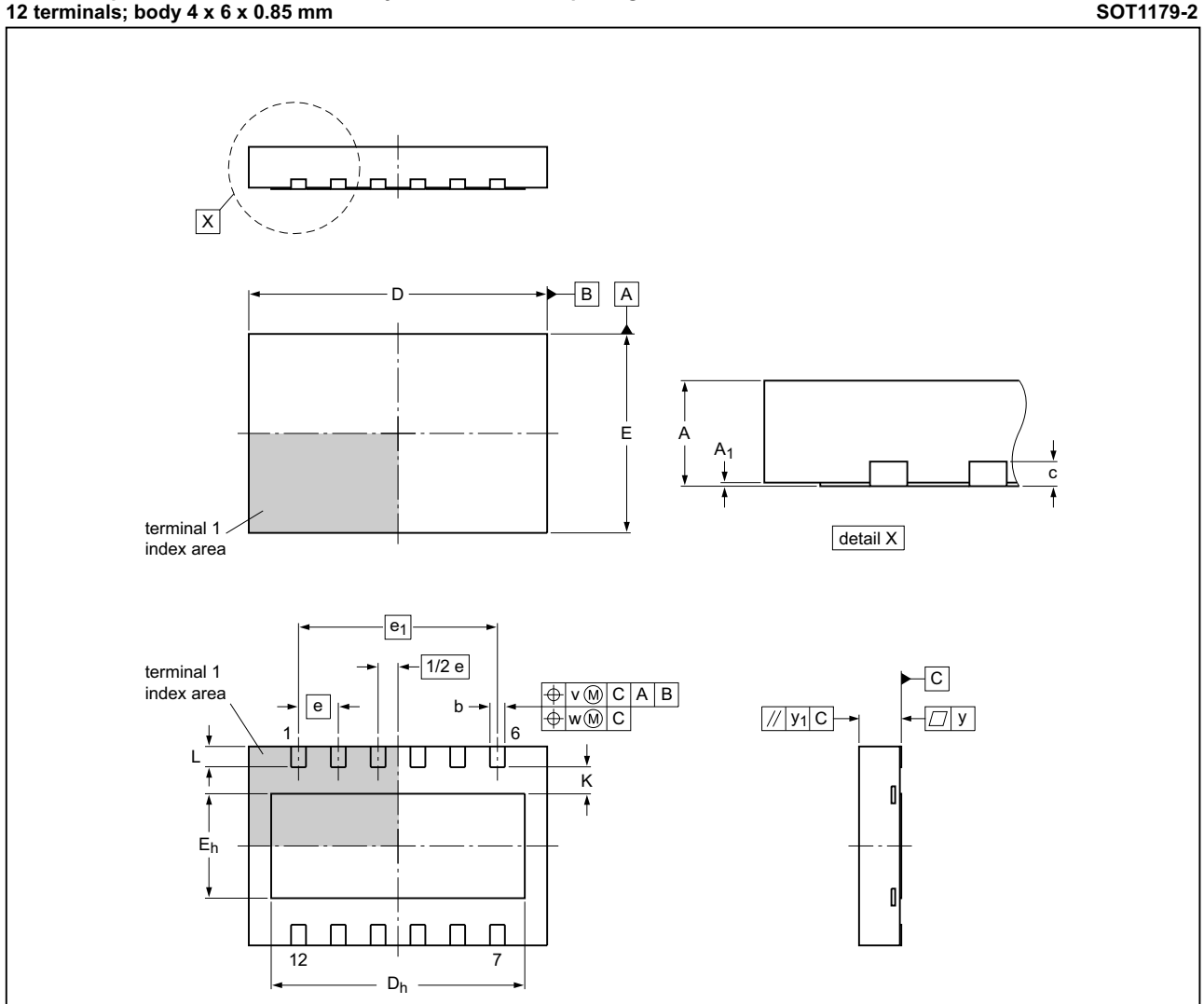
9. Test information

9.1 Ruggedness in class-AB operation

The BLP7G22-05 is capable of withstanding a load mismatch corresponding to VSWR = 10: 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 55 mA; P_L = 5 W (CW).

10. Package outline

HVSON12: plastic thermal enhanced very thin small outline package; no leads; 12 terminals; body 4 x 6 x 0.85 mm **SOT1179-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	K	L	v	w	y	y_1
	max	1.00	0.05	0.35		6.1	5.2	4.1	2.2				0.5				
mm	nom	0.85	0.03	0.30	0.2	6.0	5.1	4.0	2.1	0.8	4		0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.25		5.9	5.0	3.9	2.0			0.5	0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1179-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1179-2	- - -	MO-229	- - -			~~13-02-26~~ 13-07-16

Fig 7. Package outline SOT1179-2 (HVSON12)

11. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

12. Abbreviations

Table 9. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
CDMA	Code Division Multiple Access
CW	Continuous Wave
EDGE	Enhanced Data rates for GSM Evolution
ESD	ElectroStatic Discharge
GSM	Global System for Mobile Communication
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LTE	Long Term Evolution
MC-GSM	Multi Carrier GSM
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access

13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP7G22-05 v.2	20130820	Product data sheet	-	BLP7G22-05 v.1
Modifications	• Table 1 on page 1: table has been updated • Section 5 on page 3: text ‘See application note AN11198 for more details’ has been added • Table 6 on page 3: value $R_{DS(on)}$ has been changed to 2 • Section 8 on page 4: section ‘Application information’ has been added			
BLP7G22-05 v.1	20130528	Objective data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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