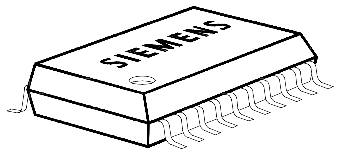
Smart Two Channel Highside Power Switch

Features

- Overload protection
- Current limitation
- Short-circuit protection
- Thermal shutdown
- Overvoltage protection (including load dump)
- Fast demagnetization of inductive loads
- Reverse battery protection[1)]
- Undervoltage and overvoltage shutdown with auto-restart and hysteresis
- Open drain diagnostic output
- Open load detection in ON-state
- CMOS compatible input
- Loss of ground and loss of V_{bb} protection
- **E**lectro**s**tatic **d**ischarge (**ESD**) protection

Product Summary

Overvoltage Protection	$V_{bb(AZ)}$		43	V
Operating voltage	$V_{bb(on)}$		5.0 ... 34	V
active channels:		one	two parallel	
On-state resistance	R_{ON}	40	20	mΩ
Nominal load current	$I_{L(NOM)}$	4.8	7.3	A
Current limitation	$I_{L(SCr)}$	19	19	A



Application

- µC compatible power switch with diagnostic feedback for 12 V and 24 V DC grounded loads
- All types of resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits

General Description

N channel vertical power FET with charge pump, ground referenced CMOS compatible input and diagnostic feedback, monolithically integrated in Smart SIPMOS® technology. Fully protected by embedded protection functions.

Pin Definitions and Functions

Pin	Symbol	Function
1,10, 11,12, 15,16, 19,20	V_{bb}	**Positive power supply voltage**. Design the wiring for the simultaneous max. short circuit currents from channel 1 to 2 and also for low thermal resistance
3	IN1	**Input 1,2**, activates channel 1,2 in case of logic high signal
7	IN2	
17,18	OUT1	**Output 1,2**, protected high-side power output of channel 1,2. Design the wiring for the max. short circuit current
13,14	OUT2	
4	ST1	**Diagnostic feedback 1,2** of channel 1,2, open drain, low on failure
8	ST2	
2	GND1	**Ground 1** of chip 1 (channel 1)
6	GND2	**Ground 2** of chip 2 (channel 2)
5,9	N.C.	**Not Connected**

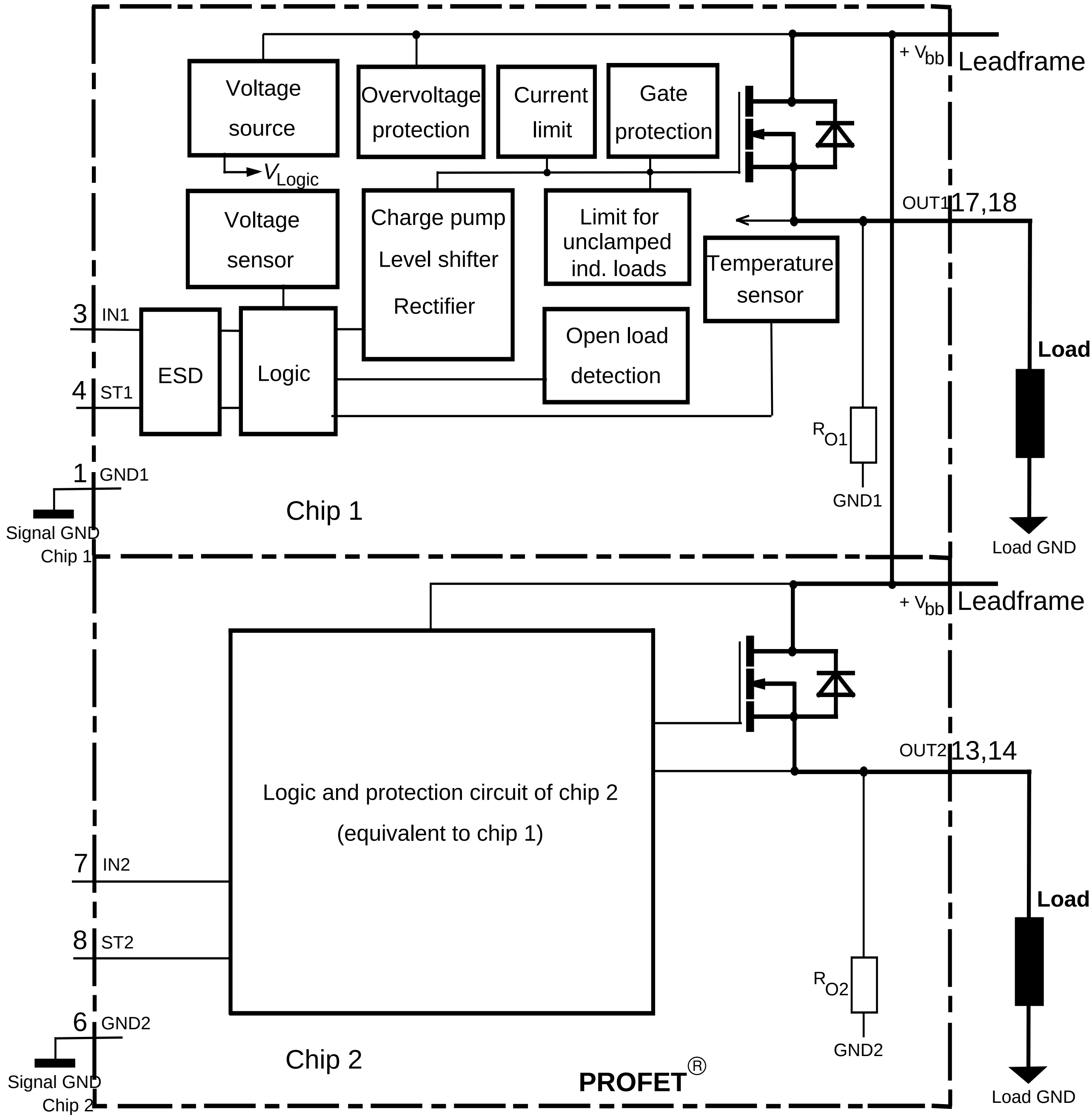
Pin configuration (top view)

V_{bb}	1	20	V_{bb}
GND1	2	19	V_{bb}
IN1	3	18	OUT1
ST1	4	17	OUT1
N.C.	5	16	V_{bb}
GND2	6	15	V_{bb}
IN2	7	14	OUT2
ST2	8	13	OUT2
N.C.	9	12	V_{bb}
V_{bb}	10	11	V_{bb}

1) With external current limit (e.g. resistor R_{GND}=150 Ω) in GND connection, resistor in series with ST connection, reverse load current limited by connected load.

Block diagram

Two Channels; Open Load detection in on state;



Leadframe connected to pin 1, 10, 11, 12, 15, 16, 19, 20

Maximum Ratings at T_j = 25°C unless otherwise specified

Parameter	Symbol	Values	Unit
Supply voltage (overvoltage protection see page 4)	V_{bb}	43	V
Supply voltage for full short circuit protection $T_{j,start}$ =-40 ...+150°C	V_{bb}	34	V

Maximum Ratings at T_j = 25°C unless otherwise specified

Parameter	Symbol	Values	Unit
Load current (Short-circuit current, see page 5)	I_L	self-limited	A
Load dump protection[2] $V_{LoadDump} = U_A + V_s$, U_A = 13.5 V R_I[3] = 2 Ω, t_d = 200 ms; IN = low or high, each channel loaded with R_L = 2.8 Ω,	$V_{Load\,dump}$[4]	60	V
Operating temperature range	T_j	-40 ...+150	°C
Storage temperature range	T_{stg}	-55 ...+150	
Power dissipation (DC)[5] T_a = 25°C:	P_{tot}	3.8	W
(all channels active) T_a = 85°C:		2.0	
Inductive load switch-off energy dissipation, single pulse V_{bb} = 12V, $T_{j,start}$ = 150°C[5],			
I_L = 4.8 A, Z_L = 44 mH, 0 Ω one channel:	E_{AS}	0.65	J
I_L = 7.3 A, Z_L = 44 mH, 0 Ω two parallel channels:		1.5	
see diagrams on page 10			
Electrostatic discharge capability (ESD) (Human Body Model)	V_{ESD}	1.0	kV
Input voltage (DC)	V_{IN}	-10 ... +16	V
Current through input pin (DC)	I_{IN}	±2.0	mA
Current through status pin (DC)	I_{ST}	±5.0	
see internal circuit diagram page 8			

Thermal Characteristics

Parameter and Conditions	Symbol	Values			Unit
		min	typ	max	
Thermal resistance					
junction - soldering point[5),6)] each channel:	R_{thjs}	--	--	11	K/W
junction - ambient[5] one channel active:	R_{thja}	--	40	--	
all channels active:		--	33	--	

2) Supply voltages higher than $V_{bb(AZ)}$ require an external current limit for the GND and status pins, e.g. with a 150 Ω resistor in the GND connection and a 15 kΩ resistor in series with the status pin. A resistor for input protection is integrated.

3) R_I = internal resistance of the load dump test pulse generator

4) $V_{Load\,dump}$ is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

5) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm^2 (one layer, 70µm thick) copper area for V_{bb} connection. PCB is vertical without blown air. See page 16

6) Soldering point: upper side of solder edge of device pin 15. See page 16

Electrical Characteristics

Parameter and Conditions, each of the two channels at T_j = 25 °C, V_{bb} = 12 V unless otherwise specified	**Symbol**	**Values** min	typ	max	**Unit**
Load Switching Capabilities and Characteristics					
On-state resistance (V_{bb} to OUT) I_L = 2 A each channel, T_j = 25°C:	R_{ON}	--	36	40	mΩ
T_j = 150°C:			67	75	
two parallel channels, T_j = 25°C:			18	20	
Nominal load current one channel active:	$I_{L(NOM)}$	4.4	4.8	--	A
two parallel channels active:		6.7	7.3		
Device on PCB[5], T_a = 85°C, $T_j \leq$ 150°C					
Output current while GND disconnected or pulled up; V_{bb} = 30 V, V_{IN} = 0, see diagram page 9	$I_{L(GNDhigh)}$	--	--	10	mA
Turn-on time[7] IN ⌐ to 90% V_{OUT}:	t_{on}	80	180	350	µs
Turn-off time IN ¬ to 10% V_{OUT}:	t_{off}	80	250	450	
R_L = 12 Ω, T_j =-40...+150°C					
Slew rate on[7] 10 to 30% V_{OUT}, R_L = 12 Ω, T_j =-40...+150°C:	dV/dt$_{on}$	0.1	--	1	V/µs
Slew rate off[7] 70 to 40% V_{OUT}, R_L = 12 Ω, T_j =-40...+150°C:	-dV/dt$_{off}$	0.1	--	1	V/µs
Operating Parameters					
Operating voltage[8] T_j =-40...+150°C:	$V_{bb(on)}$	5.0	--	34	V
Undervoltage shutdown T_j =-40...+150°C:	$V_{bb(under)}$	3.5	--	5.0	V
Undervoltage restart T_j =-40...+25°C:	$V_{bb(u\ rst)}$	--	--	5.0	V
T_j =+150°C:				7.0	
Undervoltage restart of charge pump see diagram page 14 T_j =-40...+150°C:	$V_{bb(ucp)}$	--	5.6	7.0	V
Undervoltage hysteresis $\Delta V_{bb(under)} = V_{bb(u\ rst)} - V_{bb(under)}$	$\Delta V_{bb(under)}$	--	0.2	--	V
Overvoltage shutdown T_j =-40...+150°C:	$V_{bb(over)}$	34	--	43	V
Overvoltage restart T_j =-40...+150°C:	$V_{bb(o\ rst)}$	33	--	--	V
Overvoltage hysteresis T_j =-40...+150°C:	$\Delta V_{bb(over)}$	--	0.5	--	V
Overvoltage protection[9] T_j =-40...+150°C: I_{bb} = 40 mA	$V_{bb(AZ)}$	42	47	--	V
Standby current, all channels off T_j =25°C:	$I_{bb(off)}$	--	16	40	µA
V_{IN} = 0 T_j =150°C:		--	24	50	

7) See timing diagram on page 12.
8) At supply voltage increase up to V_{bb} = 5.6 V typ without charge pump, $V_{OUT} \approx V_{bb}$ - 2 V
9) see also $V_{ON(CL)}$ in circuit diagram on page 8.

Parameter and Conditions, each of the two channels at T_j = 25 °C, V_{bb} = 12 V unless otherwise specified	Symbol	Values min	typ	max	Unit
Leakage output current (included in $I_{bb(off)}$) $V_{IN} = 0$	$I_{L(off)}$	--	--	20	µA
Operating current [10], $V_{IN} = 5V$, T_j =-40...+150°C $I_{GND} = I_{GND1} + I_{GND2}$, one channel on:	I_{GND}	--	1.8	4	mA
two channels on:		--	3.6	8	

Protection Functions

Parameter and Conditions	Symbol	min	typ	max	Unit
Initial peak short circuit current limit, (see timing diagrams, page 13) each channel, T_j =-40°C:	$I_{L(SCp)}$	47	55	66	A
T_j =25°C:		35	44	54	
T_j =+150°C:		21	26	34	
two parallel channels	twice the current of one channel				
Repetitive short circuit current limit, $T_j = T_{jt}$ each channel	$I_{L(SCr)}$	--	19	--	A
two parallel channels (see timing diagrams, page 13)		--	19	--	
Initial short circuit shutdown time $T_{j,start}$ =-40°C:	$t_{off(SC)}$	--	3	--	ms
$T_{j,start}$ = 25°C: (see page 11 and timing diagrams on page 13)		--	2.5	--	
Output clamp (inductive load switch off)[11] at $V_{ON(CL)} = V_{bb} - V_{OUT}$	$V_{ON(CL)}$	41	47	--	V
Thermal overload trip temperature	T_{jt}	150	--	--	°C
Thermal hysteresis	ΔT_{jt}	--	10	--	K

Reverse Battery

Parameter and Conditions	Symbol	min	typ	max	Unit
Reverse battery voltage [12]	$-V_{bb}$	--	--	32	V
Drain-source diode voltage ($V_{out} > V_{bb}$) $I_L = -4.8$ A, $T_j = +150$°C	$-V_{ON}$	--	600	--	mV

10) Add I_{ST}, if $I_{ST} > 0$

11) If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest $V_{ON(CL)}$

12) Requires a 150 Ω resistor in GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Power dissipation is higher compared to normal operating conditions due to the voltage drop across the drain-source diode. The temperature protection is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 3 and circuit page 8).

Parameter and Conditions, each of the two channels at T_j = 25 °C, V_{bb} = 12 V unless otherwise specified	Symbol	Values min	Values typ	Values max	Unit
Diagnostic Characteristics					
Open load detection current, (on-condition) each channel, T_j = -40°C:	$I_{L\ (OL)}$	20	--	1050	mA
T_j = 25°C:		20	--	800	
T_j = 150°C:		20	--	800	
two parallel channels	twice the current of one channel				
Open load detection voltage[13] T_j =-40..+150°C:	$V_{OUT(OL)}$	2	3	4	V
Internal output pull down (OUT to GND), V_{OUT} = 5 V T_j =-40..+150°C:	R_O	4	10	30	kΩ

Input and Status Feedback[14]

Parameter and Conditions	Symbol	min	typ	max	Unit
Input resistance (see circuit page 8)	R_I	2.5	3.5	6	kΩ
Input turn-on threshold voltage T_j =-40..+150°C:	$V_{IN(T+)}$	1.7	--	3.3	V
Input turn-off threshold voltage T_j =-40..+150°C:	$V_{IN(T-)}$	1.5	--	--	V
Input threshold hysteresis	$\Delta\ V_{IN(T)}$	--	0.5	--	V
Off state input current V_{IN} = 0.4 V: T_j =-40..+150°C:	$I_{IN(off)}$	1	--	50	µA
On state input current V_{IN} = 5 V: T_j =-40..+150°C:	$I_{IN(on)}$	20	50	90	µA
Delay time for status with open load after switch off (see timing diagrams, page 13), T_j =-40..+150°C:	$t_{d(ST\ OL4)}$	100	520	1000	µs
Status invalid after positive input slope (open load) T_j =-40..+150°C:	$t_{d(ST)}$	--	250	600	µs
Status output (open drain) Zener limit voltage T_j =-40...+150°C, I_{ST} = +1.6 mA:	$V_{ST(high)}$	5.4	6.1	--	V
ST low voltage T_j =-40...+25°C, I_{ST} = +1.6 mA:	$V_{ST(low)}$	--	--	0.4	
T_j = +150°C, I_{ST} = +1.6 mA:		--	--	0.6	

13) External pull up resistor required for open load detection in off state.

14) If ground resistors R_{GND} are used, add the voltage drop across these resistors.

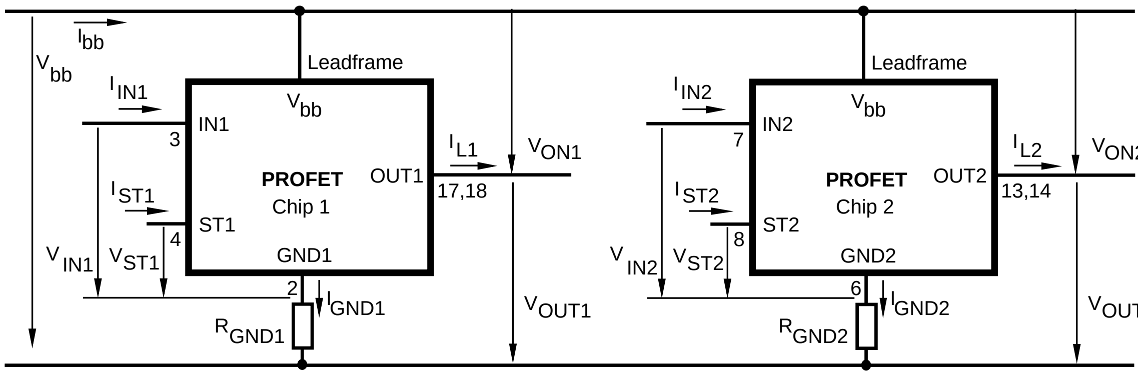
Truth Table

Channel 1	Input 1	Output 1	Status 1
Channel 2	Input 2	Output 2	Status 2
	level	level	BTS 734L1
Normal operation	L H	L H	H H
Open load	L H	Z H	H (L[15]) L
Short circuit to V_{bb}	L H	H H	L[16] H (L[17])
Overtem-perature	L H	L L	H L
Under-voltage	L H	L L	H H
Overvoltage	L H	L L	H H

L = "Low" Level X = don't care Z = high impedance, potential depends on external circuit
H = "High" Level Status signal valid after the time delay shown in the timing diagrams

Parallel switching of channel 1 and 2 is easily possible by connecting the inputs and outputs in parallel. The status outputs ST1 and ST2 have to be configured as a 'Wired OR' function with a single pull-up resistor.

Terms



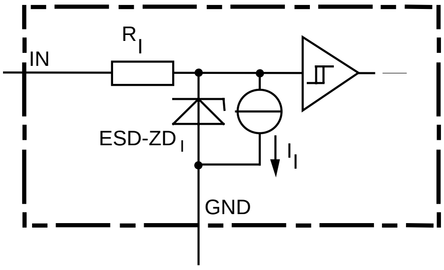
Leadframe (V_{bb}) is connected to pin 1,10,11,12,15,16,19,20
External R_{GND} optional; two resistors R_{GND1}, R_{GND2} = 150 Ω or a single resistor R_{GND} = 75 Ω for reverse battery protection up to the max. operating voltage.

15) With external resistor between output and V_{bb}

16) An external short of output to V_{bb} in the off state causes an internal current from output to ground. If R_{GND} is used, an offset voltage at the GND and ST pins will occur and the $V_{ST\ low}$ signal may be errorious.

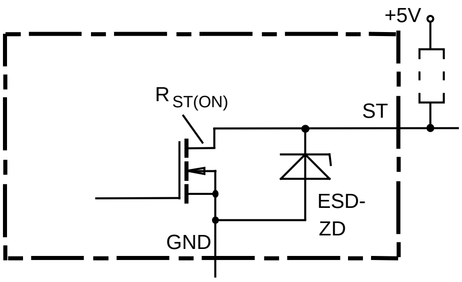
17) Low resistance to V_{bb} may be detected by no-load-detection

Input circuit (ESD protection), IN1 or IN2



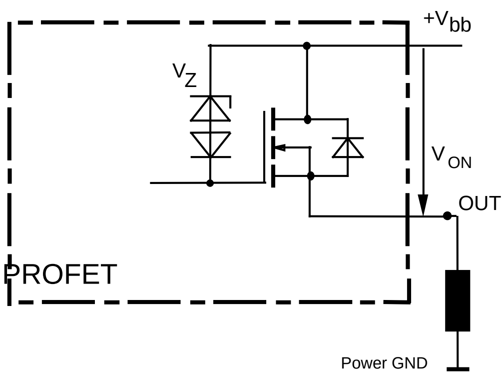
ESD zener diodes are not to be used as voltage clamp at DC conditions. Operation in this mode may result in a drift of the zener voltage (increase of up to 1 V).

Status output, ST1 or ST2



ESD-Zener diode: 6.1 V typ., max 5.0 mA; $R_{ST(ON)}$ < 375 Ω at 1.6 mA, ESD zener diodes are not to be used as voltage clamp at DC conditions. Operation in this mode may result in a drift of the zener voltage (increase of up to 1 V).

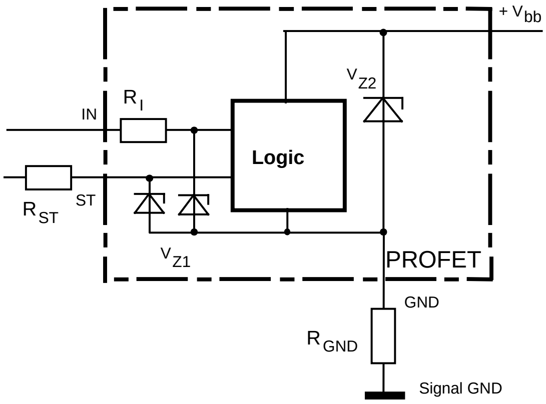
Inductive and overvoltage output clamp, OUT1 or OUT2



V_{ON} clamped to $V_{ON(CL)}$ = 47 V typ.

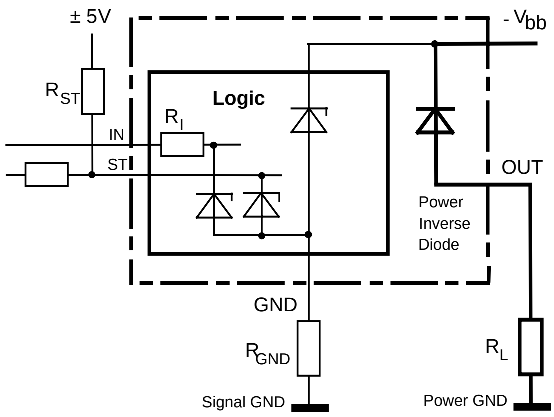
Overvoltage protection of logic part

GND1 or GND2



V_{Z1} = 6.1 V typ., V_{Z2} = 47 V typ., R_I = 3.5 kΩ typ., R_{GND} = 150 Ω, R_{ST} = 15 kΩ nominal.

Reverse battery protection



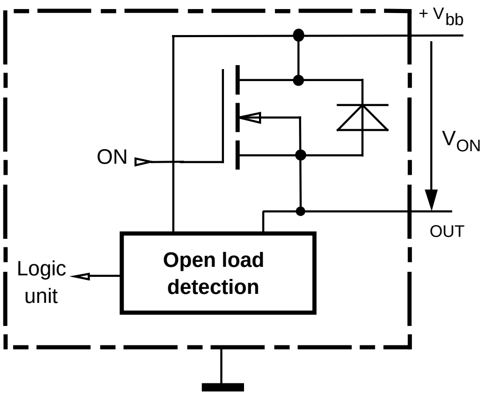
R_{GND} = 150 Ω, R_I = 3.5 kΩ typ,

Temperature protection is not active during inverse current operation.

Open-load detection, OUT1 or OUT2

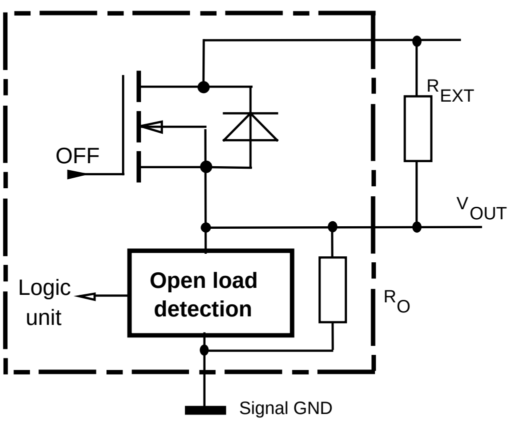
ON-state diagnostic condition:

$V_{ON} < R_{ON} \cdot I_{L(OL)}$; IN high

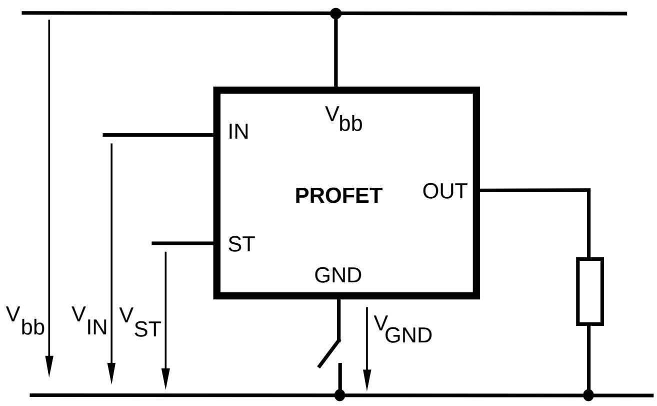


OFF-state diagnostic condition:

$V_{OUT} > 3$ V typ.; IN low

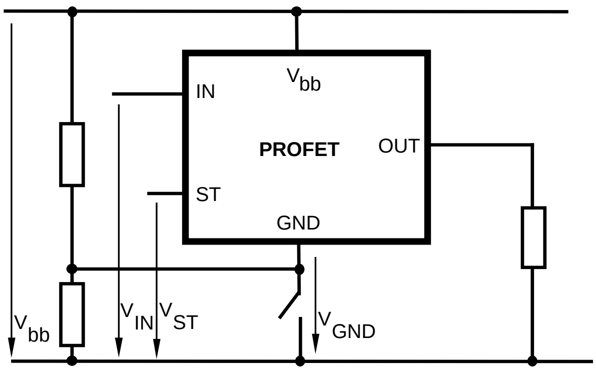


GND disconnect



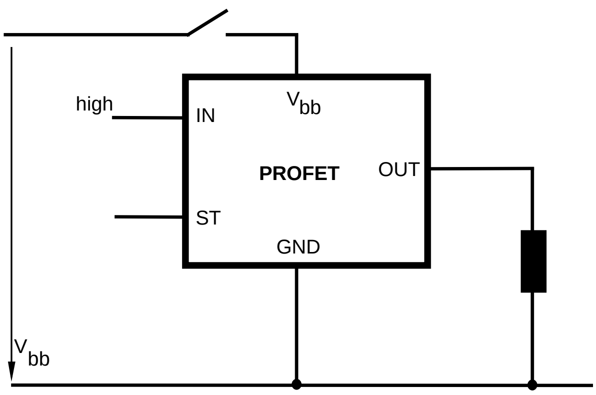
Any kind of load. In case of IN = high is $V_{OUT} \approx V_{IN} - V_{IN(T+)}$.
Due to $V_{GND} > 0$, no V_{ST} = low signal available.

GND disconnect with GND pull up



Any kind of load. If $V_{GND} > V_{IN} - V_{IN(T+)}$ device stays off
Due to $V_{GND} > 0$, no V_{ST} = low signal available.

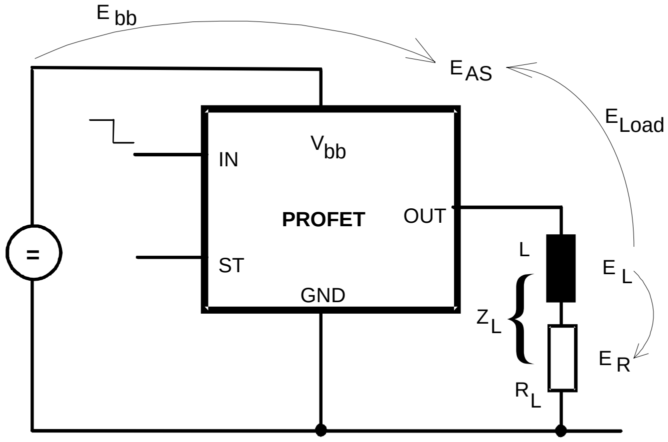
V_{bb} disconnect with energized inductive load



For inductive load currents up to the limits defined by E_{AS} (max. ratings and diagram on page 10) each switch is protected against loss of V_{bb}.

Consider at your PCB layout that in the case of Vbb dis-connection with energized inductive load all the load current flows through the GND connection.

Inductive load switch-off energy dissipation



Energy stored in load inductance:

$$E_L = {}^{1}/_{2} \cdot L \cdot I_L^2$$

While demagnetizing load inductance, the energy dissipated in PROFET is

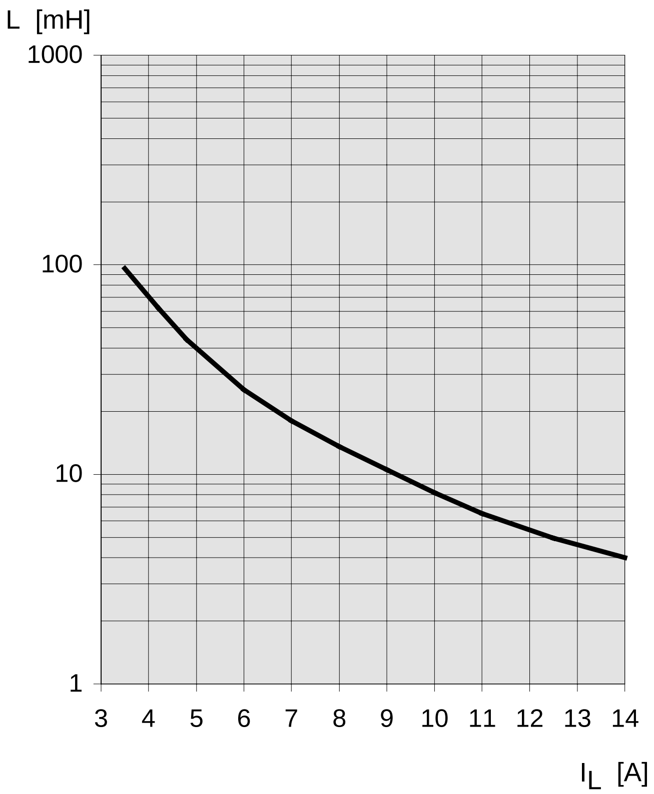
$$E_{AS} = E_{bb} + E_L - E_R = \int V_{ON(CL)} \cdot i_L(t)\, dt,$$

with an approximate solution for $R_L > 0\,\Omega$:

$$E_{AS} = \frac{I_L \cdot L}{2 \cdot R_L} \left(V_{bb} + |V_{OUT(CL)}| \right) \; ln \left(1 + \frac{I_L \cdot R_L}{|V_{OUT(CL)}|}\right)$$

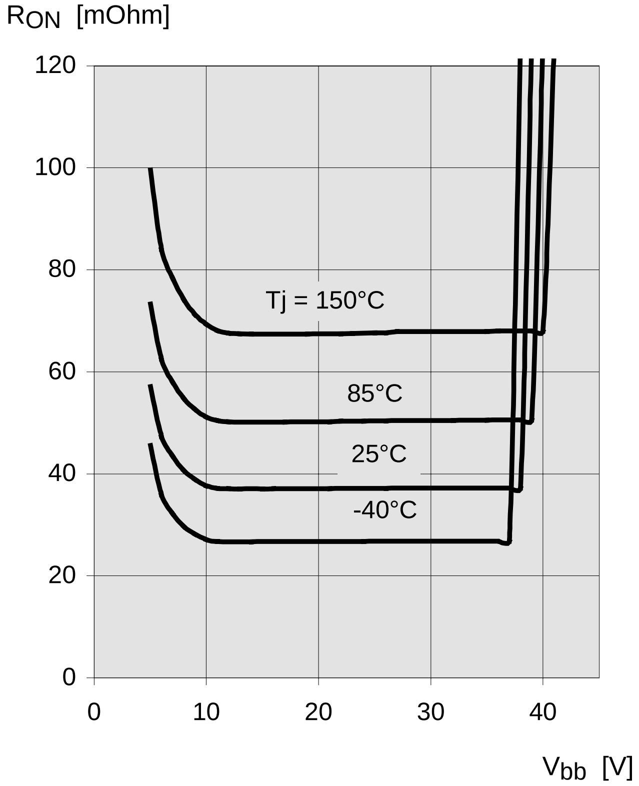
Maximum allowable load inductance for a single switch off (one channel)[5)]

$L = f(I_L)$; $T_{j,start} = 150°C$, $V_{bb} = 12\,V$, $R_L = 0\,\Omega$



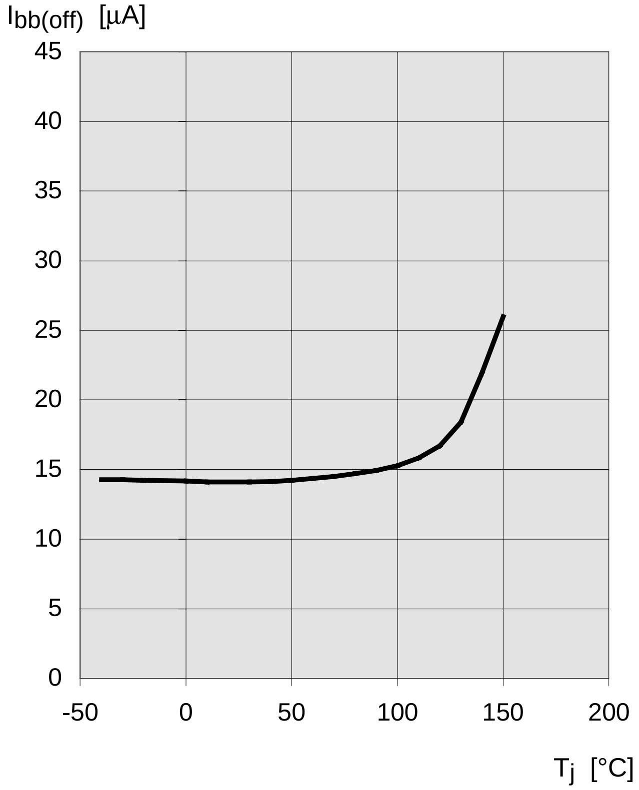
Typ. on-state resistance

$R_{ON} = f(V_{bb}, T_j)$; I_L = 2 A, IN = high



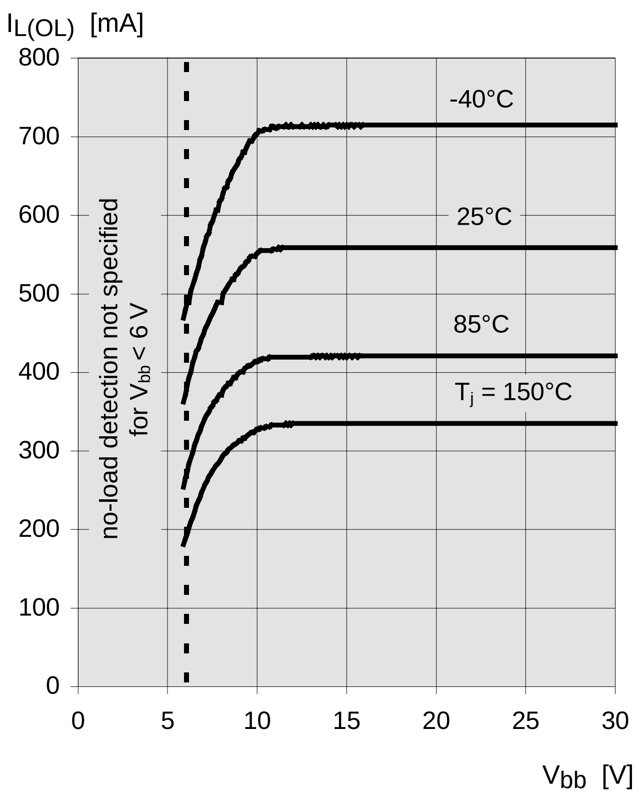
Typ. standby current

$I_{bb(off)} = f(T_j)$; V_{bb} = 9...34 V, IN1,2 = low



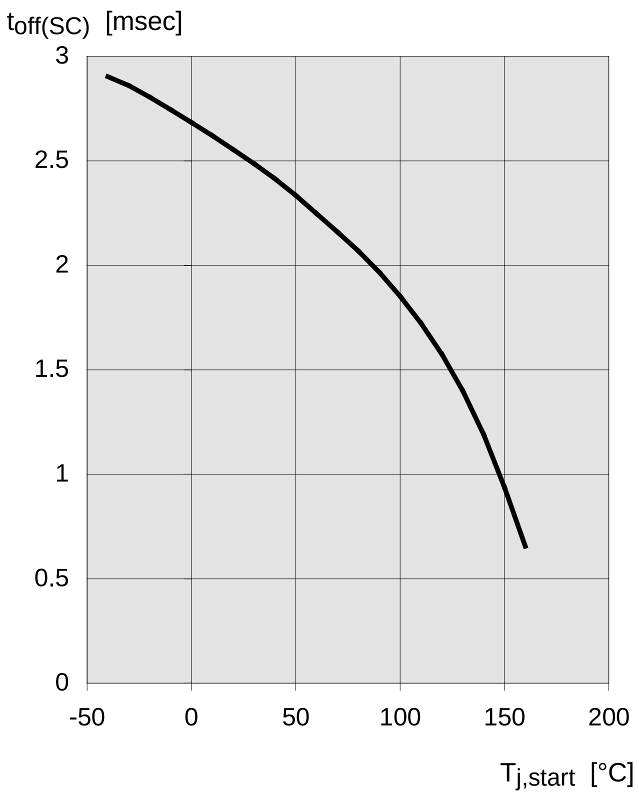
Typ. open load detection current

$I_{L(OL)} = f(V_{bb}, T_j)$; IN = high



Typ. initial short circuit shutdown time

$t_{off(SC)} = f(T_{j,start})$; V_{bb} =12 V



Timing diagrams

Both channels are symmetric and consequently the diagrams are valid for channel 1 and channel 2

Figure 1a: V_{bb} turn on:

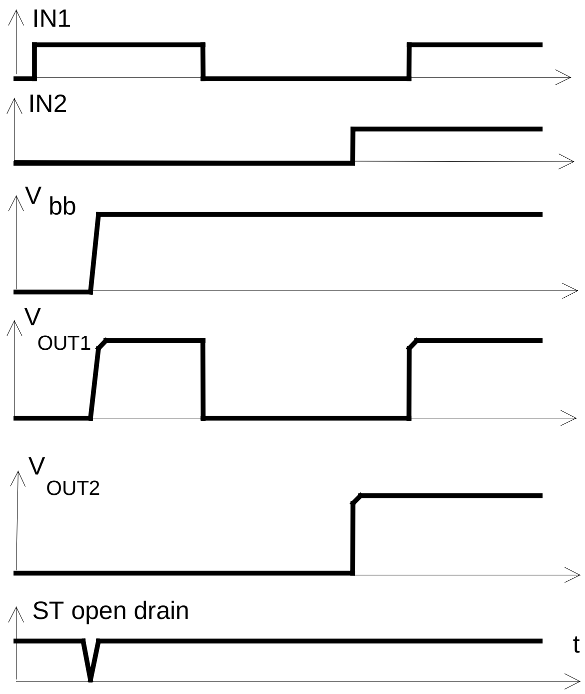


Figure 2a: Switching a resistive load, turn-on/off time and slew rate definition:

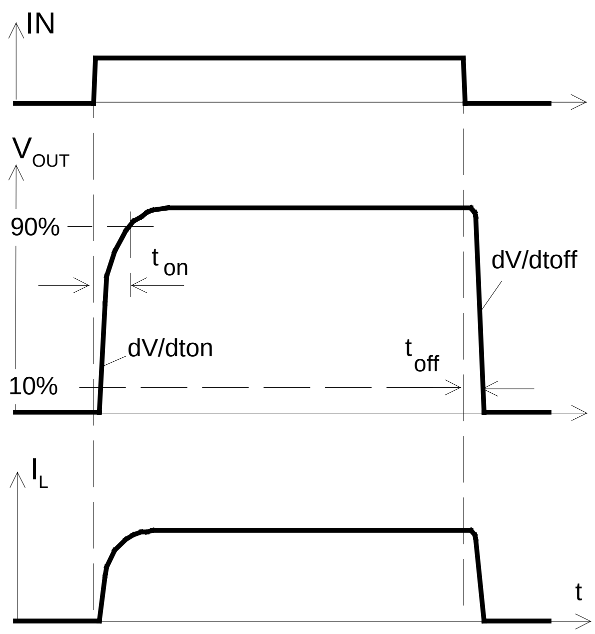
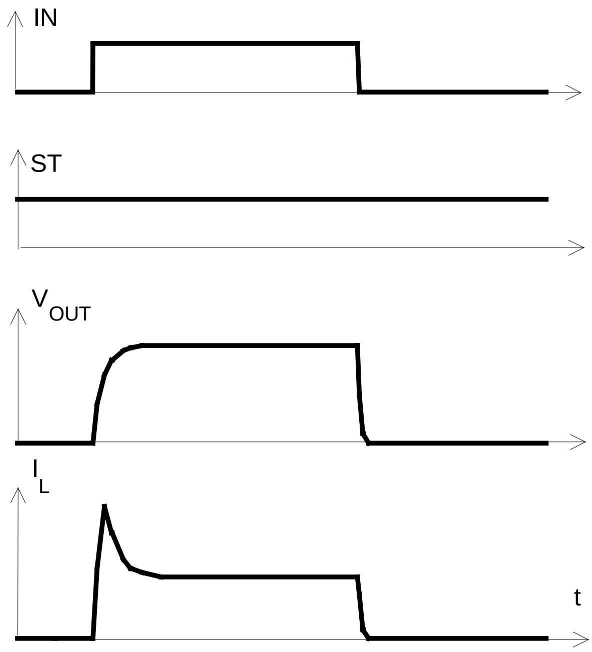
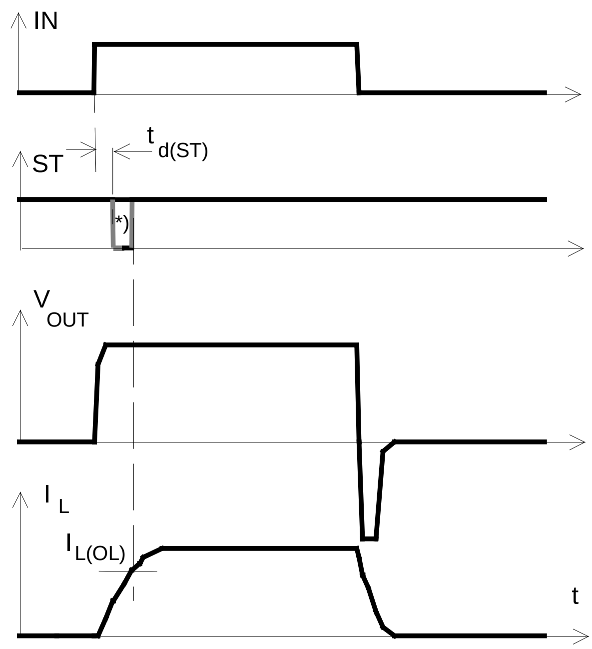


Figure 2b: Switching a lamp:



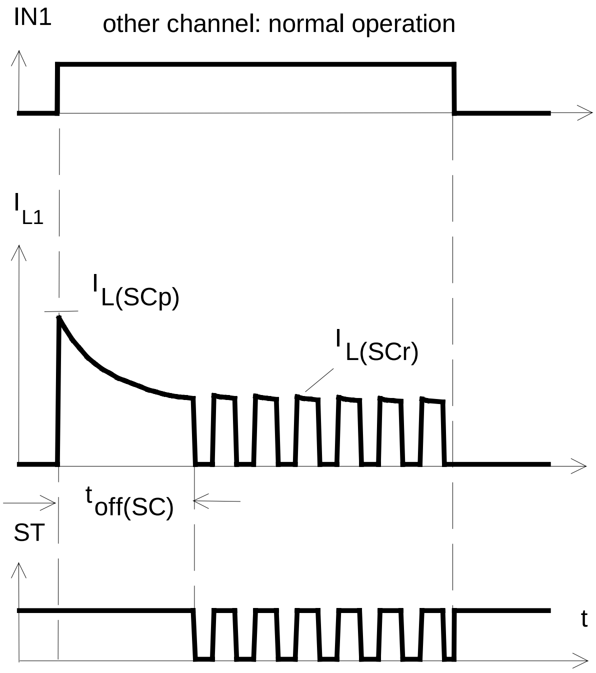
The initial peak current should be limited by the lamp and not by the initial short circuit current $I_{L(SCp)}$ = 44 A typ. of the device.

Figure 2c: Switching an inductive load



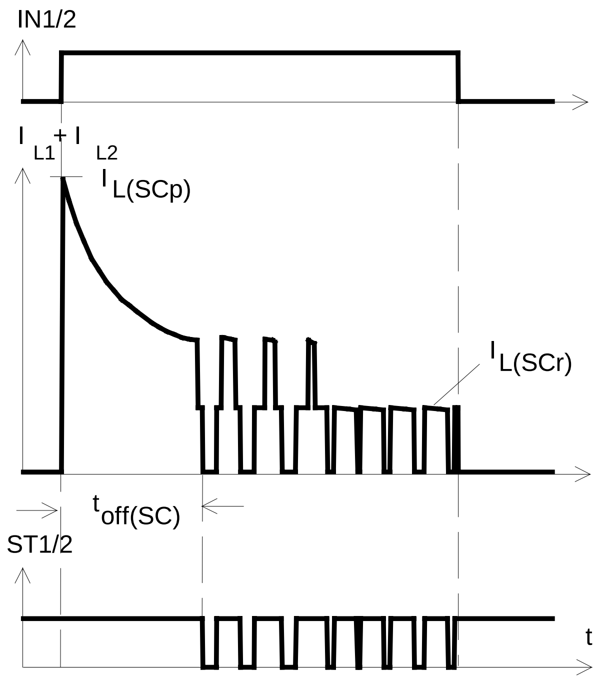
*) if the time constant of load is too large, open-load-status may occur

Figure 3a: Turn on into short circuit:
shut down by overtemperature, restart by cooling



Heating up of the chip may require several milliseconds, depending on external conditions ($t_{off(SC)}$ vs. $T_{j,start}$ see page 11)

Figure 3b: Turn on into short circuit:
shut down by overtemperature, restart by cooling
(two parallel switched channels 1 and 2)



ST1 and ST2 have to be configured as a 'Wired OR' function ST1/2 with a single pull-up resistor.

Figure 4a: Overtemperature:
Reset if $T_j < T_{jt}$

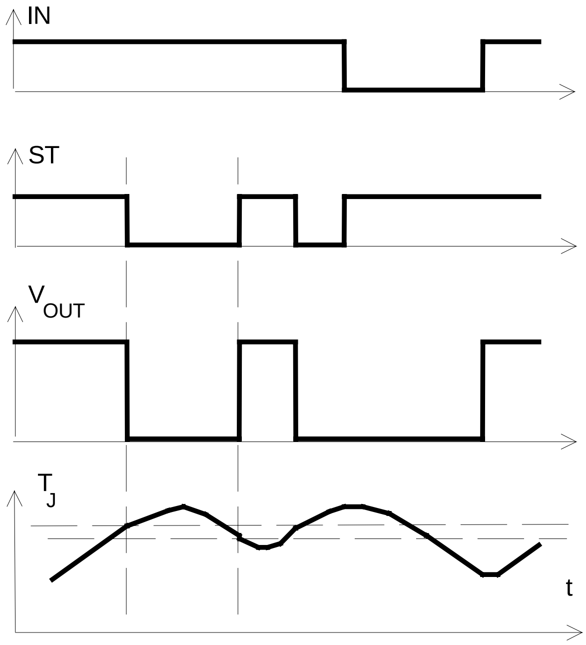
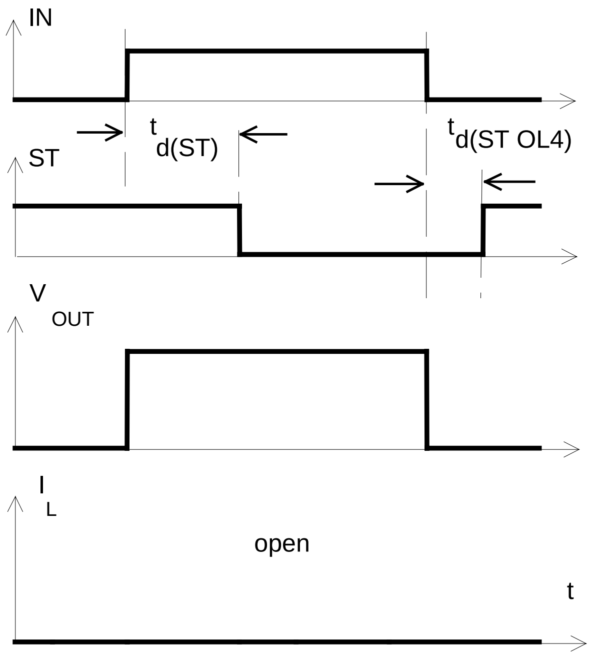
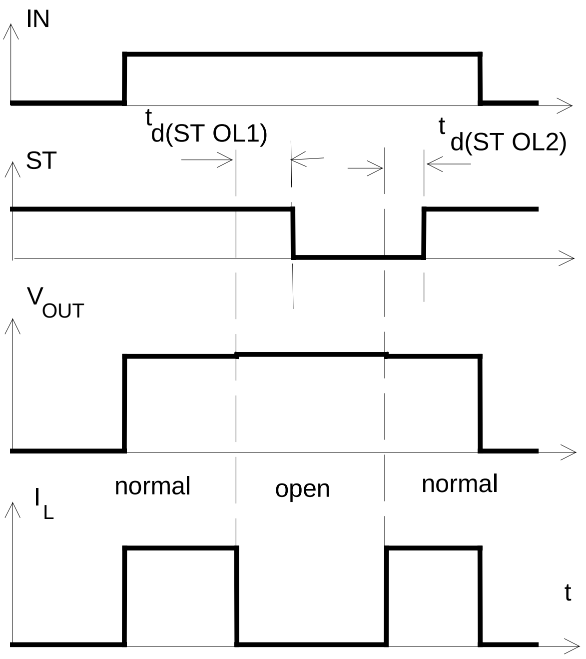


Figure 5a: Open load: detection in ON-state, turn on/off to open load



The status delay $t_{d(ST\ OL4)}$ is for differentiation between the failure modes "open load in ON-state" and "overtemperature"; $t_{d(ST\ OL4)}$ only appears after turn off to open load.

Figure 5b: Open load: detection in ON-state, open load occurs in on-state



$t_{d(ST\ OL1)}$ = 20 µs typ., $t_{d(ST\ OL2)}$ = 10 µs typ

Figure 5c: Open load: detection in ON- and OFF-state (with R_{EXT}), turn on/off to open load

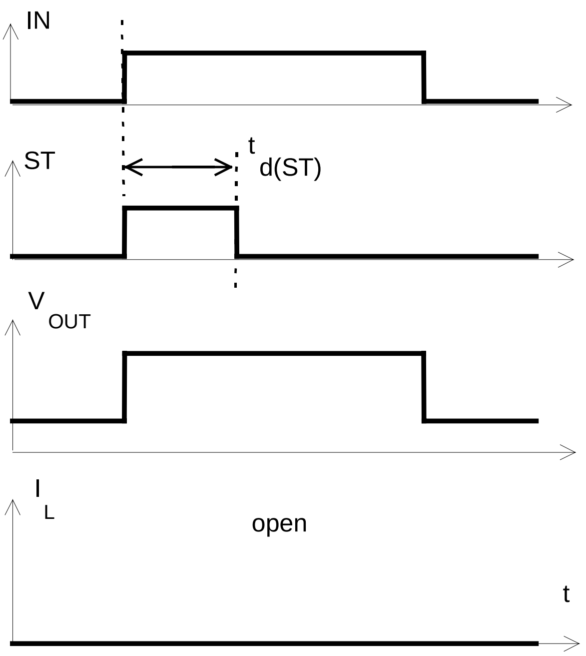


Figure 6a: Undervoltage:

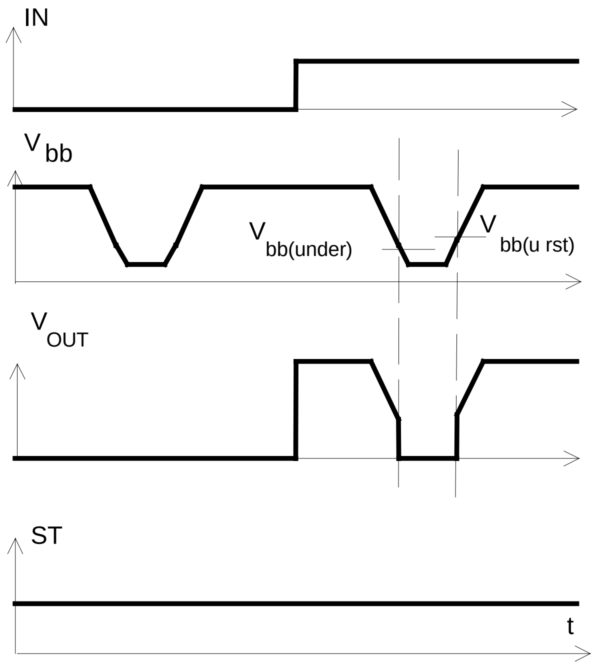
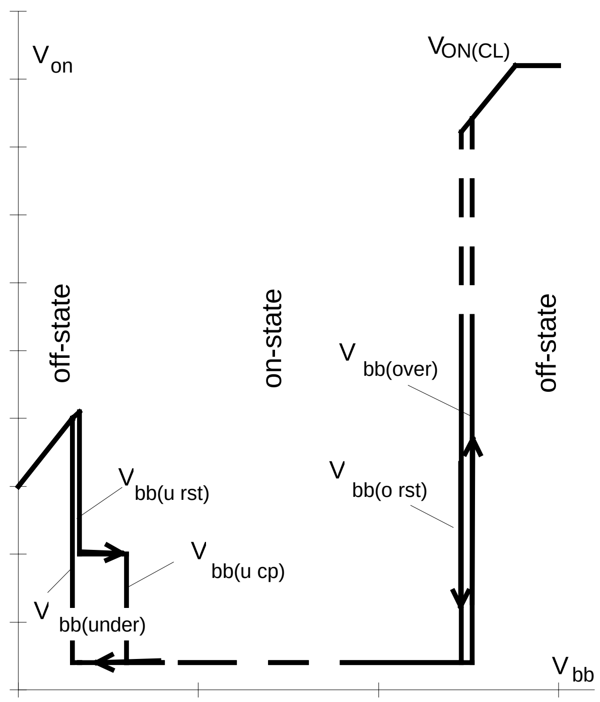
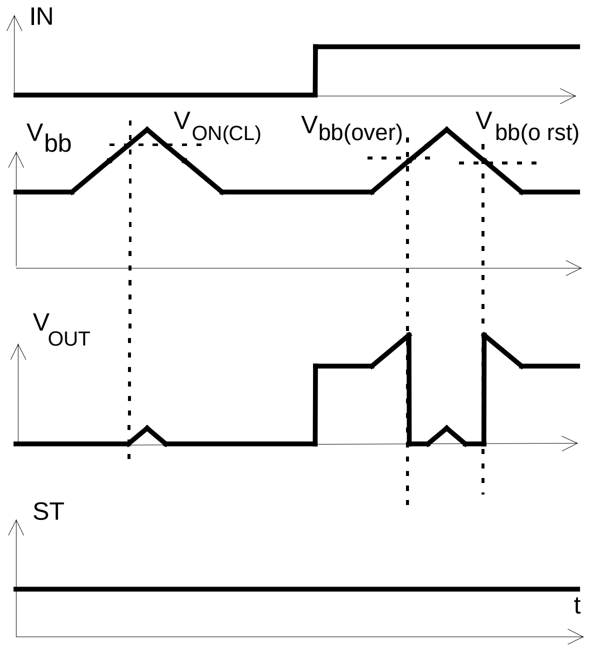


Figure 6b: Undervoltage restart of charge pump



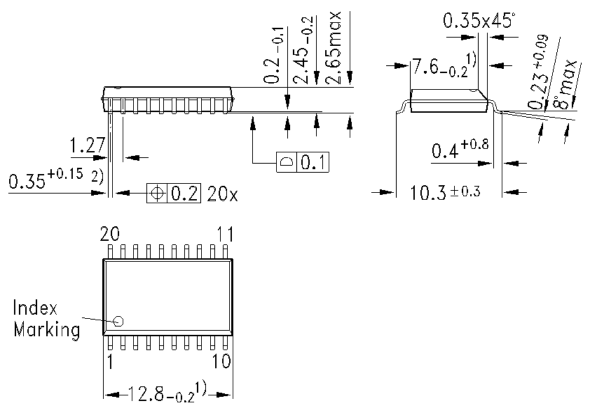
IN = high, normal load conditions.
Charge pump starts at $V_{bb(ucp)}$ = 5.6 V typ.

Figure 7a: Overvoltage:



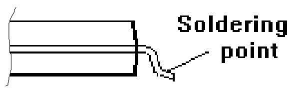
Package and Ordering Code

Standard P-DSO-20-9	Ordering Code
BTS734L1	Q67060-S7009-A2



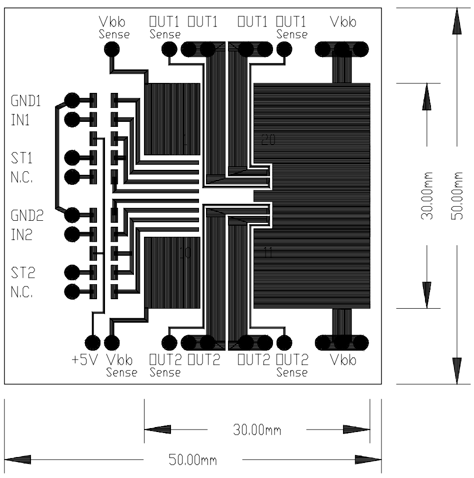
All dimensions in millimetres
1) Does not include plastic or metal protrusions of 0.15 max per side
2) Does not include dambar protrusion of 0.05 max per side

Definition of soldering point with temperature T_S: upper side of solder edge of device pin 15.



Pin 15

Printed circuit board (FR4, 1.5mm thick, one layer 70µm, 6cm^2 active heatsink area) as a reference for max. power dissipation P_{tot}, nominal load current $I_{L(NOM)}$ and thermal resistance R_{thja}



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