

# 256K x 16 (4-MBIT) DYNAMIC RAM WITH EDO PAGE MODE

## FEATURES

- TTL compatible inputs and outputs
- Refresh Interval: 512 cycles/8 ms
- Refresh Mode : RAS-Only, CAS-before-RAS (CBR), and Hidden
- JEDEC standard pinout
- Single power supply  
    5V  $\pm$  10% (IS41C16256A)  
    3.3V  $\pm$  10% (IS41LV16256A)
- Byte Write and Byte Read operation via two CAS
- Lead-free available

## KEY TIMING PARAMETERS

## DESCRIPTION

The *ISSI* IS41C16256A and IS41LV16256A are 262,144 x 16-bit high-performance CMOS Dynamic Random Access Memory. Both products offer accelerated cycle access EDO Page Mode. EDO Page Mode allows 512 random accesses within a single row with access cycle time as short as 10ns per 16-bit word. The Byte Write control, of upper and lower byte, makes the IS41C16256A and IS41LV16256A ideal for use in 16 and 32-bit wide data bus systems.

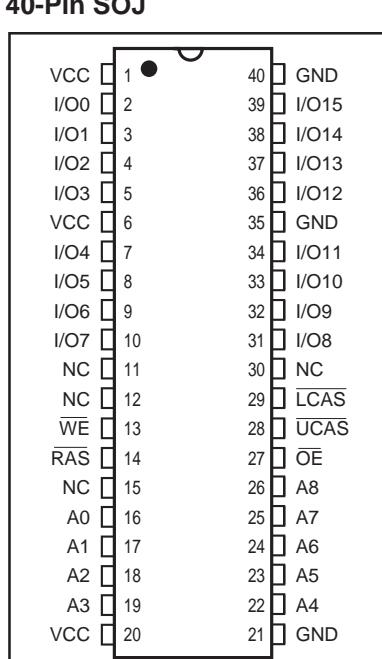
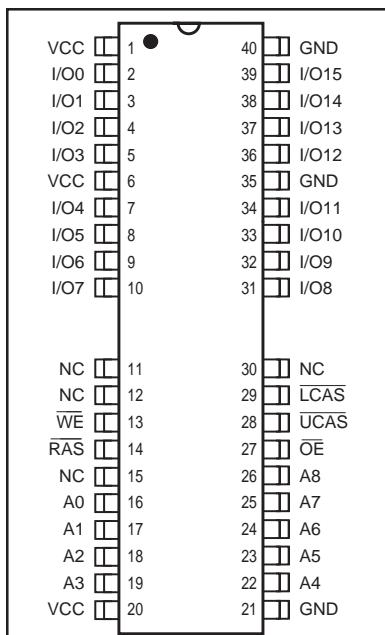
These features make the IS41C16256A and IS41LV1626 ideally suited for high band-width graphics, digital signal processing, high-performance computing systems, and peripheral applications.

The IS41C16256A and IS41LV16256A are packaged in 40-pin 400-mil SOJ and TSOP (Type II).

Parameter	-35	-60	Unit
Max. <u>RAS</u> Access Time (tRAC)	35	60	ns
Max. <u>CAS</u> Access Time (tcAC)	11	15	ns
Max. Column Address Access Time (tAA)	18	30	ns
Min. EDO Page Mode Cycle Time (tpC)	14	25	ns
Min. Read/Write Cycle Time (trC)	60	110	ns

## PIN CONFIGURATIONS

## 40-Pin TSOP (Type II)

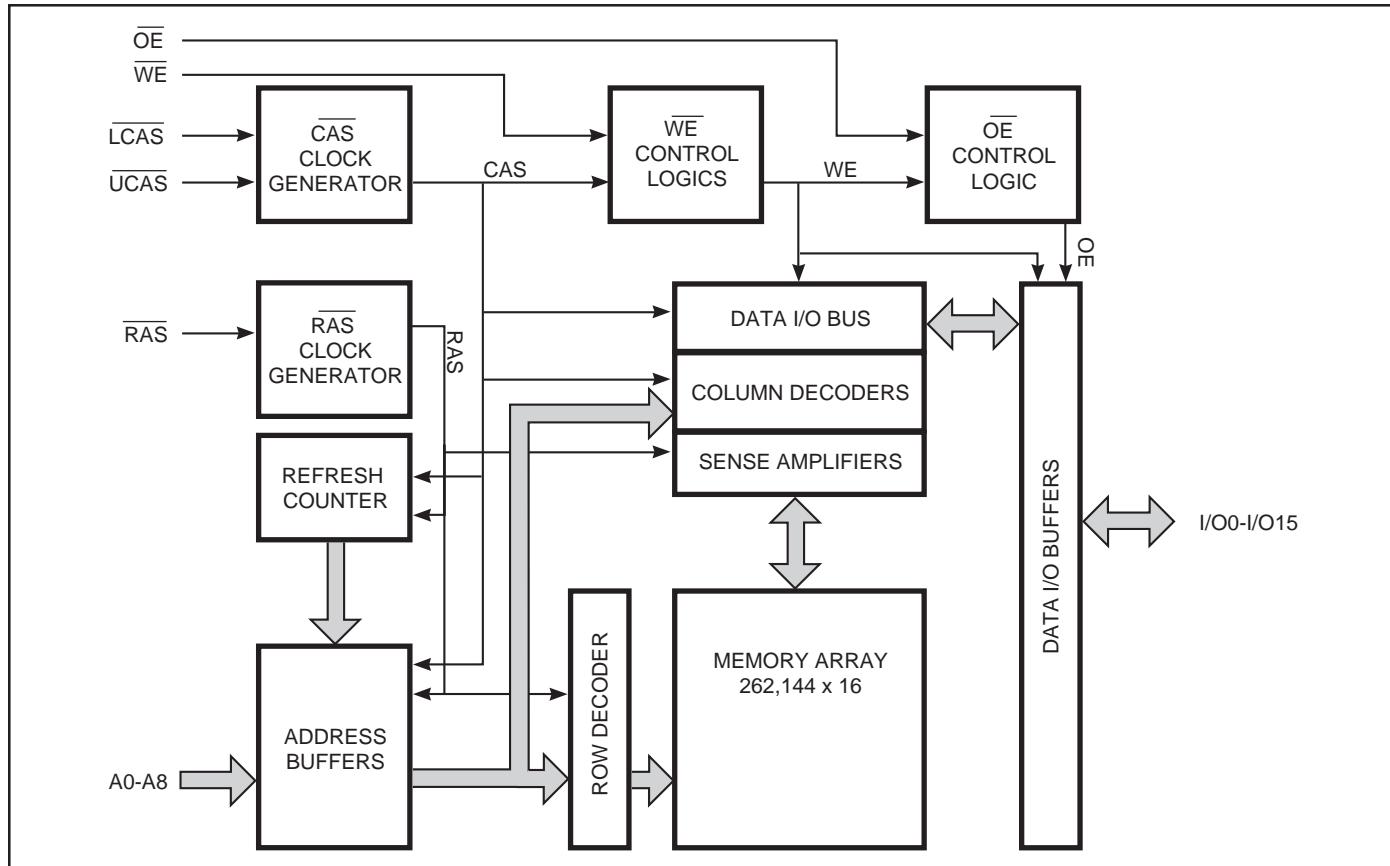


## PIN DESCRIPTIONS

A0-A8	Address Inputs
I/O0-15	Data Inputs/Outputs
<u>WE</u>	Write Enable
<u>OE</u>	Output Enable
<u>RAS</u>	Row Address Strobe
<u>UCAS</u>	Upper Column Address Strobe
<u>LCAS</u>	Lower Column Address Strobe
Vcc	Power
GND	Ground
NC	No Connection

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FUNCTIONAL BLOCK DIAGRAM



## TRUTH TABLE

Function	RAS	LCAS	UCAS	WE	OE	Address	t <sub>R</sub> /t <sub>C</sub>	I/O
Standby	H	H	H	X	X	X		High-Z
Read: Word	L	L	L	H	L	ROW/COL		DOUT
Read: Lower Byte	L	L	H	H	L	ROW/COL		Lower Byte, DOUT Upper Byte, High-Z
Read: Upper Byte	L	H	L	H	L	ROW/COL		Lower Byte, High-Z Upper Byte, DOUT
Write: Word (Early Write)	L	L	L	L	X	ROW/COL		DIN
Write: Lower Byte (Early Write)	L	L	H	L	X	ROW/COL		Lower Byte, DIN Upper Byte, High-Z
Write: Upper Byte (Early Write)	L	H	L	L	X	ROW/COL		Lower Byte, High-Z Upper Byte, DIN
Read-Write <sup>(1,2)</sup>	L	L	L	H→L	L→H	ROW/COL		DOUT, DIN
EDO Page-Mode Read <sup>(2)</sup>	L	H→L	H→L	H	L	ROW/COL		DOUT
1st Cycle:	L	H→L	H→L	H	L	NA/COL		DOUT
2nd Cycle:	L	L→H	L→H	H	L	NA/NA		DOUT
Any Cycle:	L	L→H	L→H	H	L	NA/NA		DOUT
EDO Page-Mode Write <sup>(1)</sup>	L	H→L	H→L	L	X	ROW/COL		DIN
1st Cycle:	L	H→L	H→L	L	X	NA/COL		DIN
2nd Cycle:	L	H→L	H→L	H	L	NA/NA		DOUT
EDO Page-Mode Read-Write <sup>(1,2)</sup>	L	H→L	H→L	H→L	L→H	ROW/COL		DOUT, DIN
1st Cycle:	L	H→L	H→L	H→L	L→H	NA/COL		DOUT, DIN
2nd Cycle:	L	H→L	H→L	H→L	L→H	NA/NA		DOUT, DIN
Hidden Refresh <sup>(2)</sup>	Read L→H→L	L	L	H	L	ROW/COL		DOUT
	Write L→H→L	L	L	L	X	ROW/COL		DOUT
RAS-Only Refresh	L	H	H	X	X	ROW/NA		High-Z
CBR Refresh <sup>(3)</sup>	H→L	L	L	X	X	X		High-Z

## Notes:

1. These WRITE cycles may also be BYTE WRITE cycles (either LCAS or UCAS active).
2. These READ cycles may also be BYTE READ cycles (either LCAS or UCAS active).
3. At least one of the two CAS signals must be active (LCAS or UCAS).

## Functional Description

The IS41C16256A and IS41LV16256A is a CMOS DRAM optimized for high-speed bandwidth, low power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits. These are entered nine bits (A0-A8) at a time. The row address is latched by the Row Address Strobe (**RAS**). The column address is latched by the Column Address Strobe (**CAS**). **RAS** is used to latch the first nine bits and **CAS** is used the latter nine bits.

The IS41C16256A and IS41LV16256A has two **CAS** controls, **LCAS** and **UCAS**. The **LCAS** and **UCAS** inputs internally generates a **CAS** signal functioning in an identical manner to the single **CAS** input on the other 256K x 16 DRAMs. The key difference is that each **CAS** controls its corresponding I/O tristate logic (in conjunction with **OE** and **WE** and **RAS**). **LCAS** controls I/O0 through I/O7 and **UCAS** controls I/O8 through I/O15.

The IS41C16256A and IS41LV16256A **CAS** function is determined by the first **CAS** (**LCAS** or **UCAS**) transitioning LOW and the last transitioning back HIGH. The two **CAS** controls give the IS41C16256A both BYTE READ and BYTE WRITE cycle capabilities.

## Memory Cycle

A memory cycle is initiated by bring **RAS** LOW and it is terminated by returning both **RAS** and **CAS** HIGH. To ensures proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum **trAS** time has expired. A new cycle must not be initiated until the minimum precharge time **trP**, **tCP** has elapsed.

## Read Cycle

A read cycle is initiated by the falling edge of **CAS** or **OE**, whichever occurs last, while holding **WE** HIGH. The column address must be held for a minimum time specified by **tAR**. Data Out becomes valid only when **trAC**, **tAA**, **tcAC** and **toEA** are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

## Write Cycle

A write cycle is initiated by the falling edge of **CAS** and **WE**, whichever occurs last. The input data must be valid at or before the falling edge of **CAS** or **WE**, whichever occurs last.

## Refresh Cycle

To retain data, 512 refresh cycles are required in each 8 ms period. There are two ways to refresh the memory.

1. By clocking each of the 512 row addresses (A0 through A8) with **RAS** at least once every 8 ms. Any read, write, read-modify-write or **RAS**-only cycle refreshes the addressed row.

2. Using a **CAS**-before-**RAS** refresh cycle. **CAS**-before-**RAS** refresh is activated by the falling edge of **RAS**, while holding **CAS** LOW. In **CAS**-before-**RAS** refresh cycle, an internal 9-bit counter provides the row addresses and the external address inputs are ignored.

**CAS**-before-**RAS** is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

## Extended Data Out Page Mode

EDO page mode operation permits all 512 columns within a selected row to be randomly accessed at a high data rate.

In EDO page mode read cycle, the data-out is held to the next **CAS** cycle's falling edge, instead of the rising edge. For this reason, the valid data output time in EDO page mode is extended compared with the fast page mode. In the fast page mode, the valid data output time becomes shorter as the **CAS** cycle time becomes shorter. Therefore, in EDO page mode, the timing margin in read cycle is larger than that of the fast page mode even if the **CAS** cycle time becomes shorter.

In EDO page mode, due to the extended data function, the **CAS** cycle time can be shorter than in the fast page mode if the timing margin is the same.

The EDO page mode allows both read and write operations during one **RAS** cycle, but the performance is equivalent to that of the fast page mode in that case.

## Power-On

After application of the **Vcc** supply, an initial pause of 200  $\mu$ s is required followed by a minimum of eight initialization cycles (any combination of cycles containing a **RAS** signal).

During power-on, it is recommended that **RAS** track with **Vcc** or be held at a valid **VIH** to avoid current surges.

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameters		Rating	Unit
V <sub>T</sub>	Voltage on Any Pin Relative to GND	5V	−1.0 to +7.0	V
		3.3V	−0.5 to 4.6	V
V <sub>CC</sub>	Supply Voltage	5V	−1.0 to +7.0	V
		3.3V	−0.5 to 4.6	V
I <sub>OUT</sub>	Output Current	50	mA	
P <sub>D</sub>	Power Dissipation	1	W	
T <sub>A</sub>	Commercial Operation Temperature	0 to +70	°C	
T <sub>STG</sub>	Storage Temperature	−55 to +125	°C	

**Note:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	5V	4.5	5.0	5.5	V
		3.3V	3.0	3.3	3.6	
V <sub>IH</sub>	Input High Voltage	5V	2.4	—	V <sub>CC</sub> + 1.0	V
		3.3V	2.0	—	V <sub>CC</sub> + 0.3	
V <sub>IL</sub>	Input Low Voltage	5V	−1.0	—	0.8	V
		3.3V	−0.3	—	0.8	
T <sub>A</sub>	Commercial Ambient Temperature	0	—	—	+70	°C

CAPACITANCE<sup>(1,2)</sup>

Symbol	Parameter	Max.	Unit
C <sub>IN1</sub>	Input Capacitance: A0-A8	5	pF
C <sub>IN2</sub>	Input Capacitance: RAS, UCAS, LCAS, WE, OE	7	pF
C <sub>IO</sub>	Data Input/Output Capacitance: I/O0-I/O15	7	pF

**Notes:**

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz,

ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

(Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed	Min.	Max.	Unit
I <sub>IL</sub>	Input Leakage Current	Any input $0V \leq V_{IN} \leq V_{CC}$ Other inputs not under test = 0V		-10	10	µA
I <sub>IO</sub>	Output Leakage Current	Output is disabled (Hi-Z) $0V \leq V_{OUT} \leq V_{CC}$		-10	10	µA
V <sub>OH</sub>	Output High Voltage Level	$I_{OH} = -2\text{ mA}$		2.4	—	V
V <sub>OL</sub>	Output Low Voltage Level	$I_{OL} = +2\text{ mA}$		—	0.4	V
I <sub>CC1</sub>	Stand-by Current: TTL	$\overline{RAS}, \overline{LCAS}, \overline{UCAS} \geq V_{IH}$ Commercial	5V	—	4	mA
I <sub>CC1</sub>	Stand-by Current: TTL	$\overline{RAS}, \overline{LCAS}, \overline{UCAS} \geq V_{IH}$ Commercial	3V	—	4	mA
I <sub>CC2</sub>	Stand-by Current: CMOS	$\overline{RAS}, \overline{LCAS}, \overline{UCAS} \geq V_{CC} - 0.2V$	5V	—	2	mA
			3V	—	1	
I <sub>CC3</sub>	Operating Current: Random Read/Write <sup>(2,3,4)</sup> Average Power Supply Current	$\overline{RAS}, \overline{LCAS}, \overline{UCAS},$ Address Cycling, $t_{RC} = t_{RC}$ (min.)	-35 -60	—	230 170	mA
I <sub>CC4</sub>	Operating Current: EDO Page Mode <sup>(2,3,4)</sup> Average Power Supply Current	$\overline{RAS} = V_{IL}, \overline{LCAS}, \overline{UCAS},$ Cycling $t_{PC} = t_{PC}$ (min.)	-35 -60	—	220 160	mA
I <sub>CC5</sub>	Refresh Current: $\overline{RAS}$ -Only <sup>(2,3)</sup> Average Power Supply Current	$\overline{RAS}$ Cycling, $\overline{LCAS}, \overline{UCAS} \geq V_{IH}$ $t_{RC} = t_{RC}$ (min.)	-35 -60	—	230 170	mA
I <sub>CC6</sub>	Refresh Current: CBR <sup>(2,3,5)</sup> Average Power Supply Current	$\overline{RAS}, \overline{LCAS}, \overline{UCAS}$ Cycling $t_{RC} = t_{RC}$ (min.)	-35 -60	—	230 170	mA

## Notes:

1. An initial pause of 200 µs is required after power-up followed by eight  $\overline{RAS}$  refresh cycles ( $\overline{RAS}$ -Only or CBR) before proper device operation is assured. The eight  $\overline{RAS}$  cycles wake-up should be repeated any time the  $t_{REF}$  refresh requirement is exceeded.
2. Dependent on cycle rates.
3. Specified values are obtained with minimum cycle time and the output open.
4. Column-address is changed once each EDO page cycle.
5. Enables on-chip refresh and address counters.

AC CHARACTERISTICS<sup>(1,2,3,4,5,6)</sup>

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-35		-60		Units
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Random READ or WRITE Cycle Time	70	—	110	—	ns
t <sub>TRAC</sub>	Access Time from $\overline{\text{RAS}}^{(6, 7)}$	35	—	60	—	ns
t <sub>TCAC</sub>	Access Time from $\overline{\text{CAS}}^{(6, 8, 15)}$	—	11	—	15	ns
t <sub>AA</sub>	Access Time from Column-Address <sup>(6)</sup>	—	18	—	30	ns
t <sub>TRAS</sub>	$\overline{\text{RAS}}$ Pulse Width	35	10K	60	10K	ns
t <sub>RP</sub>	$\overline{\text{RAS}}$ Precharge Time	25	—	40	—	ns
t <sub>TCAS</sub>	$\overline{\text{CAS}}$ Pulse Width <sup>(26)</sup>	6	10K	10	10K	ns
t <sub>CP</sub>	$\overline{\text{CAS}}$ Precharge Time <sup>(9, 25)</sup>	6	—	10	—	ns
t <sub>CSH</sub>	$\overline{\text{CAS}}$ Hold Time <sup>(21)</sup>	35	—	60	—	ns
t <sub>TRCD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time <sup>(10, 20)</sup>	13	24	20	45	ns
t <sub>TASR</sub>	Row-Address Setup Time	0	—	0	—	ns
t <sub>TRAH</sub>	Row-Address Hold Time	6	—	10	—	ns
t <sub>TASC</sub>	Column-Address Setup Time <sup>(20)</sup>	0	—	0	—	ns
t <sub>CAH</sub>	Column-Address Hold Time <sup>(20)</sup>	6	—	10	—	ns
t <sub>TAR</sub>	Column-Address Hold Time (referenced to $\overline{\text{RAS}}$ )	30	—	45	—	ns
t <sub>TRAD</sub>	$\overline{\text{RAS}}$ to Column-Address Delay Time <sup>(11)</sup>	10	20	15	30	ns
t <sub>TRAL</sub>	Column-Address to $\overline{\text{RAS}}$ Lead Time	18	—	30	—	ns
t <sub>TRPC</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	0	—	0	—	ns
t <sub>TRSH</sub>	$\overline{\text{RAS}}$ Hold Time <sup>(27)</sup>	10	—	15	—	ns
t <sub>TCLZ</sub>	$\overline{\text{CAS}}$ to Output in Low-Z <sup>(15, 29)</sup>	3	—	3	—	ns
t <sub>TCRP</sub>	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time <sup>(21)</sup>	5	—	5	—	ns
t <sub>TOD</sub>	Output Disable Time <sup>(19, 28, 29)</sup>	3	15	3	15	ns
t <sub>TOE / TOEA</sub>	Output Enable Time <sup>(15, 16)</sup>	0	11	—	15	ns
t <sub>TOEHC</sub>	$\overline{\text{OE}}$ HIGH Hold Time from $\overline{\text{CAS}}$ HIGH	8	—	8	—	ns
t <sub>TOEP</sub>	$\overline{\text{OE}}$ HIGH Pulse Width	8	—	8	—	ns
t <sub>TOES</sub>	$\overline{\text{OE}}$ LOW to $\overline{\text{CAS}}$ HIGH Setup Time	5	—	7	—	ns
t <sub>TRCS</sub>	Read Command Setup Time <sup>(17, 20)</sup>	0	—	0	—	ns
t <sub>TRRH</sub>	Read Command Hold Time (referenced to $\overline{\text{RAS}}$ ) <sup>(12)</sup>	0	—	0	—	ns
t <sub>TRCH</sub>	Read Command Hold Time (referenced to $\overline{\text{CAS}}$ ) <sup>(12, 17, 21)</sup>	0	—	0	—	ns
t <sub>WCH</sub>	Write Command Hold Time <sup>(17, 27)</sup>	5	—	10	—	ns
t <sub>WCR</sub>	Write Command Hold Time (referenced to $\overline{\text{RAS}}$ ) <sup>(17)</sup>	30	—	50	—	ns

AC CHARACTERISTICS (Continued)<sup>(1,2,3,4,5,6)</sup>

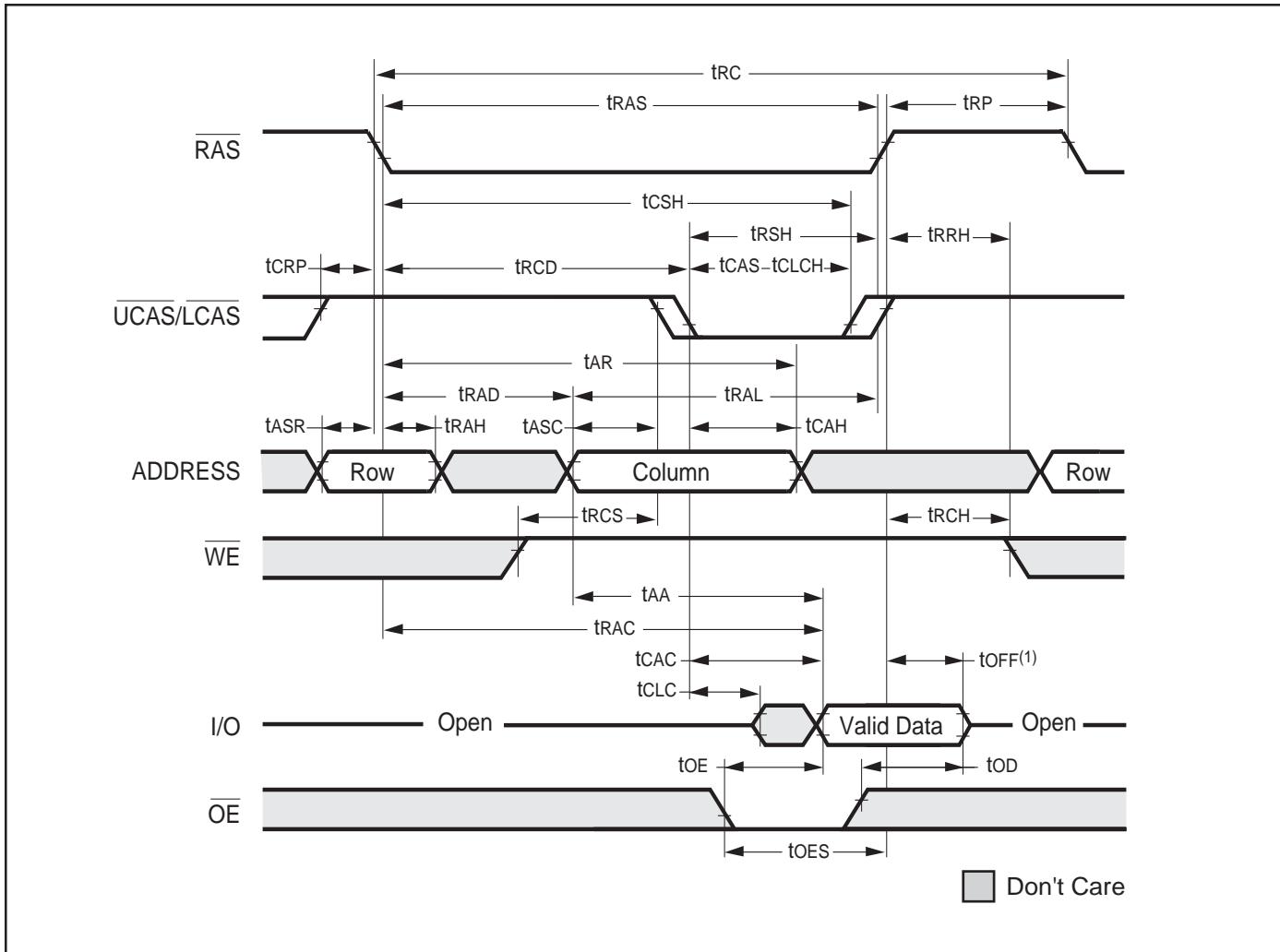
(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-35		-60		Units
		Min.	Max.	Min.	Max.	
tWP	Write Command Pulse Width <sup>(17)</sup>	5	—	10	—	ns
tWPZ	<u>WE</u> Pulse Widths to Disable Outputs	10	—	10	—	ns
trWL	Write Command to <u>RAS</u> Lead Time <sup>(17)</sup>	10	—	15	—	ns
tcWL	Write Command to <u>CAS</u> Lead Time <sup>(17, 21)</sup>	8	—	15	—	ns
twCS	Write Command Setup Time <sup>(14, 17, 20)</sup>	0	—	0	—	ns
tdHR	Data-in Hold Time (referenced to <u>RAS</u> )	30	—	46	—	ns
tACH	Column-Address Setup Time to <u>CAS</u> Precharge during WRITE Cycle	15	—	15	—	ns
toEH	<u>OE</u> Hold Time from <u>WE</u> during READ-MODIFY-WRITE cycle <sup>(18)</sup>	8	—	15	—	ns
tdS	Data-In Setup Time <sup>(15, 22)</sup>	0	—	0	—	ns
tdH	Data-In Hold Time <sup>(15, 22)</sup>	6	—	10	—	ns
trWC	READ-MODIFY-WRITE Cycle Time	80	—	140	—	ns
trWD	<u>RAS</u> to <u>WE</u> Delay Time during READ-MODIFY-WRITE Cycle <sup>(14)</sup>	46	—	80	—	ns
tcWD	<u>CAS</u> to <u>WE</u> Delay Time <sup>(14, 20)</sup>	25	—	36	—	ns
tAWD	Column-Address to <u>WE</u> Delay Time <sup>(14)</sup>	30	—	49	—	ns
tPC	EDO Page Mode READ or WRITE Cycle Time <sup>(24)</sup>	14	—	25	—	ns
trASP	<u>RAS</u> Pulse Width in EDO Page Mode	35	100K	60	100K	ns
tCPA	Access Time from <u>CAS</u> Precharge <sup>(15)</sup>	—	20	—	35	ns
tPRWC	EDO Page Mode READ-WRITE Cycle Time <sup>(24)</sup>	45	—	60	—	ns
tCOH / tDOH	Data Output Hold after <u>CAS</u> LOW	5	—	5	—	ns
tOFF	Output Buffer Turn-Off Delay from <u>CAS</u> or <u>RAS</u> <sup>(13, 15, 19, 29)</sup>	3	10	3	15	ns
tWHZ	Output Disable Delay from <u>WE</u>	3	10	3	15	ns
tCLCH	Last <u>CAS</u> going LOW to First <u>CAS</u> returning HIGH <sup>(23)</sup>	10	—	10	—	ns
tCSR	<u>CAS</u> Setup Time (CBR REFRESH) <sup>(30, 20)</sup>	8	—	10	—	ns
tCHR	<u>CAS</u> Hold Time (CBR REFRESH) <sup>(30, 21)</sup>	8	—	10	—	ns
tORD	<u>OE</u> Setup Time prior to <u>RAS</u> during HIDDEN REFRESH Cycle	0	—	0	—	ns
tREF	Refresh Period (512 Cycles)	—	8	—	8	ms
tr	Transition Time (Rise or Fall) <sup>(2, 3)</sup>	2	50	2	50	ns

**Notes:**

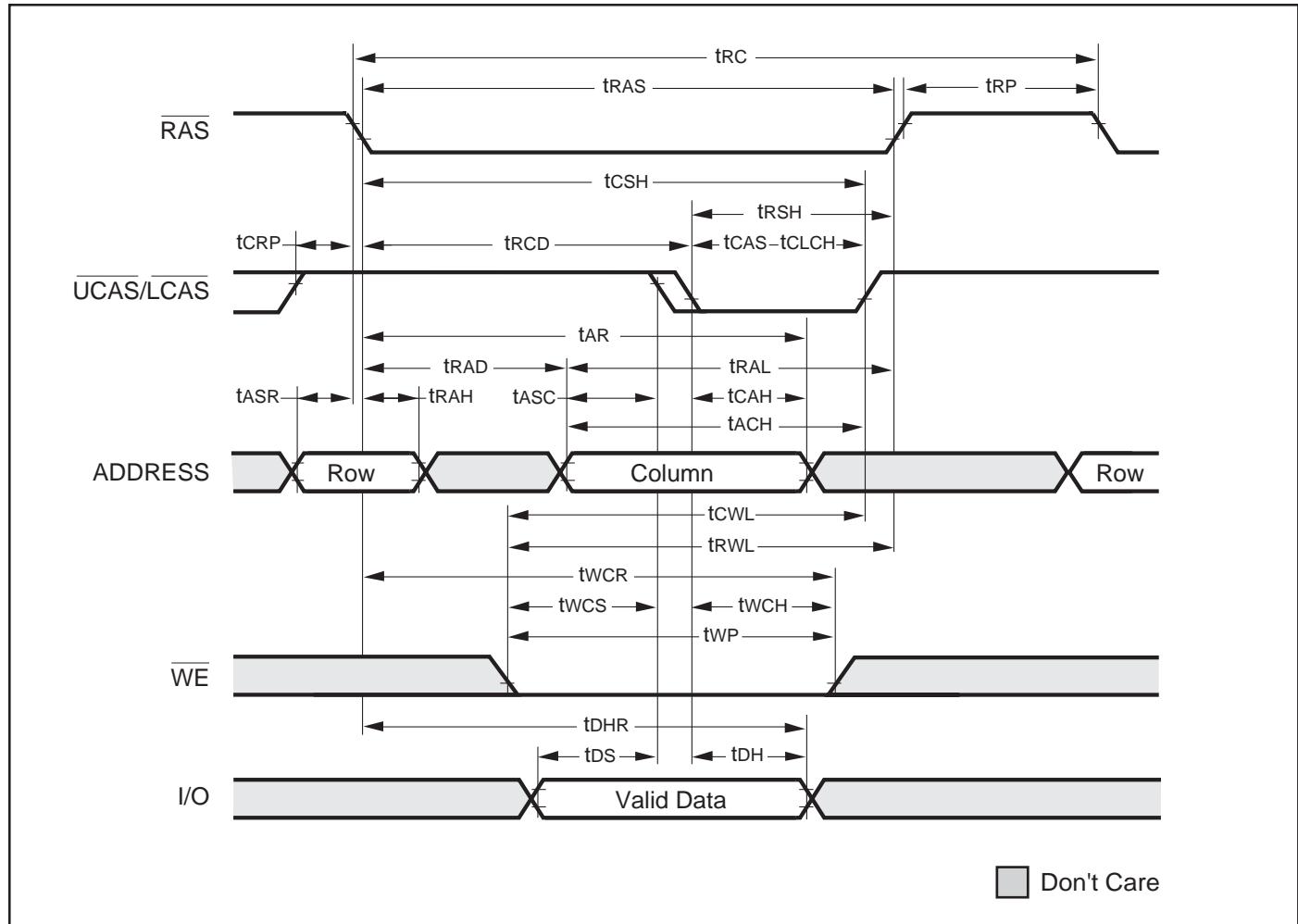
1. An initial pause of 200  $\mu$ s is required after power-up followed by eight RAS refresh cycle (RAS-Only or CBR) before proper device operation is assured. The eight RAS cycles wake-up should be repeated any time the tREF refresh requirement is exceeded.
2.  $V_{IH}$  (MIN) and  $V_{IL}$  (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) and assume to be 1 ns for all inputs.
3. In addition to meeting the transition rate specification, all input signals must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
4. If CAS and RAS =  $V_{IH}$ , data output is High-Z.
5. If CAS =  $V_{IL}$ , data output may contain data from the last valid READ cycle.
6. Measured with a load equivalent to one TTL gate and 50 pF.
7. Assumes that  $trCD \leq trCD$  (MAX). If  $trCD$  is greater than the maximum recommended value shown in this table,  $trAC$  will increase by the amount that  $trCD$  exceeds the value shown.
8. Assumes that  $trCD \geq trCD$  (MAX).
9. If CAS is LOW at the falling edge of RAS, data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer, CAS and RAS must be pulsed for  $t_{CP}$ .
10. Operation with the  $trCD$  (MAX) limit ensures that  $trAC$  (MAX) can be met.  $trCD$  (MAX) is specified as a reference point only; if  $trCD$  is greater than the specified  $trCD$  (MAX) limit, access time is controlled exclusively by  $t_{CAC}$ .
11. Operation within the  $trAD$  (MAX) limit ensures that  $trCD$  (MAX) can be met.  $trAD$  (MAX) is specified as a reference point only; if  $trAD$  is greater than the specified  $trAD$  (MAX) limit, access time is controlled exclusively by  $t_{AA}$ .
12. Either  $trCH$  or  $trRH$  must be satisfied for a READ cycle.
13.  $t_{OFF}$  (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to  $V_{OH}$  or  $V_{OL}$ .
14.  $twCS$ ,  $trWD$ ,  $tAWD$  and  $tcWD$  are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If  $twCS \geq twCS$  (MIN), the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If  $trWD \geq trWD$  (MIN),  $tAWD \geq tAWD$  (MIN) and  $tcWD \geq tcWD$  (MIN), the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until CAS and RAS or OE go back to  $V_{IH}$ ) is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW result in a LATE WRITE (OE-controlled) cycle.
15. Output parameter (I/O) is referenced to corresponding CAS input, I/O0-I/O7 by LCAS and I/O8-I/O15 by UCAS.
16. During a READ cycle, if OE is LOW then taken HIGH before CAS goes HIGH, I/O goes open. If OE is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
17. Write command is defined as WE going low.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both  $t_{OD}$  and  $t_{OEH}$  met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if CAS remains LOW and OE is taken back to LOW after  $t_{OEH}$  is met.
19. The I/Os are in open during READ cycles once  $t_{OD}$  or  $t_{OFF}$  occur.
20. The first  $\chi$ CAS edge to transition LOW.
21. The last  $\chi$ CAS edge to transition HIGH.
22. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. Last falling  $\chi$ CAS edge to first rising  $\chi$ CAS edge.
24. Last rising  $\chi$ CAS edge to next cycle's last rising  $\chi$ CAS edge.
25. Last rising  $\chi$ CAS edge to first falling  $\chi$ CAS edge.
26. Each  $\chi$ CAS must meet minimum pulse width.
27. Last  $\chi$ CAS to go LOW.
28. I/Os controlled, regardless UCAS and LCAS.
29. The 3 ns minimum is a parameter guaranteed by design.
30. Enables on-chip refresh and address counters.

## READ CYCLE

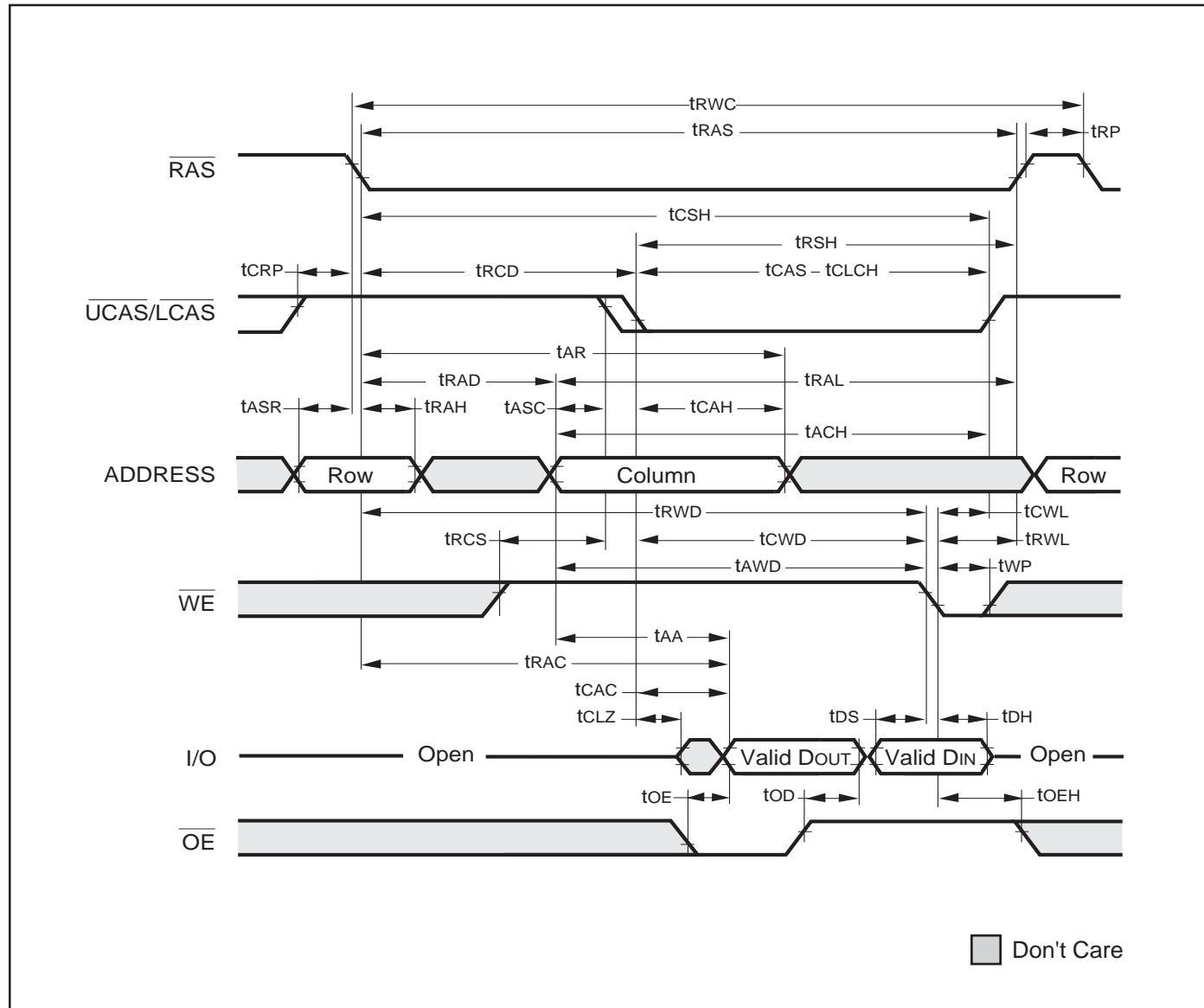
**Note:**

1.  $t_{OFF}$  is referenced from rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.

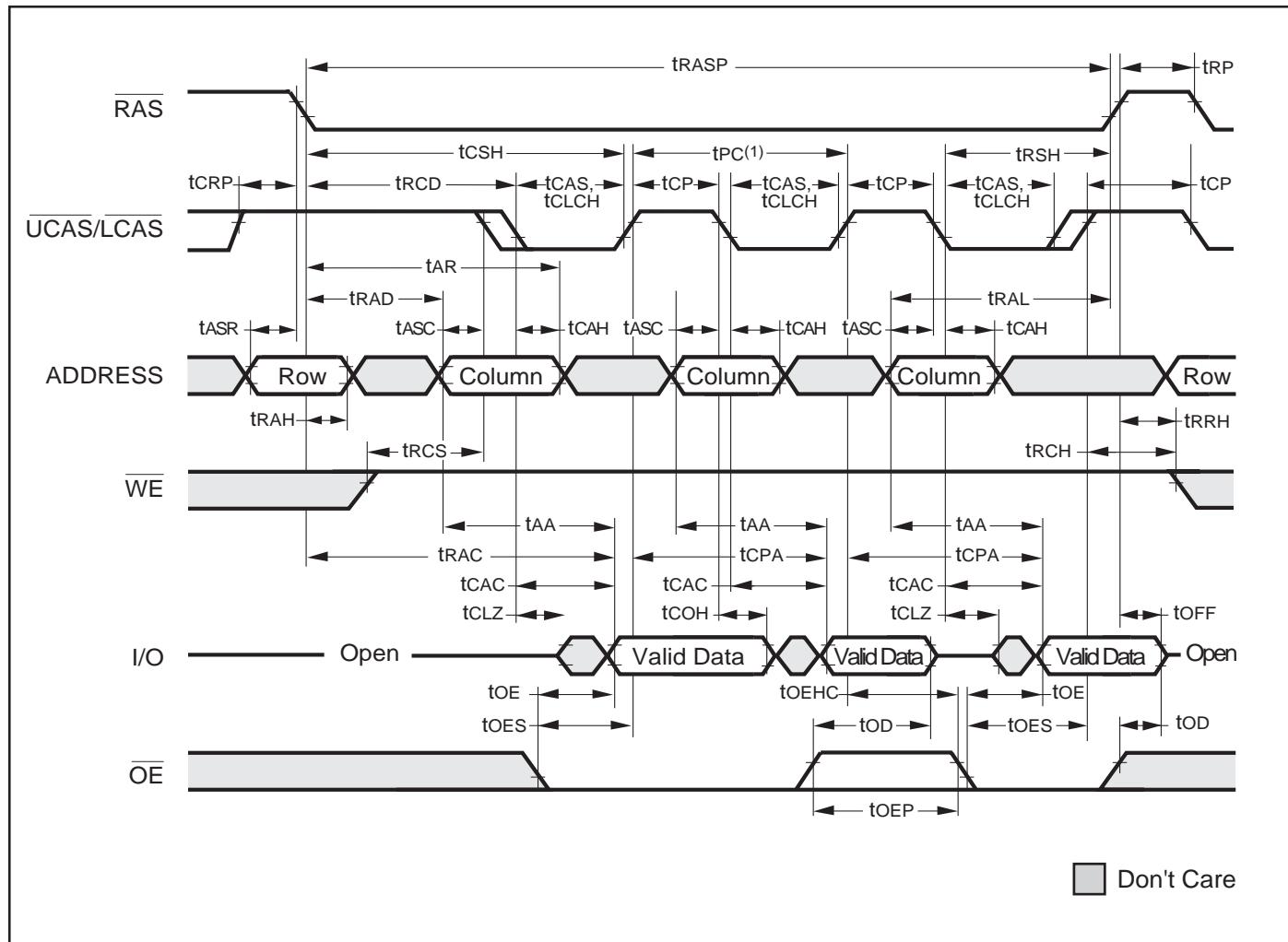
EARLY WRITE CYCLE ( $\overline{OE}$  = DON'T CARE)



READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)



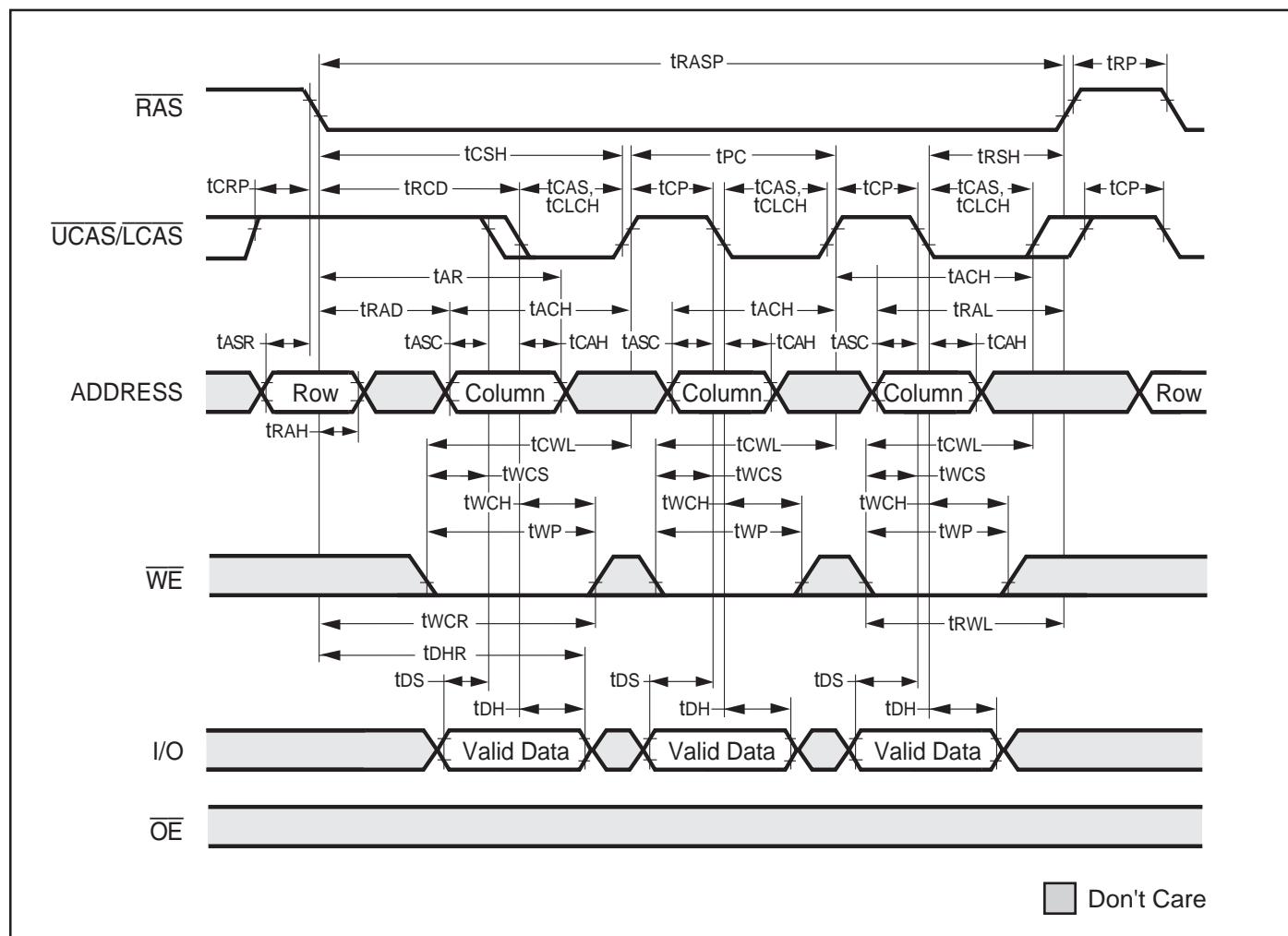
EDO-PAGE-MODE READ CYCLE



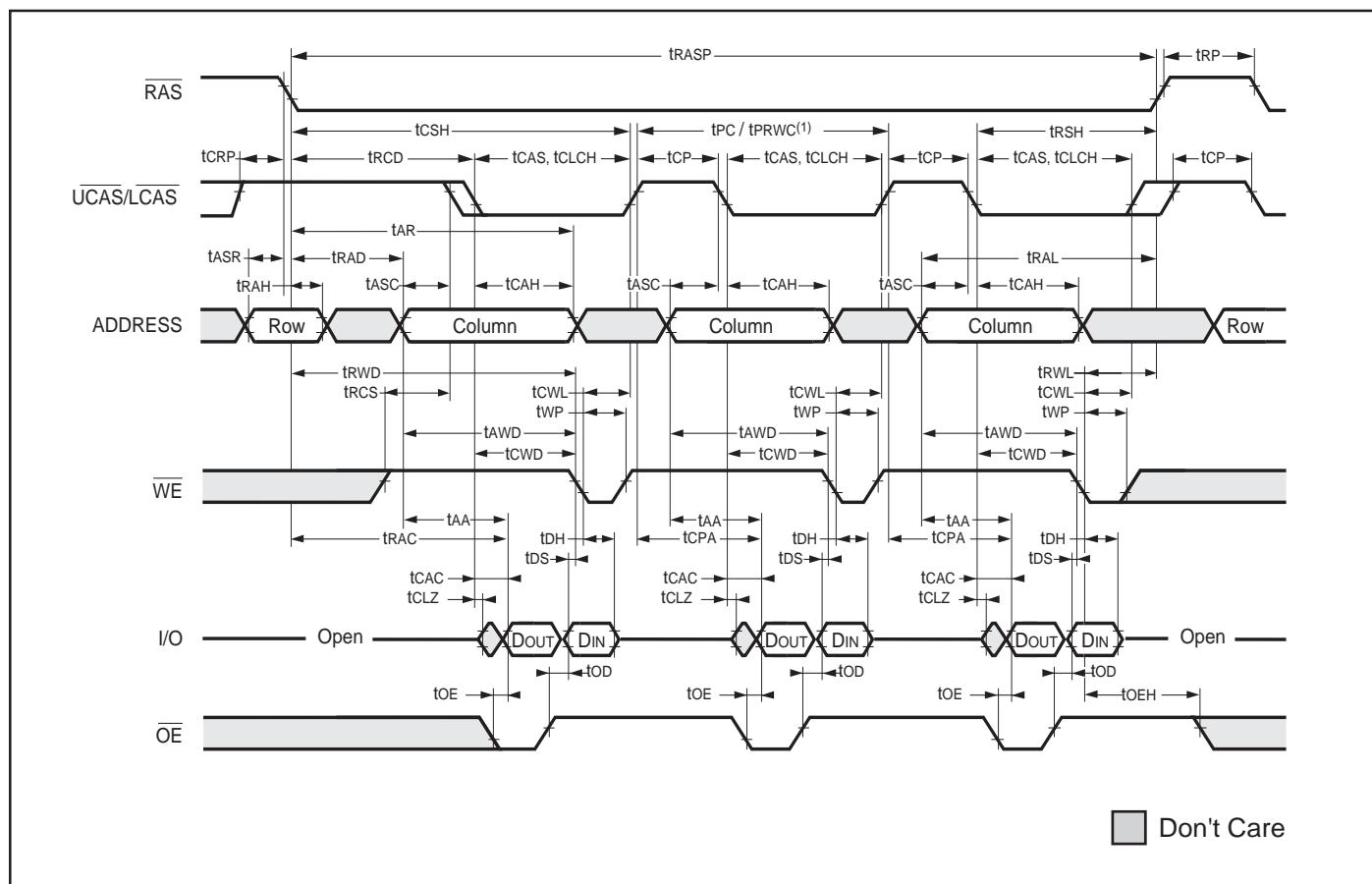
**Note:**

1. tPC can be measured from falling edge of **CAS** to falling edge of **CAS**, or from rising edge of **CAS** to rising edge of **CAS**. Both measurements must meet the tPC specifications.

EDO-PAGE-MODE EARLY-WRITE CYCLE



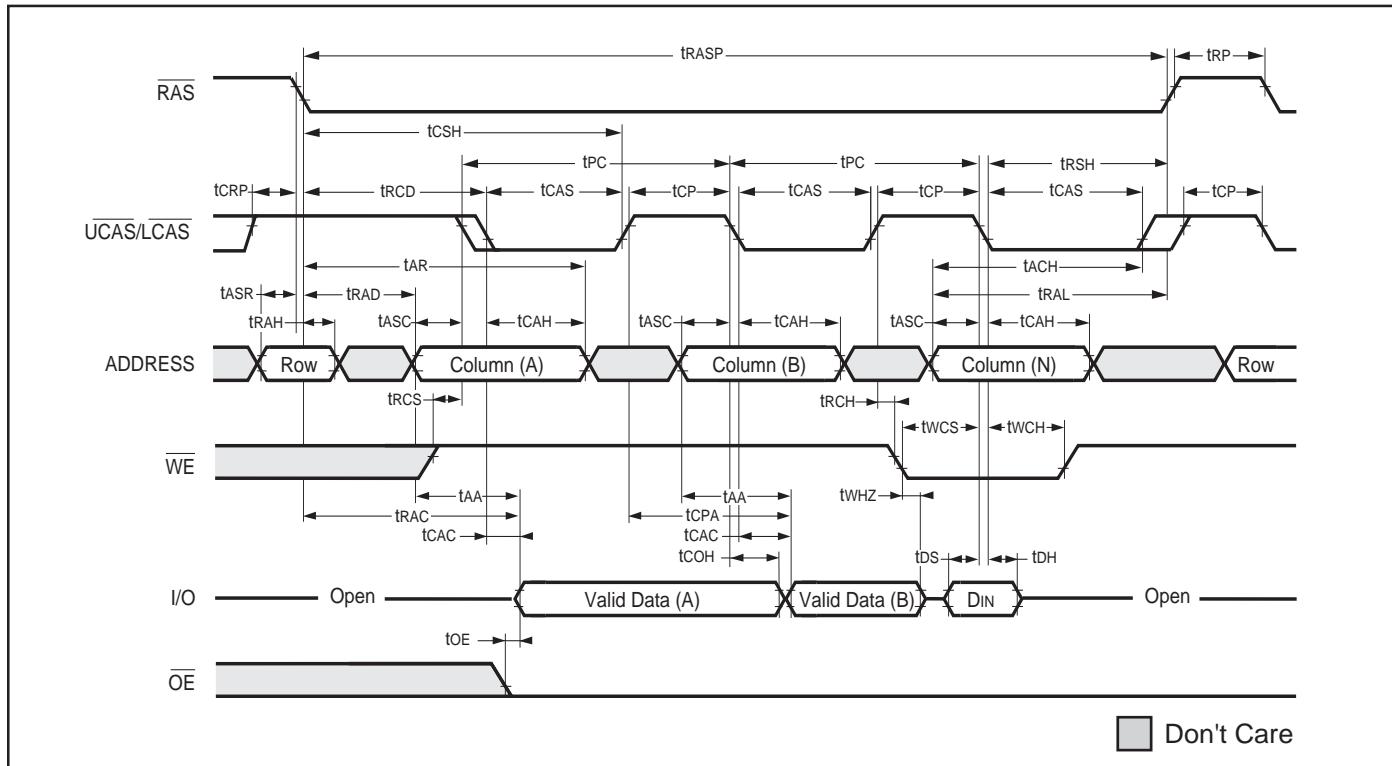
## EDO-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY WRITE Cycles)



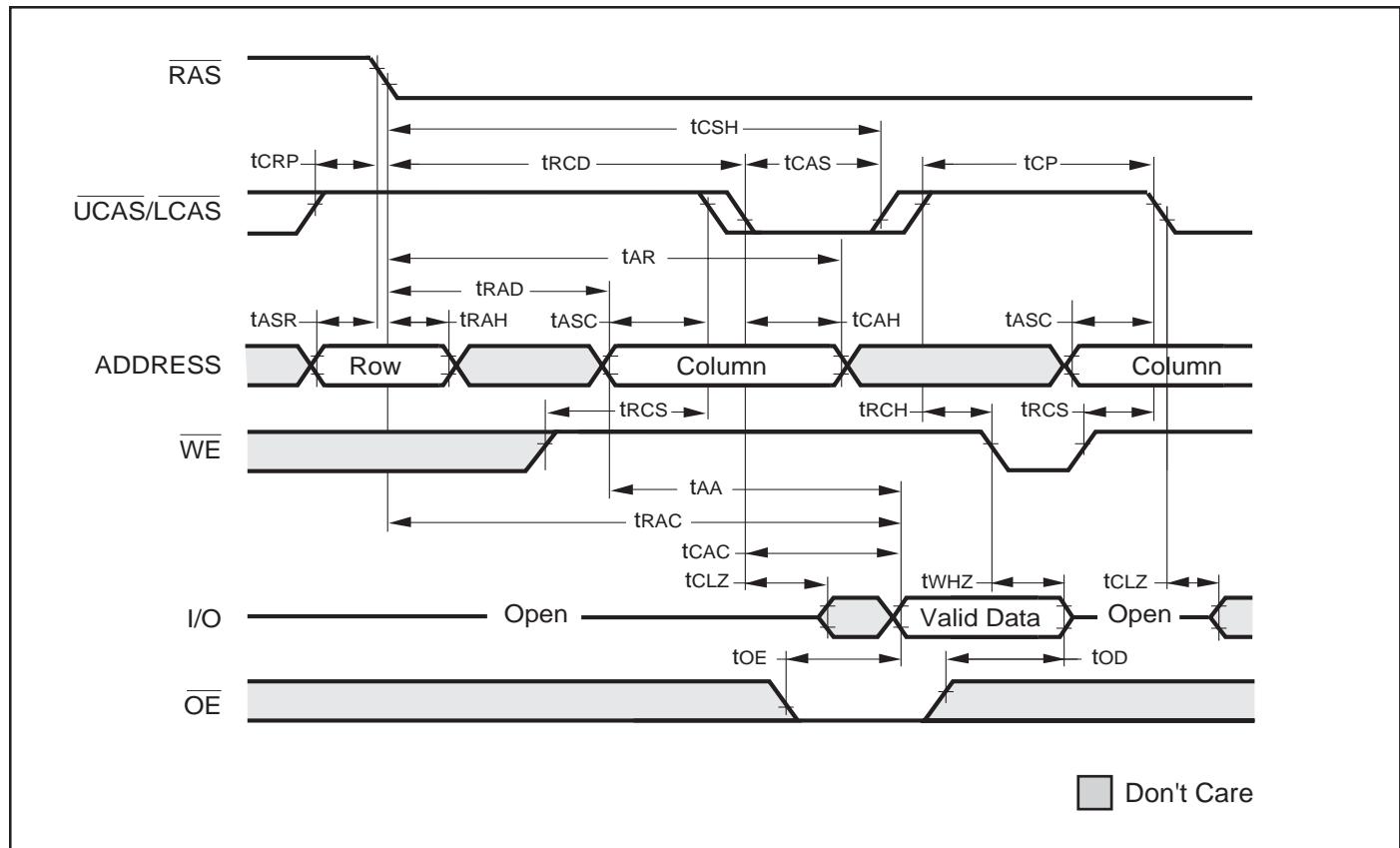
### Note:

1.  $t_{PC}$  can be measured from falling edge of  $\overline{CAS}$  to falling edge of  $\overline{CAS}$ , or from rising edge of  $\overline{CAS}$  to rising edge of  $\overline{CAS}$ . Both measurements must meet the  $t_{PC}$  specifications.

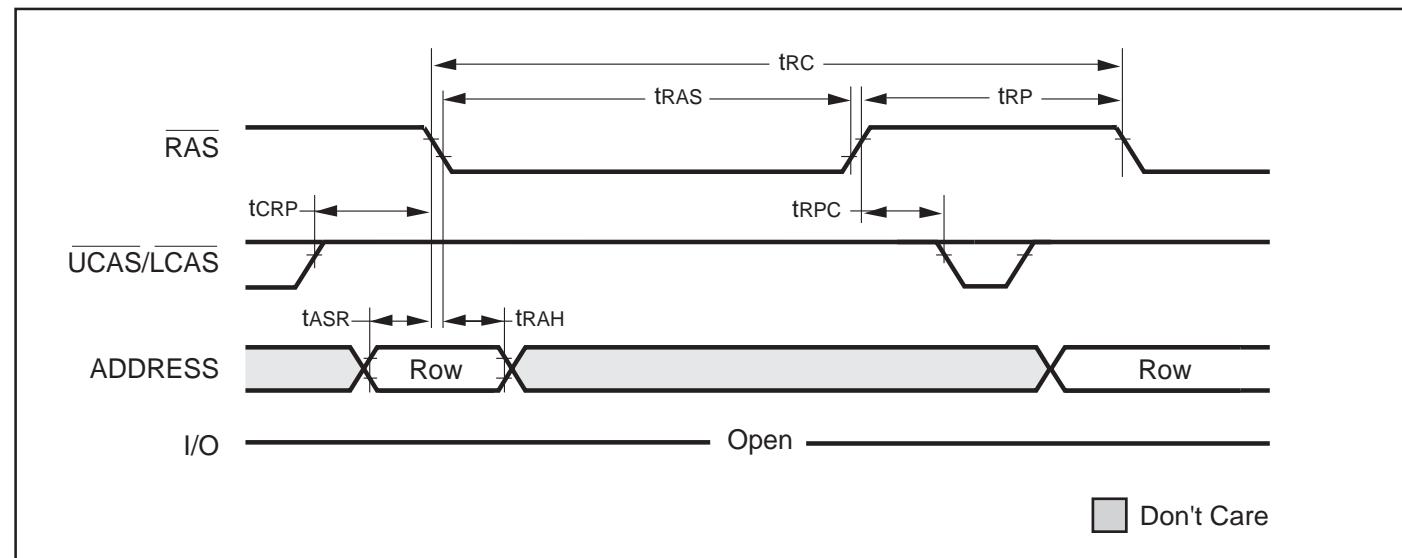
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE (Pseudo READ-MODIFY WRITE)



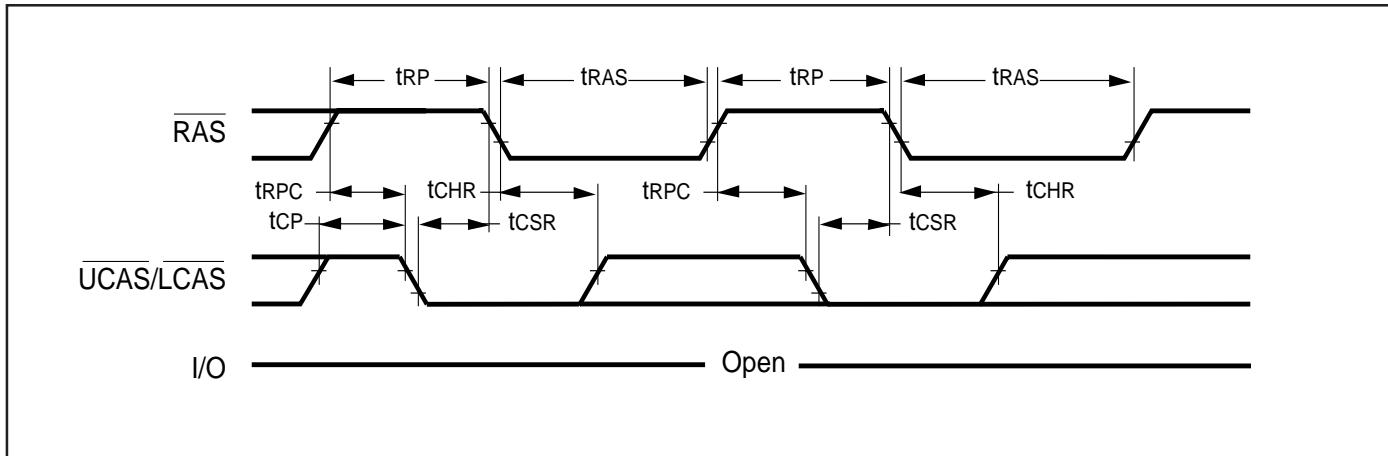
**AC WAVEFORMS**  
**READ CYCLE (With  $\overline{WE}$ -Controlled Disable)**



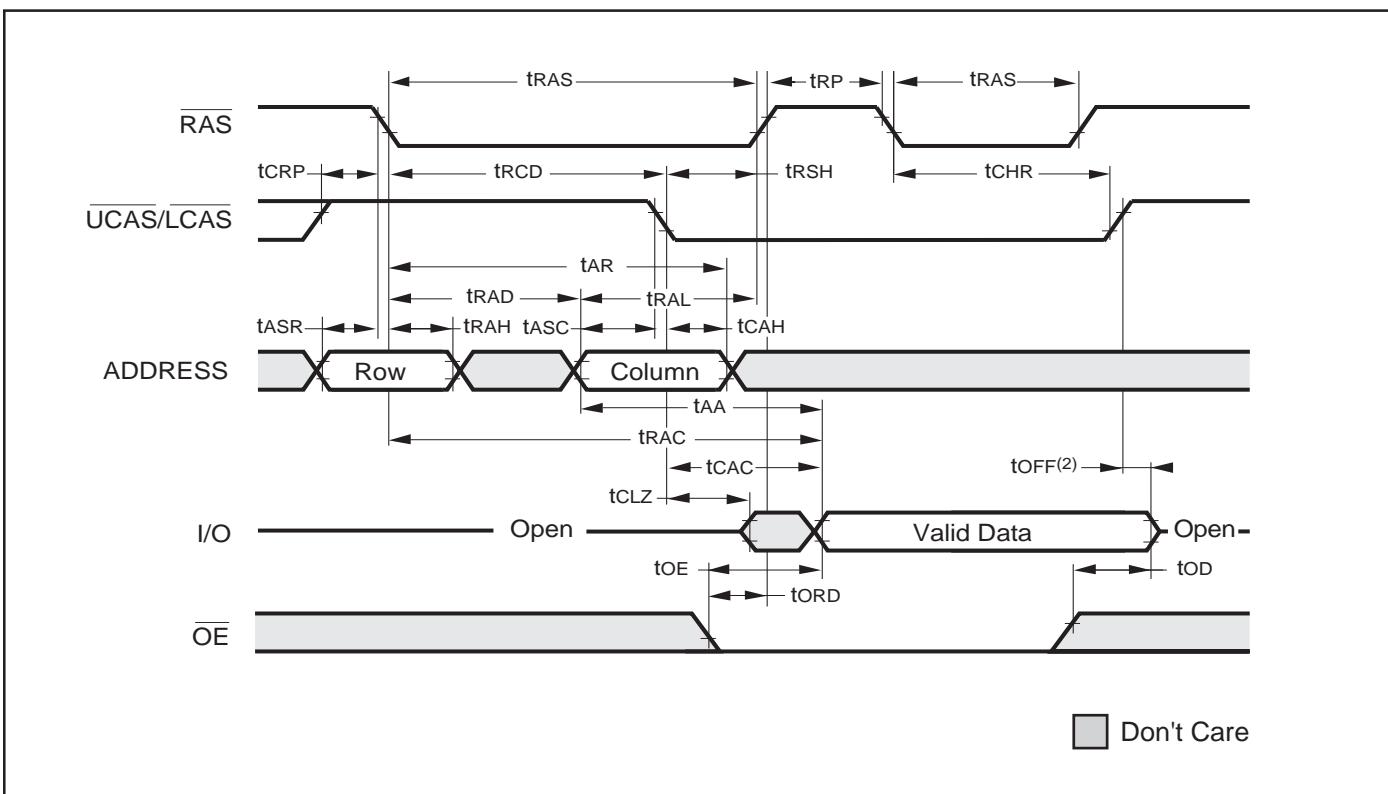
**RAS-ONLY REFRESH CYCLE ( $\overline{OE}$ ,  $\overline{WE}$  = DON'T CARE)**



**CBR REFRESH CYCLE (Addresses;  $\overline{WE}$ ,  $\overline{OE}$  = DON'T CARE)**



**HIDDEN REFRESH CYCLE ( $\overline{WE}$  = HIGH;  $\overline{OE}$  = LOW)<sup>(1)</sup>**



**Notes:**

1. A Hidden Refresh may also be performed after a Write Cycle. In this case,  $\overline{WE}$  = LOW and  $\overline{OE}$  = HIGH.
2. tOFF is referenced from rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.

**ORDERING INFORMATION : 5V**

**Commercial Range: 0°C to +70°C**

<b>Speed(ns)</b>	<b>Order Part No.</b>	<b>Package</b>
35	IS41C16256A-35K	400-mil SOJ
	IS41C16256A-35T	400-mil TSOP (Type II)
60	IS41C16256A-60K	400-mil SOJ
	IS41C16256A-60T	400-mil TSOP (Type II)

**ORDERING INFORMATION : 3.3V**

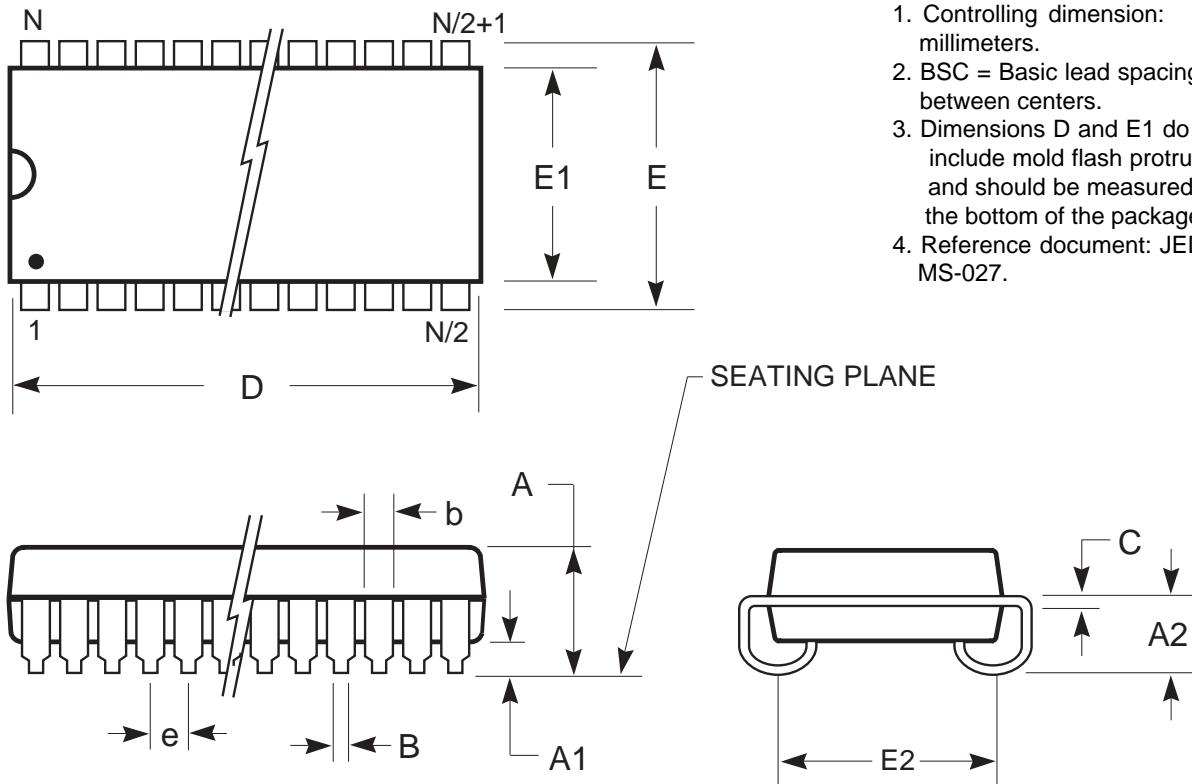
**Commercial Range: 0°C to +70°C**

<b>Speed(ns)</b>	<b>Order Part No.</b>	<b>Package</b>
35	IS41LV16256A-35K	400-mil SOJ
	IS41LV16256A-35KL	400-mil SOJ, Lead-free
	IS41LV16256A-35T	400-mil TSOP (Type II)
	IS41LV16256A-35TL	400-mil TSOP (Type II), Lead-free
60	IS41LV16256A-60K	400-mil SOJ
	IS41LV16256A-60KL	400-mil SOJ, Lead-free
	IS41LV16256A-60T	400-mil TSOP (Type II)
	IS41LV16256A-60TL	400-mil TSOP (Type II), Lead-free

# PACKAGING INFORMATION

**ISSI®**

400-mil Plastic SOJ  
Package Code: K



Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads (N)	28		32		36							
A	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	—	0.025	—	0.64	—	0.025	—	0.64	—	0.025	—
A2	2.08	—	0.082	—	2.08	—	0.082	—	2.08	—	0.082	—
B	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
C	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	18.29	18.54	0.720	0.730	20.82	21.08	0.820	0.830	23.37	23.62	0.920	0.930
E	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC	
e	1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC	

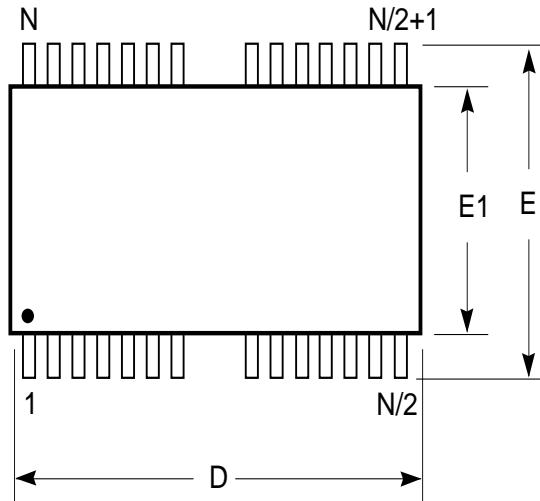
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Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads (N)	40		42		44							
A	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	—	0.025	—	0.64	—	0.025	—	0.64	—	0.025	—
A2	2.08	—	0.082	—	2.08	—	0.082	—	2.08	—	0.082	—
B	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
C	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	25.91	26.16	1.020	1.030	27.18	27.43	1.070	1.080	28.45	28.70	1.120	1.130
E	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC	
e	1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC	

## PACKAGING INFORMATION

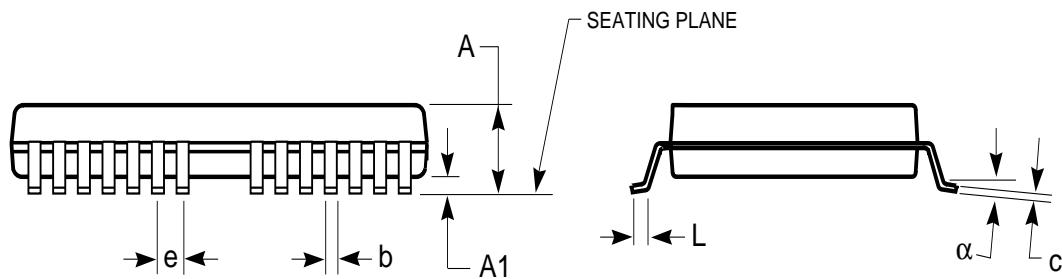
## Plastic TSOP

## Package Code: T (Type II)



## Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D1 and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



## Plastic TSOP (T - Type II) (MS 25)

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
Ref. Std.				
N	24/26			
A	1.20		0.0472	
A1	0.05	0.15	0.002	0.0059
b	0.30	0.51	0.012	0.0201
c	0.12	0.21	0.005	0.0083
D	17.01	17.27	0.670	0.6899
E <sub>1</sub>	7.49	7.75	0.295	0.3051
e	1.27	BSC	0.050	BSC
E	9.02	9.42	0.462	0.4701
L	0.40	0.60	0.016	0.0236
α	0°	5°	0°	5°

## Plastic TSOP (T - Type II) (MS 24)

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
Ref. Std.				
N	40/44			
A	1.20		0.0472	
A1	0.05	0.15	0.002	0.0059
b	0.30	0.45	0.012	0.0157
c	0.12	0.21	0.005	0.0083
D	18.31	18.51	0.721	0.7287
E <sub>1</sub>	10.06	10.26	0.396	0.4040
e	0.80	BSC	0.031	BSC
E	11.56	11.96	0.455	0.4709
L	0.40	0.60	0.016	0.0236
α	0°	8°	0°	8°

## Plastic TSOP (T - Type II) (MS 24)

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
Ref. Std.				
N	44/50			
A	1.20		0.0472	
A1	0.05	0.15	0.002	0.0059
b	0.30	0.45	0.012	0.0157
c	0.12	0.21	0.005	0.0083
D	20.85	21.05	0.821	0.8287
E <sub>1</sub>	10.06	10.26	0.396	0.4040
e	0.80	BSC	0.031	BSC
E	11.56	11.96	0.455	0.4709
L	0.40	0.60	0.016	0.0236
α	0°	8°	0°	8°