

RoHS Compliant

CFast

Product Specifications

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Version 1.1



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Features:

- **Standard Serial ATA 2.6 (Gen. 2)**
 - SATA II, 3.0 Gbps
 - ATA-compatible command set
 - ATA modes support
- **Connector type**
 - 7 + 17 pin female connector
- **Power consumption (typical)****
 - Supply voltage: 3.3V
 - Active mode: 360 mA
 - Idle mode: 85 mA
- **Performance****
 - Sustained read: Up to 160 MB/sec
 - Sustained write: Up to 140 MB/sec
- **Capacity**
 - 4, 8, 16, 32, 64 GB
- **NAND Flash Type: SLC**
- **MTBF: >2,000,000**
- **Temperature ranges**
 - Operation:
 - Standard: 0 °C to 70 °C
 - ET*: -40 °C to 85 °C
 - Storage: -40 °C to 100 °C
- **Intelligent endurance design**
 - Built-in hardware ECC, enabling up to 16/24 bit correction per 1K bytes
 - Dynamic/Static wear-leveling scheme together with dynamical block allocation to significantly increase the lifetime of a flash device and optimize the disk performance
 - Flash bad-block management
 - S.M.A.R.T.
 - Power Failure Management
 - ATA Secure Erase
 - TRIM
- **RoHS Compliant**

*Extended Temperature

**Vary from capacities. The values presented in Power consumption and Performances are typical, and may vary depending on different settings and platforms.

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1. General Description

CFast emerges as the evolution of the CompactFlash card, by adopting SATA transfer bus rather than PATA, which delivers a much higher data transfer rate required in industrial and enterprise storage usages. Although not backward compatible with its former CF form factor, CFast proves to be a more advanced embedded solution for cache, storage acceleration, communication and networking applications that require small physical fit.

Apacer CFast is designed with a powerful controller that easily breaks the performance limit for CompactFlash by delivering the transfer rate up to 160 MB/s while maintaining the reliability and power efficiency inherited from its former. Leveraging from CompactFlash form factor and SATA interface, CFast can be integrated into host computing system without excessive BIOS configurations and driver installations.

In addition to its performance, Apacer CFast is designed with reliability and data integrity. The CFast card adopts static wear-leveling to average the use of all flash blocks to prolong the lifetime and improve block efficiency of flash media. A built-in powerful ECC engine operates at hardware level for error correction and detection. With its well-organized architecture, CFast is an ideal storage device for industrial, enterprise and mobile applications.

2. Functional Block

Apacer CFast includes a single-chip SATA II Controller and the flash media. The controller integrates the flash management unit to support multi-channel, multi-bank flash arrays. Figure 2-1 shows the functional block diagram.

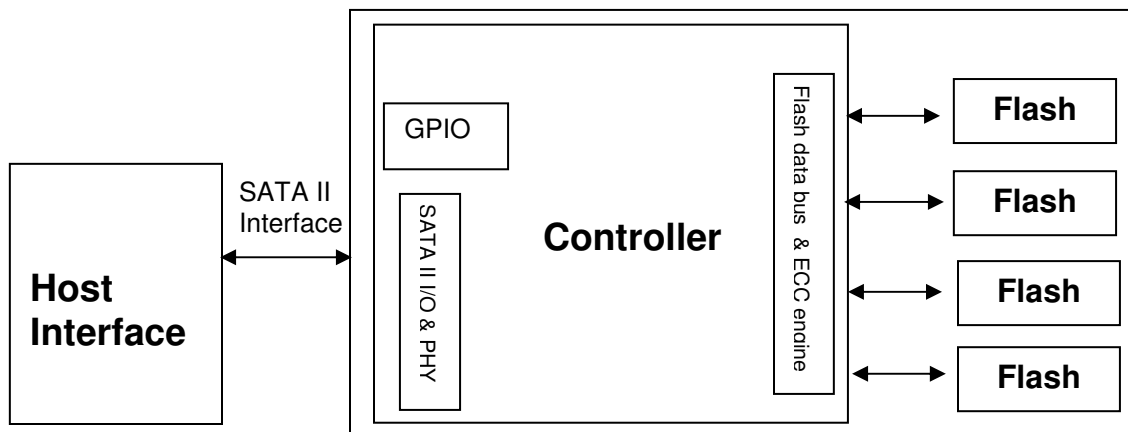


Figure 2-1 Apacer CFast block diagram

3. Pin Assignments

Table 3-1 describes CFast signal segment, and Table 3-2, its power segment.

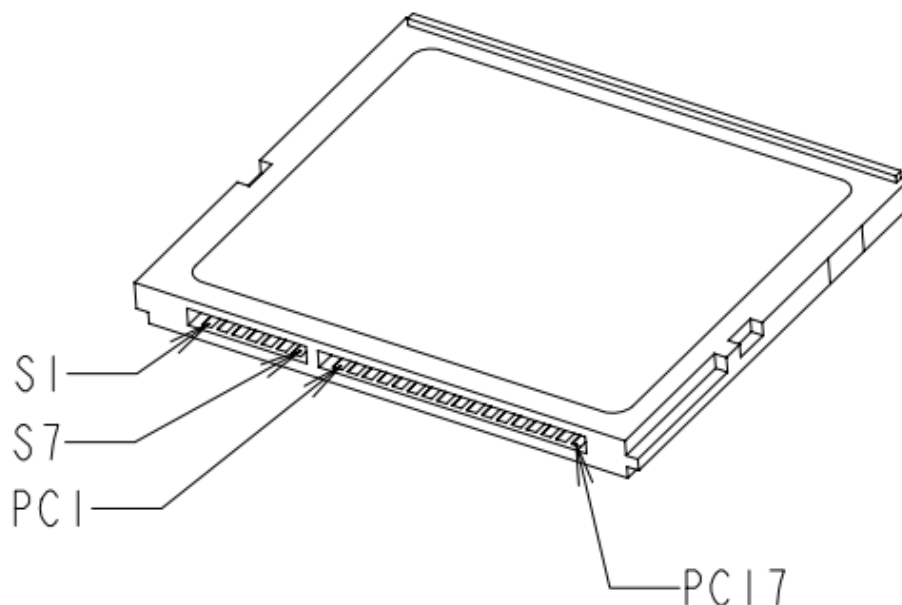


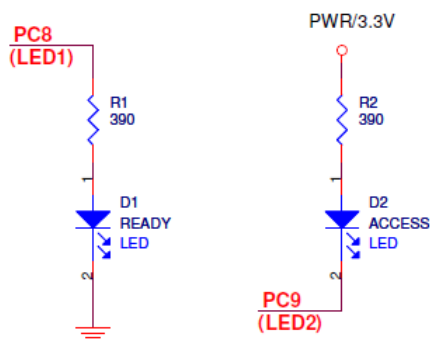
Figure 3-1 Pin Assignment

Table 3-1: Signal segment

PinC	Type	Description
S1	GND	
S2	A+	SATA Differential Signal Pair A
S3	A-	
S4	GND	
S5	B-	SATA Differential Signal Pair B
S6	B+	
S7	GND	

Table 3-2: Power segment

Pin	Name	Type	Description
PC1	CDI	CMOS Input	Card Detect In
PC2	GND	Device GND	
PC3	TBD	TBD	
PC4	TBD	TBD	
PC5	TBD	TBD	
PC6	TBD	TBD	
PC7	GND	Device GND	
PC8*	LED1	LED Output	Ready
PC9*	LED2	LED Output	Access
PC10	IO1	CMOS I/O	Reserved I/O
PC11	IO2	CMOS I/O	Write Protect**
PC12	IO3	CMOS I/O	Reserved I/O
PC13	PWR	3.3V	Device Power (3.3V)
PC14	PWR	3.3V	Device Power (3.3V)
PC15	PGND	Device GND	Device GND
PC16	PGND	Device GND	Device GND
PC17	CDO	CMOS Output	Card Detect Out



*Refer above for LED output design guide

**Enabled by adjusting the pin "PC11" from high to low active

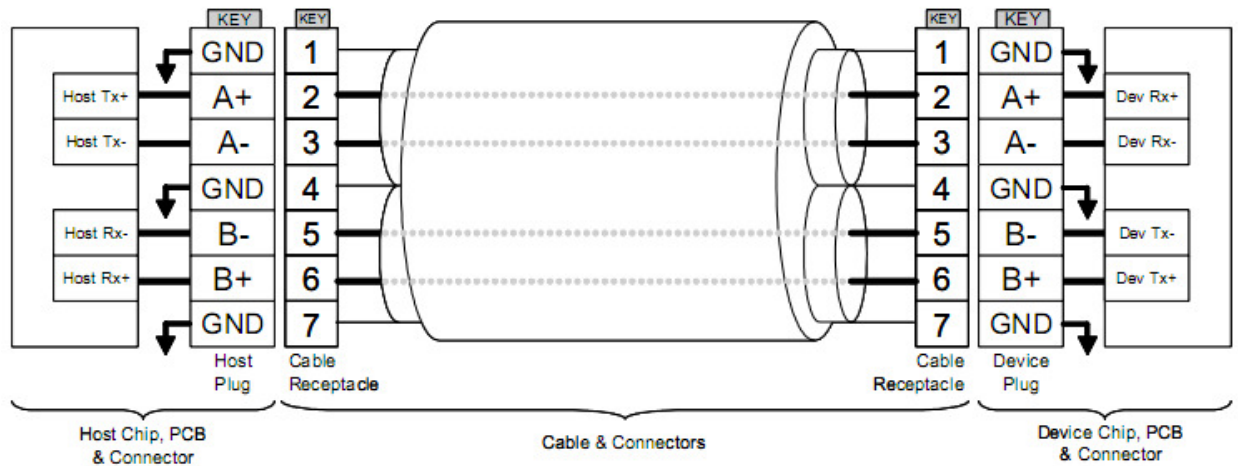


Figure 3-2 SATA Cable / Connector Connection Diagram

The connector on the left represents the Host with TX/RX differential pairs connected to a cable while the connector on the right shows the Device with TX/RX differential pairs also connected to the cable. Notice also the ground path connecting the shielding of the cable to the Cable Receptacle.

4. Capacity Specification

Capacity specification of the CFast is available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1: Capacity specifications

Capacity	Total bytes*	Cylinders	Heads	Sectors	Max LBA
4 GB	4,011,614,208	7773	16	63	7,835,184
8 GB	8,012,390,400	15525	16	63	15,649,200
16 GB	16,013,942,784	16383	16	63	31,277,232
32 GB	32,017,047,552	16383	16	63	62,533,296
64 GB	64,023,257,088	16383	16	63	125,045,424

*Display of total bytes varies from file systems.

**Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies

4.1 Performance

Performance of CFast product family is available as shown in Table 4-2.

Table 4-2: Performance table

<div>Capacity</div> <div>Performance</div>	4 GB	8 GB	16 GB	32 GB	64 GB
Sustained Read (MB/s)	140	150	150	160	160
Sustained Write (MB/s)	55	100	100	140	140

Note: Performances results are measured by CrystalDiskMark under Windows XP SP3 and may vary from host system configurations.

4.2 Environmental Specifications

Environmental specification of the CFast follows the MIL-STD-810F testing standards, shown in Table 4-3.

Table 4-3 Environmental specification

Environment		Specification
Temperature	Operation	0 °C to 70 °C (Standard); -40 °C to 85 °C (Extended Temperature)
	Storage	-40 °C to 100 °C
Humidity		5% to 95% RH (Non-condensing)
Vibration (Non-Operating)		Sine wave : 10~2000Hz, 15G (X, Y, Z axis)
Shock (Non-Operating)		Half sine wave, 1500 G (X, Y, Z ; All 6 axis)

Note: this Environmental Specification table indicates the conditions for testing the device. Real world usages may affect the results.

4.3 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in CFast. Serving as statistical reference, the prediction result for CFast is more than 2,000,000 hours.

Notes about the MTBF:

The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 2” method.

4.4 Certification and Compliance

CFast complies with the following standards

- CE
- FCC
- RoHS
- MIL-STD
- SATA II (SATA Rev. 2.6)
- Up to ATA/ATAPI-7 (including S.M.A.R.T.)

5. Flash Management

5.1 Error Correction/Detection

CFast implements a hardware ECC which is based on the BCH algorithm. It can detect and correct up to 16 bits or 24 bits error in 1K bytes depending on the NAND flash configuration used.

5.2 Bad Block Management

Although bad blocks on the flash media are already identified by the flash manufacturer, they can also be accumulated over time during operation. CFast's controller maintains a table that lists those normal blocks with disk data, the free blocks for wear leveling, and bad blocks with errors. When a normal block is detected with error, it is replaced with a free block and listed as a bad block. When a free block is detected with error, it is then removed from the free block list and marked as a bad block.

During device operation, this ensures that newly accumulated bad blocks are transparent to the host. The device will stop file write service once there are only two free blocks left; such that the read function is still available for copying the files from the disk into another.

5.3 Wear Leveling

The NAND flash devices are limited by a certain number of write cycles. When using a FAT-based file system, frequent FAT table updates are required. If some area on the flash wears out faster than others, it would significantly reduce the lifetime of the whole SSD; even if the erase counts of others are far from the write cycle limit. Thus, if the write cycles can be distributed evenly across the media, the lifetime of the media can be prolonged significantly. This algorithm is called wear leveling.

Apacer's wear-leveling scheme is achieved both via buffer management and Apacer-specific dynamic/static global wear leveling to ensure the lifetime of the flash media can be increased and the disk access performance is optimized as well.

5.4 Power Failure Management

The Low Power Detection on the controller initiates cached data saving before the power supply to the device is too low. This feature prevents the device from malfunctioning and ensures data integrity during an unexpected blackout. Once power failure happens before cached data completes writing back into flash, data in the cache will be lost. Once power resumes, the controller will check these fragmented data segment, and, if necessary, replace them with old data kept in flash until programmed successfully.

5.5 ATA Secure Erase

Accomplished by the Secure Erase (SE) command, which is added to the open ANSI standards that control disk drives, "ATA Secure Erase" is built into the disk drive itself and thus far less susceptible to malicious software attacks than external software utilities. It is an easy-to-use data destroy command, amounting to electronic data shredding. Executing the command causes a drive to internally completely erase all possible user data. This command is carried out within disk drives, so no additional software is required. Once executed, neither data nor the erase counter on the device would be recoverable, which blurs the accuracy of device lifespan. The process to erase will not be stopped until finished even if power failure is encountered, and will be continued when power resumes.

5.6 S.M.A.R.T.

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure.

Apacer devices use the standard SMART command B0h to read data out from the drive to activate our SMART feature that complies with the ATA/ATAPI-7 specifications. Based on the SFF-8035i Rev. 2.0 specifications, Apacer SMART defines vendor-specified SMART Attribute IDs (A0 ~ A5, and 0C). They represent Initial bad block count, Bad block count, Spare block count, Maximum erase count, Average erase count and Power cycle. When the Apacer SMART Utility running on the host, it analyzes and reports the disk status to the host before the device reaches in critical condition.

5.7 TRIM

Made of millions of NAND flash cells, SSD can be written into groups called pages in 4K size generally, but can only be erased in larger groups called blocks of 128 pages or 512KB. These stipulations are partially the source of many performance issues. Until an address is used again, the SSD keeps track of every last bit of data that's written on it. The ATA-TRIM instruction tilts the balance in favor of the SSD. TRIM addresses a major part of the performance degradation issue over time that plagues all SSDs. A TRIM enabled drive running an OS with TRIM supported will stay closer to its peak performance over time.

6. Software Interface

6.1 ATA Command Set

Table 6-1 summarizes the ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 6-1: Command set

Code	Command	Code	Command
E5h	Check Power Mode	F3h	Security Erase Prepare
06h	Data Set Management	F4h	Security Erase Unit
90h	Execute Device Diagnostic	F5h	Security Freeze Lock
E7h	Flush Cache	F1h	Security Set Password
Eah	Flush Cache EXT	F2h	Security Unlock
Ech	Identify Device	70h	Seek
E3h	Idle	Efh	Set Features
E1h	Idle Immediate	C6h	Set Multiple Mode
91h	Initialize Device Parameters	E6h	Sleep
C8h	Read DMA	B0h	SMART
25h	Read DMA EXT	E2h	Standby
C4h	Read Multiple	E0h	Standby Immediate
29h	Read Multiple EXT	Cah	Write DMA
20h	Read Sector	35h	Write DMA EXT
24h	Read Sector EXT	C5h	Write Multiple
40h	Read Verify Sectors	39h	Write Multiple EXT
42h	Read Verify Sectors EXT	30h	Write Sector
10h	Recalibrate	34h	Write Sector EXT
F6h	Security Disable Password		

7. Electrical Specification

Caution: Absolute Maximum Stress Ratings – Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

7.1 Absolute Maximum Rating

Table 7-1 lists Absolute Maximum Rating of CFast.

Table 7-1: Absolute Maximum Rating

Parameter	Symbol	Min	Max	Units
Power Supply	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Output Voltage	Vout	-0.3	Vcc+0.3	V
Storage Temperature	Ts	-40	100	°C

7.2 Recommended Operation Conditions

Table 7-2 lists CFast recommended operation conditions.

Table 7-2: Recommended Operations Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	Vcc	3.0	3.3	3.6	V
Input Voltage	Vin	0	-	Vcc	V

7.3 Power Consumption

Table 7-3 Power consumption (typical)

Mode \ Capacity	4 GB	8 GB	16 GB	32 GB	64 GB
Active (mA)	250	320	345	325	360
Standby (mA)	85	85	85	85	85

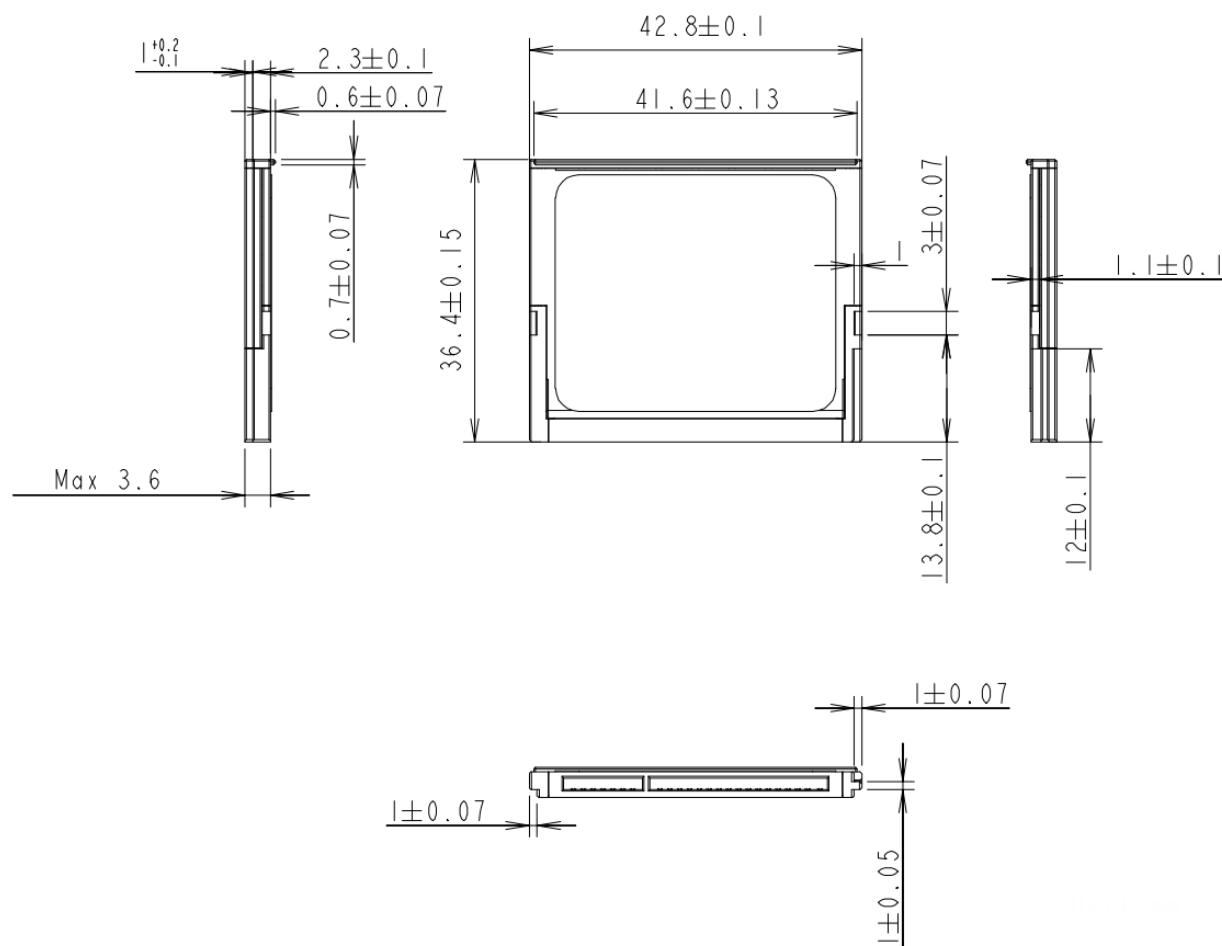
Note: Power consumption may vary from flash configurations and/or platform settings.

8. Physical Characteristics

8.1 Dimensions

TABLE 8-1: CFast physical specification

Length:	36.40 ±0.15 mm
Width:	42.80 ±0.10 mm
Thickness (Including Label Area):	3.6 mm (Max)



Unit: mm

FIGURE 8-1: Physical dimension

9.2 Valid Combinations

9.2.1 Standard

<i>Capacity</i>	<i>AP/N</i>	<i>AP/N—Extended Temp.</i>
4GB	APCFA004GTAHS-AT	APCFA004GTAHS-ETAT
8GB	APCFA008GTAHS-AT	APCFA008GTAHS-ETAT
16GB	APCFA016GTAHS-AT	APCFA016GTAHS-ETAT
32GB	APCFA032GTAHS-AC	APCFA032GTAHS-ETAC
64GB	APCFA064GTAHS-AC	APCFA064GTAHS-ETAC

Note:

- Valid combinations list out the available models for mass production.
- Products are normally shipped in unformatted capacities unless required otherwise.
- For customization request, please consult with Apacer sales representatives.

Revision History

Revision	Date	Description	Remark
1.0	05/20/2012	Official release	
1.1	05/29/2012	Added notes about hardware write protect in pin assignment Revised General Description	

Global Presence

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