MCH12140, MCK12140

Phase-Frequency Detector

The MCH/K12140 is a phase frequency−detector intended for phase−locked loop applications which require a minimum amount of phase and frequency difference at lock. When used in conjunction with high performance VCO such as the MC100EL1648, a high bandwidth PLL can be realized. The device is functionally compatible with the MC12040 phase−frequency detector with the maximum frequency extending to 800 MHz.

When the Reference (R) and VCO (V) inputs are unequal in frequency and/or phase, the differential UP (U) and DOWN (D) outputs will provide pulse streams which when subtracted and integrated provide an error voltage for control of a VCO. See AND8040 for further information. The device is packaged in a small outline, surface mount 8−lead SOIC package. There are two versions of the device to provide I/O compatibility to the two existing ECL standards. The MCH12140 is compatible with MECL 10H logic levels while the MCK12140 is compatible to 100 K ECL logic levels. This device can also be used in +5.0 V systems. See AND8020 for termination information

Features

- 800 MHz Typical Bandwidth
- Small Outline 8-Lead SOIC Package
- 75 kΩ Internal Input Pulldown Resistors
- >1000 V ESD Protection
- Pb−Free Package is Available

For proper operation, the input edge rate of the R and V inputs should be less than 5.0 ns.

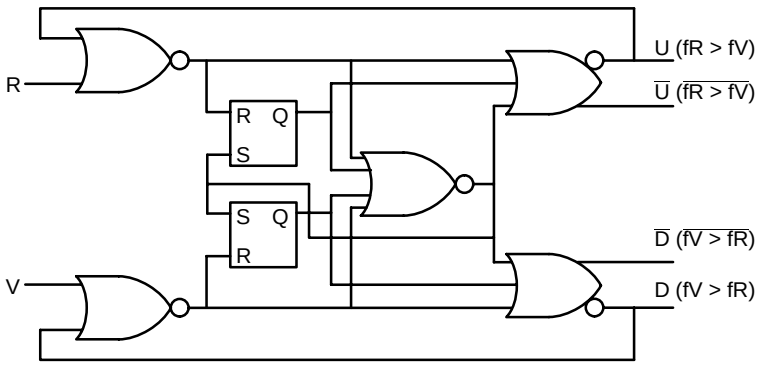

Figure 1. Logic Diagram

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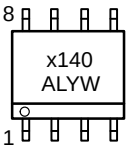
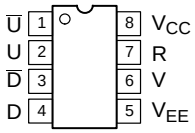
MARKING DIAGRAM

SOIC−8
D SUFFIX
CASE 751



x = H or K
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
MCH12140D	SOIC−8	98 Units/Rail
MCH12140DR2	SOIC−8	2500 Tape & Reel
MCH12140DR2G	SOIC−8 (Pb−Free)	2500 Tape & Reel
MCK12140D	SOIC−8	98 Units/Rail
MCK12140DR2	SOIC−8	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TRUTH TABLE*

Input		Output				Input		Output			
R	V	U	D	U	D	R	V	U	D	U	D
0	0	X	X	X	X	1	1	0	0	1	1
0	1	X	X	X	X	1	0	0	0	1	1
1	1	X	X	X	X	1	1	0	1	1	0
0	1	X	X	X	X	1	0	0	1	1	0
1	1	1	0	0	1	1	1	0	1	1	0
0	1	1	0	0	1	0	1	0	1	1	0
1	1	1	0	0	1	1	1	0	0	1	1
1	0	1	0	0	1						

*This is not strictly a functional table; i.e., it does not cover all possible modes of operation. However, it gives a sufficient number of tests to ensure that the device will function properly.

H−SERIES DC CHARACTERISTICS (V_{EE} = V_{EE}(min) − V_{EE}(max); V_{CC} = GND (Note 1), unless otherwise noted.)

Characteristic	Symbol	−40°C		0°C		25°C		70°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Output HIGH Voltage	V_{OH}	−1080	−890	−1020	−840	−980	−810	−910	−720	mV
Output LOW Voltage	V_{OL}	−1950	−1650	−1950	−1630	−1950	−1630	−1950	−1595	mV
Input HIGH Voltage	V_{IH}	−1230	−890	−1170	−840	−1130	−810	−1060	−720	mV
Input LOW Voltage	V_{IL}	−1950	−1500	−1950	−1480	−1950	−1480	−1950	−1445	mV
Input LOW Current	I_{IL}	0.5	−	0.5	−	0.5	−	0.3	−	μA

K−SERIES DC CHARACTERISTICS (V_{EE} = V_{EE}(min) − V_{EE}(max); V_{CC} = GND (Note 2), unless otherwise noted.)

Characteristic	Symbol	−40°C			0°C to 70°C			Condition	Unit
		Min	Typ	Max	Min	Typ	Max		
Output HIGH Voltage	V_{OH}	−1085	−1005	−880	−1025	−955	−880	V_{IN} = V_{IH}(max)	mV
Output LOW Voltage	V_{OL}	−1830	−1695	−1555	−1810	−1705	−1620	or V_{IL}(min)	mV
Output HIGH Voltage	V_{OHA}	−1095	−	−	−1035	−	−	V_{IN} = V_{IH}(min)	mV
Output LOW Voltage	V_{OLA}	−	−	−1555	−	−	−1610	or V_{IL}(max)	mV
Input HIGH Voltage	V_{IH}	−1165	−	−880	−1165	−	−880	−	mV
Input LOW Voltage	V_{IL}	−1810	−	−1475	−1810	−	−1475	−	mV
Input LOW Current	I_{IL}	0.5	−	−	0.5	−	−	V_{IN} = V_{IL}(max)	μA

MAXIMUM RATINGS (Note 3)

Rating	Symbol	Value	Unit
Power Supply (V_{CC} = 0 V)	V_{EE}	−8.0 to 0	VDC
Input Voltage (V_{CC} = 0 V)	V_I	0 to −6.0	VDC
Output Current Continuous Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	−40 to +70	°C
Operating Range (Notes 3 and 4)	V_{EE}	−5.7 to −4.2	V

NOTE: ESD data available upon request.

1. 10H circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained. Outputs are terminated through a 50 Ω resistor to −2.0 V except where otherwise specified on the individual data sheets.
2. This table replaces the three tables traditionally seen in ECL 100 K data books. The same DC parameter values at V_{EE} = −4.5 V now apply across the full V_{EE} range of −4.2 V to −5.5 V. Outputs are terminated through a 50 Ω resistor to −2.0 V except where otherwise specified on the individual data sheets.
3. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.
4. Parametric values specified at: H−Series: −4.20 V to −5.50 V
   K−Series: −4.94 V to −5.50 V

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) − V_{EE}(max); V_{CC} = GND, unless otherwise noted.)

Characteristic		Symbol	−40°C			0°C			25°C			70°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply Current	H	I_{EE}	−	45	−	38	45	52	38	45	52	38	45	52	mA
	K		−	45	−	38	45	52	38	45	52	42	50	58	
Power Supply Voltage	H	V_{EE}	−4.75	−5.2	−5.5	−4.75	−5.2	−5.5	−4.75	−5.2	−5.5	−4.75	−5.2	−5.5	V
	K		−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	
Input HIGH Current		I_{IH}	−	−	150	−	−	150	−	−	150	−	−	150	μA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) − V_{EE}(max); V_{CC} = GND, unless otherwise noted.)

Characteristic		Symbol	−40°C			0°C			25°C			70°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Maximum Toggle Frequency		F_{MAX}	−	800	−	650	800	−	650	800	−	650	800	−	−
Propagation Delay to Output	R to D	t_{PLH}	−	440	−	320	440	580	320	440	580	360	480	620	ps
	R to U	t_{PHL}	−	330	−	210	330	470	210	330	470	240	360	500	
	V to D		−	330	−	210	330	470	210	330	470	240	360	500	
	V to U		−	440	−	320	440	580	320	440	580	360	480	620	
Output Rise/Fall Times Q (20 to 80%)		t_r t_f	−	225	−	100	225	350	100	225	350	100	225	350	ps

APPLICATIONS INFORMATION

The 12140 is a high speed digital circuit used as a phase comparator in an analog phase-locked loop. The device determines the “lead” or “lag” phase relationship and time difference between the leading edges of a VCO (V) signal and a Reference (R) input. Since these edges occur only once per cycle, the detector has a range of ±2π radians.

The operation of the 12140 can best be described using the plots of Figure 2. Figure 2 plots the average value of $\overline{U}$, $\overline{D}$ and the difference between $\overline{U}$ and $\overline{D}$ versus the phase difference between the V and R inputs.

There are four potential relationships between V and R: R lags or leads V and the frequency of R is less than or greater than the frequency of V. Under these four conditions the 12140 will function as follows:

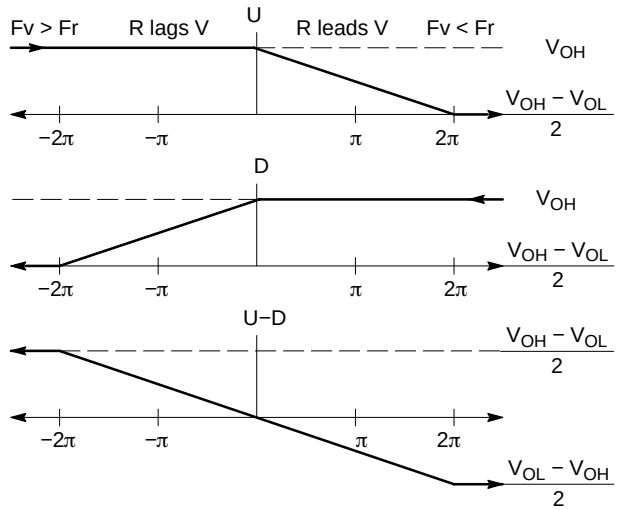


Figure 2. Average Output Voltage vs. Phase Difference

R lags V in phase

When the R and V inputs are equal in frequency and the phase of R lags that of V the $\overline{U}$ output will stay HIGH while the $\overline{D}$ output will pulse from HIGH to LOW. The magnitude of the pulse will be proportional to the phase difference between the V and R inputs reaching a minimum 50% duty cycle under a 180° out of phase condition. The signal on $\overline{D}$ indicates to the VCO to decrease in frequency to bring the loop into lock.

V frequency > R frequency

When the frequency of V is greater than that of R the 12140 behaves in a similar fashion as above. Again the signal on $\overline{D}$ indicates that the VCO frequency must be decreased to bring the loop into lock.

R leads V in phase

When the R and V inputs are equal in frequency and the phase of R leads that of V the $\overline{D}$ output will stay HIGH while the $\overline{U}$ output pulses from HIGH to LOW. The magnitude of the pulse will be proportional to the phase difference between the V and R inputs reaching a minimum 50% duty cycle under a 180° out of phase condition. The signal on $\overline{U}$ indicates to the VCO to increase in frequency to bring the loop into lock.

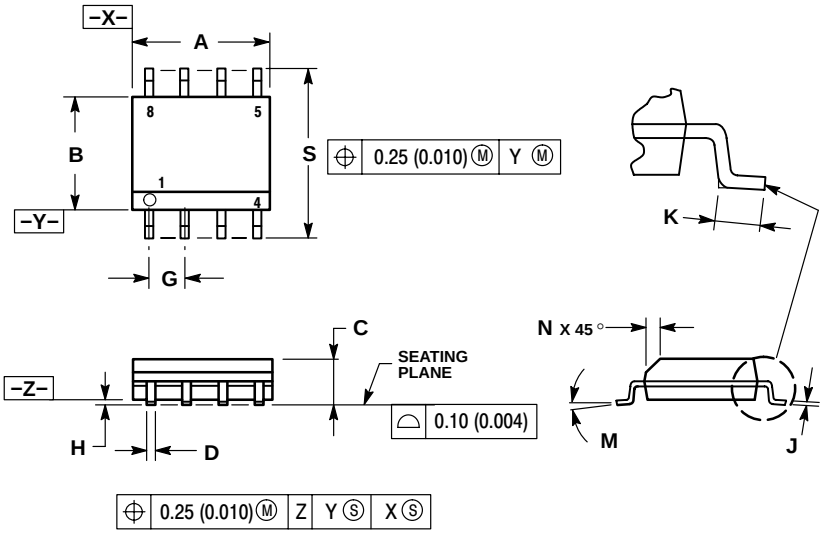
V frequency < R frequency

When the frequency of V is less than that of R the 12140 behaves in a similar fashion as above. Again the signal on $\overline{U}$ indicates that the VCO frequency must be decreased to bring the loop into lock.

From Figure 2 when V and R are at the same frequency and in phase the value of $\overline{U} - \overline{D}$ is zero thus providing a zero error voltage to the VCO. This situation indicates the loop is in lock and the 12140 action will maintain the loop in its locked state.

PACKAGE DIMENSIONS

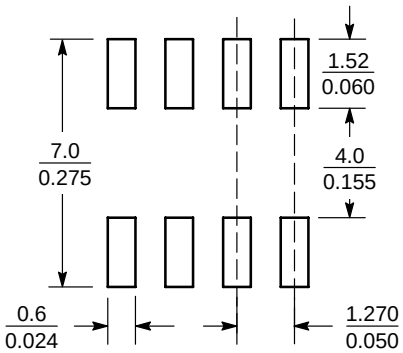
SOIC−8
D SUFFIX
CASE 751−07
ISSUE AB



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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