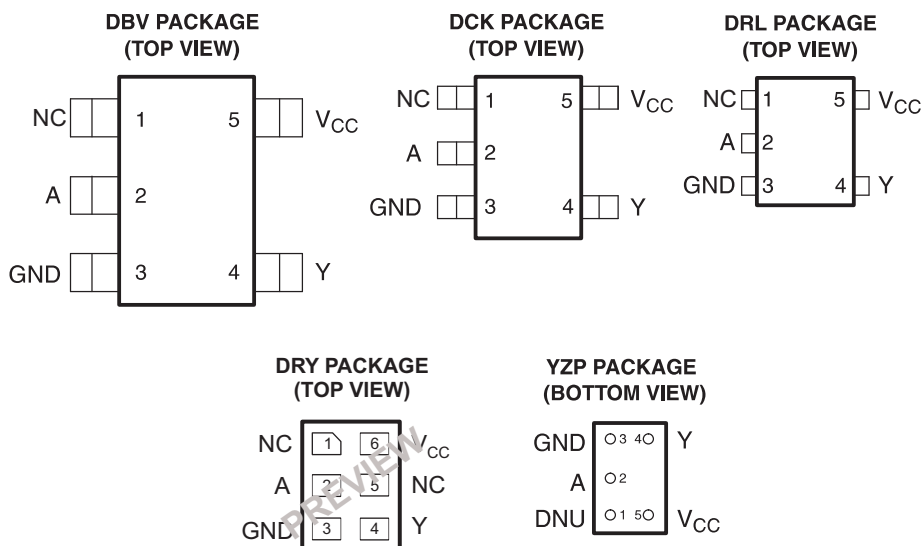


FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t_{pd} of 2.2 ns at 1.8 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 8 -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



NC – No internal connection
See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single inverter gate is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC1G04 performs the Boolean function $Y = \bar{A}$.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the output, preventing damaging current backflow through the device when it is powered down.

For more information about AUC Little Logic devices, please refer to the TI application report, *Applications of Texas Instruments AUC Sub-1-V Little Logic Devices*, literature number SCEA027.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

SN74AUC1G04

SINGLE INVERTER GATE

SCES370Q–SEPTEMBER 2001–REVISED APRIL 2007

ORDERING INFORMATION

| T _A | PACKAGE ⁽¹⁾⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING ⁽³⁾ |
|----------------|---|--------------|-----------------------|---------------------------------|
| –40°C to 85°C | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | Reel of 3000 | SN74AUC1G04YZPR | _ _ _UC_ |
| | SON – DRY | Reel of 5000 | SN74AUC1G04DRYR | PREVIEW |
| | SOT (SOT-23) – DBV | Reel of 3000 | SN74AUC1G04DBVR | U04_ |
| | SOT (SC-70) – DCK | Reel of 3000 | SN74AUC1G04DCKR | UC_ |
| | SOT (SOT-553) – DRL | Reel of 4000 | SN74AUC1G04DRLR | UC_ |

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (3) DBV/DCK/DRL/DRY: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|--------------------|-----------------------|---------|
| V _{CC} | Supply voltage range | –0.5 | 3.6 | V |
| V _I | Input voltage range ⁽²⁾ | –0.5 | 3.6 | V |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | –0.5 | 3.6 | V |
| | Output voltage range ⁽²⁾ | –0.5 | V _{CC} + 0.5 | |
| I _{IK} | Input clamp current | V _I < 0 | | –50 mA |
| I _{OK} | Output clamp current | V _O < 0 | | –50 mA |
| I _O | Continuous output current | | | ±20 mA |
| Continuous current through V _{CC} or GND | | | | ±100 mA |
| θ _{JA} | Package thermal impedance ⁽³⁾ | DBV package | | 206 |
| | | DCK package | | 252 |
| | | DRL package | | 142 |
| | | DRY package | | 234 |
| | | YZP package | | 132 |
| T _{stg} | Storage temperature range | –65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | | MIN | MAX | UNIT |
|-----------------|------------------------------------|-----------------------------------|------------------------|-----------------|------|
| V _{CC} | Supply voltage | | 0.8 | 2.7 | V |
| V _{IH} | High-level input voltage | V _{CC} = 0.8 V | V _{CC} | | V |
| | | V _{CC} = 1.1 V to 1.95 V | 0.65 × V _{CC} | | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 0.8 V | 0 | | V |
| | | V _{CC} = 1.1 V to 1.95 V | 0.35 × V _{CC} | | |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | | |
| V _I | Input voltage | | 0 | 3.6 | V |
| V _O | Output voltage | | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 0.8 V | −0.7 | | mA |
| | | V _{CC} = 1.1 V | −3 | | |
| | | V _{CC} = 1.4 V | −5 | | |
| | | V _{CC} = 1.65 V | −8 | | |
| | | V _{CC} = 2.3 V | −9 | | |
| I _{OL} | Low-level output current | V _{CC} = 0.8 V | 0.7 | | mA |
| | | V _{CC} = 1.1 V | 3 | | |
| | | V _{CC} = 1.4 V | 5 | | |
| | | V _{CC} = 1.65 V | 8 | | |
| | | V _{CC} = 2.3 V | 9 | | |
| Δt/Δv | Input transition rise or fall rate | | | 20 | ns/V |
| T _A | Operating free-air temperature | | −40 | 85 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|---------|---|-----------------|-----------------------|--------------------|------|------|
| V _{OH} | | I _{OH} = −100 μA | 0.8 V to 2.7 V | V _{CC} − 0.1 | | | V |
| | | I _{OH} = −0.7 mA | 0.8 V | 0.55 | | | |
| | | I _{OH} = −3 mA | 1.1 V | 0.8 | | | |
| | | I _{OH} = −5 mA | 1.4 V | 1 | | | |
| | | I _{OH} = −8 mA | 1.65 V | 1.2 | | | |
| | | I _{OH} = −9 mA | 2.3 V | 1.8 | | | |
| V _{OL} | | I _{OL} = 100 μA | 0.8 V to 2.7 V | | | 0.2 | V |
| | | I _{OL} = 0.7 mA | 0.8 V | 0.25 | | | |
| | | I _{OL} = 3 mA | 1.1 V | | | 0.3 | |
| | | I _{OL} = 5 mA | 1.4 V | | | 0.4 | |
| | | I _{OL} = 8 mA | 1.65 V | | | 0.45 | |
| | | I _{OL} = 9 mA | 2.3 V | | | 0.6 | |
| I _I | A input | V _I = V _{CC} or GND | 0 to 2.7 V | | | ±5 | μA |
| I _{off} | | V _I = V _O or 2.7 V | 0 | | | ±10 | μA |
| I _{CC} | | V _I = V _{CC} or GND, I _O = 0 | 0.8 V to 2.7 V | | | 10 | μA |
| C _i | | V _I = V _{CC} or GND | 2.5 V | 3 | | | pF |

(1) All typical values are at T_A = 25°C.

SN74AUC1G04

SINGLE INVERTER GATE

SCES370Q—SEPTEMBER 2001—REVISED APRIL 2007

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 0.8$ V | $V_{CC} = 1.2$ V ± 0.1 V | | $V_{CC} = 1.5$ V ± 0.1 V | | $V_{CC} = 1.8$ V ± 0.15 V | | | $V_{CC} = 2.5$ V ± 0.2 V | | UNIT |
|-----------|-----------------|----------------|------------------|---------------------------------|-----|---------------------------------|-----|----------------------------------|-----|-----|---------------------------------|-----|------|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | TYP | MAX | MIN | MAX | |
| t_{pd} | A | Y | 4.4 | 0.8 | 3 | 0.5 | 2 | 0.5 | 1 | 2.1 | 0.5 | 1.6 | ns |

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see [Figure 1](#))

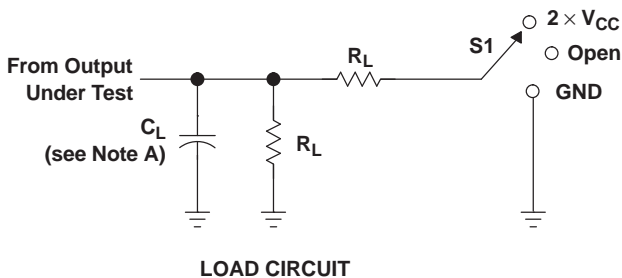
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 1.8$ V ± 0.15 V | | | $V_{CC} = 2.5$ V ± 0.2 V | | UNIT |
|-----------|-----------------|----------------|----------------------------------|-----|-----|---------------------------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| t_{pd} | A | Y | 0.6 | 1.2 | 2.2 | 0.5 | 1.9 | ns |

Operating Characteristics

$T_A = 25^\circ\text{C}$

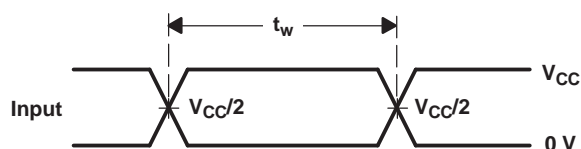
| PARAMETER | | TEST CONDITIONS | $V_{CC} = 0.8$ V | $V_{CC} = 1.2$ V | $V_{CC} = 1.5$ V | $V_{CC} = 1.8$ V | $V_{CC} = 2.5$ V | UNIT |
|-----------|-------------------------------|--------------------|------------------|------------------|------------------|------------------|------------------|------|
| | | | TYP | TYP | TYP | TYP | TYP | |
| C_{pd} | Power dissipation capacitance | $f = 10$ MHz | 14 | 14 | 14 | 14 | 19 | pF |

PARAMETER MEASUREMENT INFORMATION

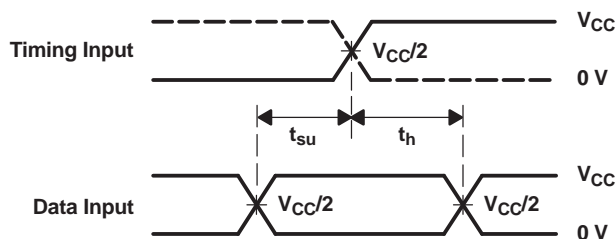


| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |

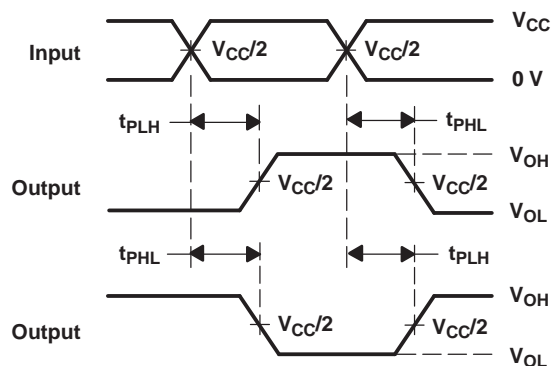
| V_{CC} | C_L | R_L | V_{Δ} |
|------------------------------------|-------|--------------|--------------|
| 0.8 V | 15 pF | 2 k Ω | 0.1 V |
| $1.2 \text{ V} \pm 0.1 \text{ V}$ | 15 pF | 2 k Ω | 0.1 V |
| $1.5 \text{ V} \pm 0.1 \text{ V}$ | 15 pF | 2 k Ω | 0.1 V |
| $1.8 \text{ V} \pm 0.15 \text{ V}$ | 15 pF | 2 k Ω | 0.15 V |
| $2.5 \text{ V} \pm 0.2 \text{ V}$ | 15 pF | 2 k Ω | 0.15 V |
| $1.8 \text{ V} \pm 0.15 \text{ V}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5 \text{ V} \pm 0.2 \text{ V}$ | 30 pF | 500 Ω | 0.15 V |



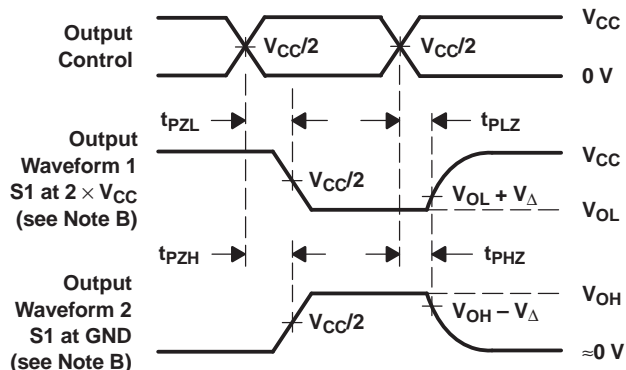
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, slew rate $\geq 1 \text{ V/ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SN74AUC1G04DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (U042 ~ U04R) | Samples |
| SN74AUC1G04DBVRE4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (U042 ~ U04R) | Samples |
| SN74AUC1G04DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (U042 ~ U04R) | Samples |
| SN74AUC1G04DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (UC5 ~ UCF ~ UCR) | Samples |
| SN74AUC1G04DCKRE4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (UC5 ~ UCF ~ UCR) | Samples |
| SN74AUC1G04DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (UC5 ~ UCF ~ UCR) | Samples |
| SN74AUC1G04DRLR | ACTIVE | SOT | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (UC7 ~ UCR) | Samples |
| SN74AUC1G04DRLRG4 | ACTIVE | SOT | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (UC7 ~ UCR) | Samples |
| SN74AUC1G04DRYR | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | UC | Samples |
| SN74AUC1G04YZPR | ACTIVE | DSBGA | YZP | 5 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (UC7 ~ UCN) | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AUC1G04DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUC1G04DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AUC1G04DRLR | SOT | DRL | 5 | 4000 | 180.0 | 9.5 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74AUC1G04DRLR | SOT | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74AUC1G04DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74AUC1G04YZPR | DSBGA | YZP | 5 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AUC1G04DBVR | SOT-23 | DBV | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUC1G04DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUC1G04DRLR | SOT | DRL | 5 | 4000 | 180.0 | 180.0 | 30.0 |
| SN74AUC1G04DRLR | SOT | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74AUC1G04DRYR | SON | DRY | 6 | 5000 | 180.0 | 180.0 | 30.0 |
| SN74AUC1G04YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 35.0 |

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



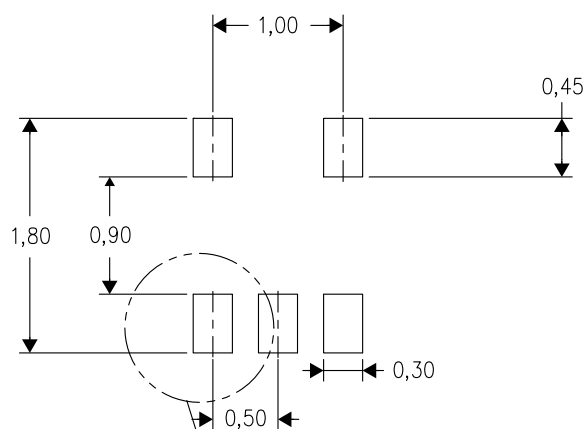
4205622-2/D 08/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

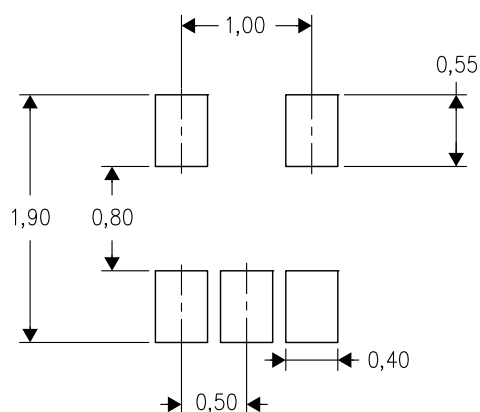
DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

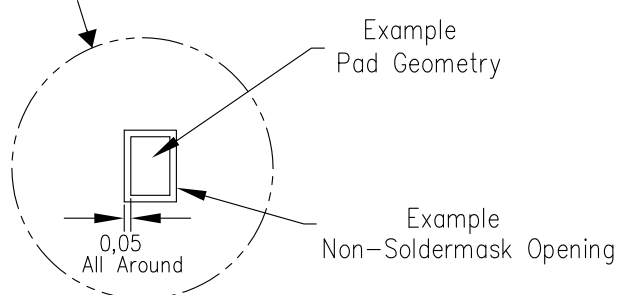
Example Board Layout



Example Stencil Design
(Note E)



Example
Non-Soldermask Defined Pad





4208207-2/E 06/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

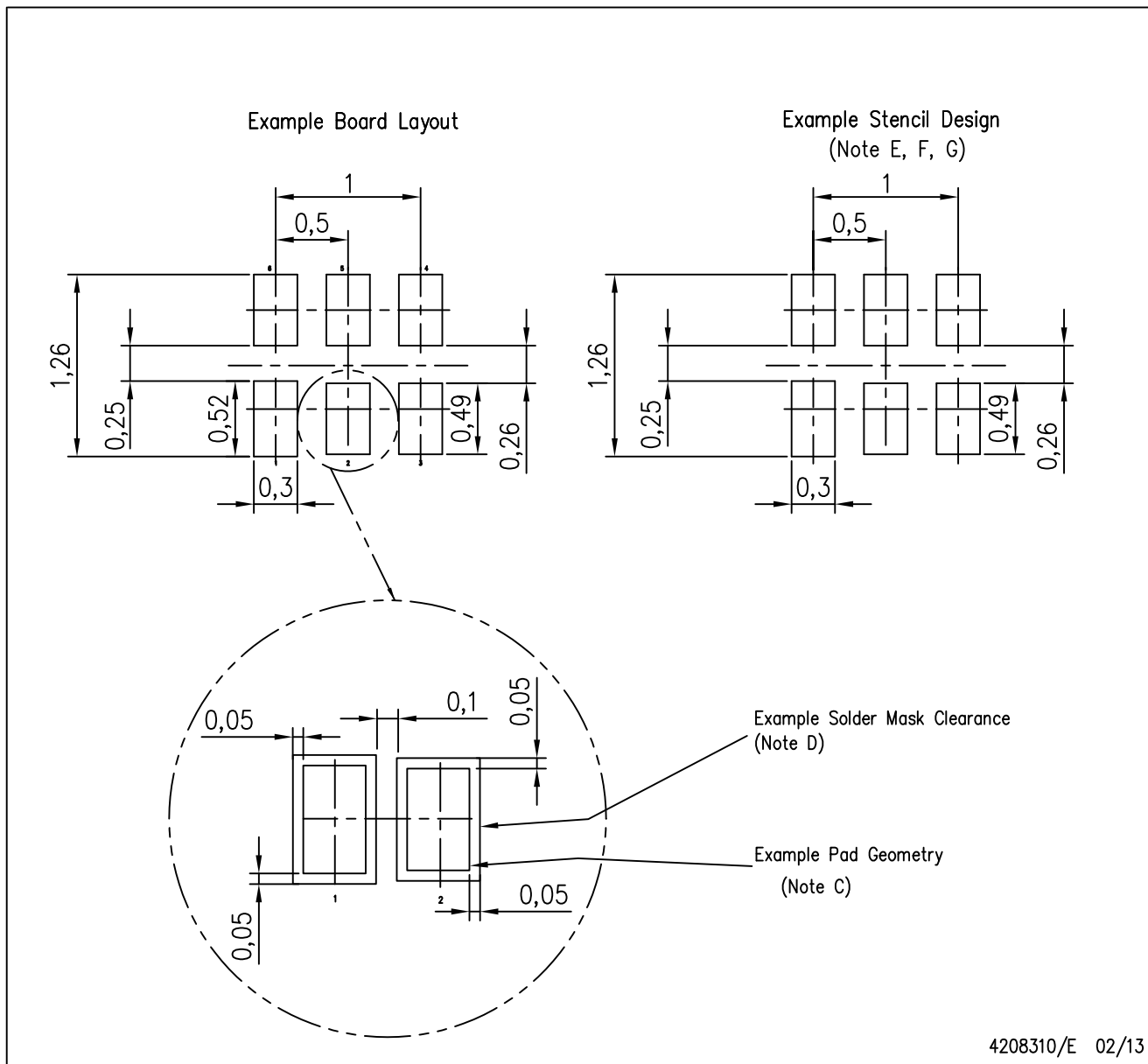


4207181/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 -  D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
 - E. This package complies to JEDEC MO-287 variation UFAD.
 -  F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R-PUSON-N6)

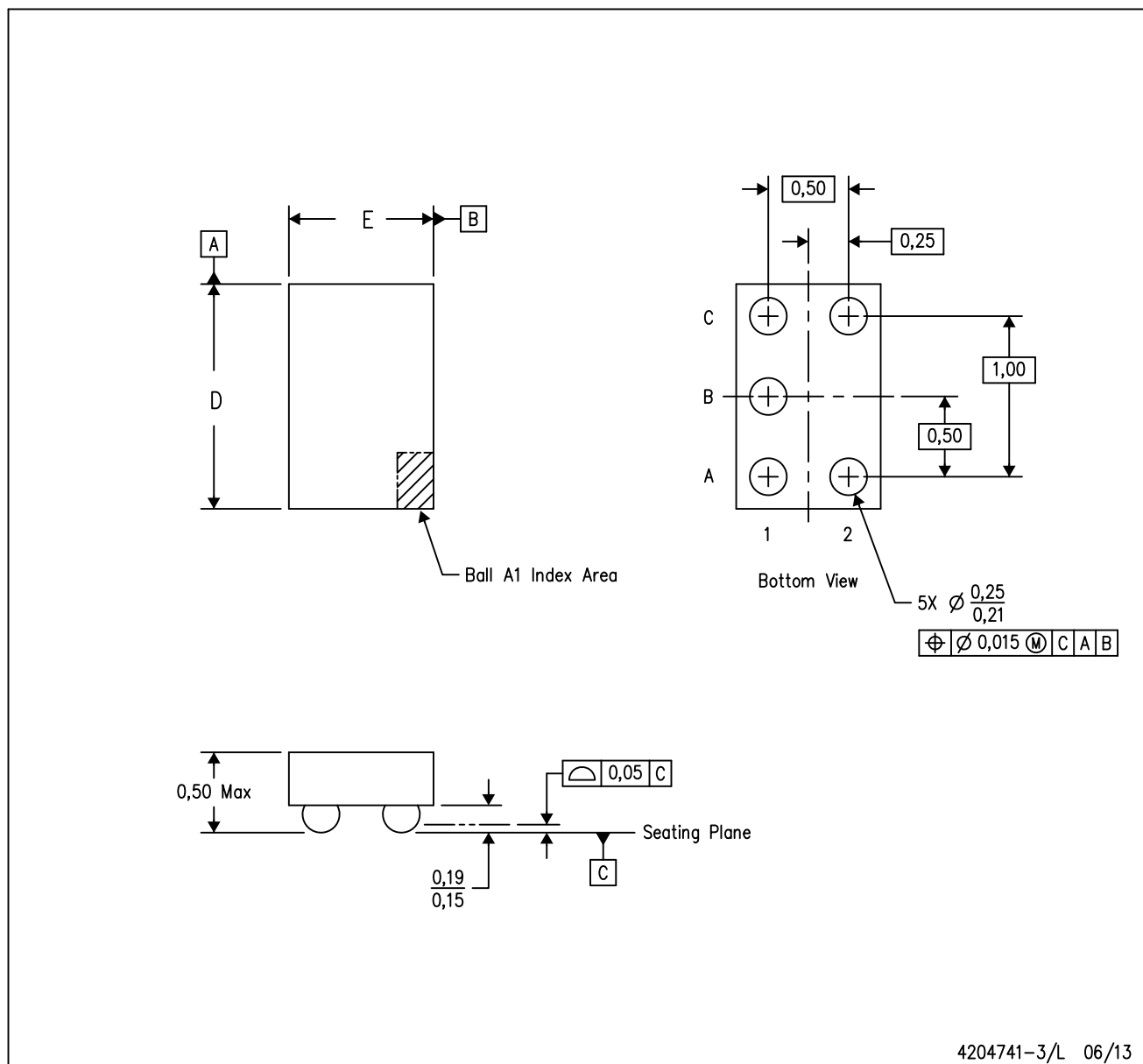
PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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