



13-Bit to 26-Bit Registered Buffer PC2700-/PC3200-Compliant

Features

- Differential clock inputs up to 280 MHz
- Supports LVTTTL switching levels on the RESET# pin
- Output drivers have controlled edge rates, so no external resistors are required.
- Two KV ESD protection
- Latch-up performance exceeds 100 mA per JESD78, Class II
- 64-pin TSSOP/JEDEC and 56-pin QFN package availability
- JEDEC specification supported

Description

This 13-bit to 26-bit registered buffer is designed for 2.3V to 2.7 VDD operations.

All inputs are compatible with the JEDEC Standard for SSTL-2, except the LVCMOS reset (RESET#) input. All outputs are SSTL_2, Class II compatible.

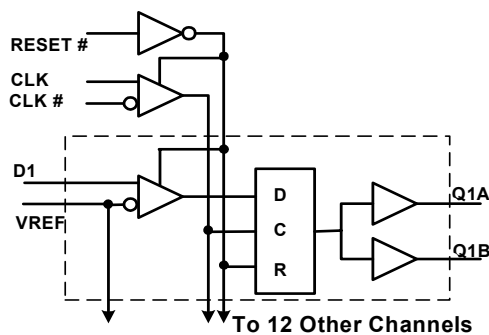
The CY2SSTV16859 operates from a differential clock (CLK and CLK#) of frequency up to 280 MHz. Data are registered at crossing of CLK going high and CLK# going low.

When RESET# is low, the differential input receivers are disabled, and undriven (floating) data and clock inputs are allowed. The LVCMOS RESET# input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, RESET# must be held in the low state during power up.

In the DDR DIMM application, RESET# is completely asynchronous with respect to CLK# and CLK. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register is cleared and the outputs are driven low quickly, relative to the time to disable the differential input receivers, thus ensuring no glitches on the output. However, when coming out of reset, the register becomes active quickly, relative to the time to enable the differential input receivers.

Block Diagram



Pin Configuration

Q13A	1	64	VDDQ
Q12A	2	63	GND
Q11A	3	62	D13
Q10A	4	61	D12
Q9A	5	60	VDD
VDDQ	6	59	VDDQ
GND	7	58	GND
Q8A	8	57	D11
Q7A	9	56	D10
Q6A	10	55	D9
Q5A	11	54	GND
Q4A	12	53	D8
Q3A	13	52	D7
Q2A	14	51	RESET #
GND	15	50	GND
Q1A	16	49	CLK #
Q13B	17	48	CLK
VDDQ	18	47	VDDQ
Q12B	19	46	VDD
Q11B	20	45	VREF
Q10B	21	44	D6
Q9B	22	43	GND
Q8B	23	42	D5
Q7B	24	41	D4
Q6B	25	40	D3
GND	26	39	GND
VDDQ	27	38	VDDQ
Q5B	28	37	VDD
Q4B	29	36	D2
Q3B	30	35	D1
Q2B	31	34	GND
Q1B	32	33	VDDQ

64 TSSOP Package



Absolute Maximum Conditions^[4,5]

Parameter	Description	Condition	Min.	Max.	Unit
$V_{TERM}^{[6]}$	Terminal Voltage with respect to V_{SS}		-0.5	3.6	V
$V_{TERM}^{[7]}$	Terminal Voltage with respect to V_{SS}		-0.5	$V_{DD} + 0.5$	V
T_{STG}	Storage Temperature		-65°	150°C	°C
I_{OUT}	DC Output Current		-50	50	mA
I_{IK}	Continuous Clamp Current	$V_I < 0$ or $V_I > V_{SS}$	-50	50	mA
I_{OK}	Continuous Clamp Current	$V_O < 0$ or $V_O > V_{DD}$	-50	50	mA
I_{dd} I_{SS}	Continuous Current through each V_{DD} , V_{DDQ} or V_{SS}		-100	100	mA

Recommended Operating Conditions^[8]

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	2.3	2.5	2.7	V
V_{DDQ}	Output supply voltage	2.3	2.5	2.7	V
	PC1600,PC2100,PC2700	2.5	2.6	2.7	V
V_{REF}	Reference voltage ($V_{REF} = V_{DDQ}/2$)	1.15	1.25	1.35	V
	PC3200	1.25	1.3	1.35	V
V_{TT}	Termination voltage	$V_{REF} - 40$ mV	V_{REF}	$V_{REF} + 40$ mV	V
V_I	Input voltage	0	–	V_{DD}	V
V_{IH}	AC Data Input high-level voltage	$V_{REF} + 310$ mV	–	–	V
V_{IL}	AC Data Input low-level voltage	–	–	$V_{REF} - 310$ mV	V
V_{IH}	DC Data Input high-level voltage	$V_{REF} + 150$ mV	–	–	V
V_{IL}	DC Data Input low-level voltage	–	–	$V_{REF} - 150$ mV	V
V_{IH}	RESET# Input high-level voltage	1.7	–	–	V
V_{IL}	RESET# Input low-level voltage	–	–	0.7	V
V_{ICR}	CLK, CLK# Common-mode input voltage range	0.97	–	1.53	V
$V_{I(PP)}$	CLK, CLK# Peak-to-peak input voltage	360	–	–	mV
I_{OH}	High-level output current	–	–	-20	mA
I_{OL}	Low-level output current	–	–	20	mA
T_A	Operating free-air temperature	0	–	85	°C

DC Electrical Specifications

Parameter	Description	Condition	VDD	Min.	Typ. ^[9]	Max.	Unit
V_{IK}	Clamp Voltage	$I_I = -18$ mA	2.3V	–	–	-1.2	V
V_{OH}	High level output voltage	$I_{OH} = -100$ μ A	2.3 to 2.7V	$V_{DD} - 0.2$	–	–	V
		$I_{OH} = -16$ mA	2.3V	1.95	–	–	V
V_{OL}	Low level output voltage	$I_{OL} = 100$ μ A	2.3 to 2.7V	–	–	0.2	V
		$I_{OL} = 16$ mA	2.3	–	–	0.35	V
I_I	All Inputs	$V_I = V_{DD}$ or V_{SS}	2.7V	–	–	± 5	μ A
I_{DD}	Static Standby	RESET# = V_{SS}	2.7V	–	–	10	μ A
	Static Operating	RESET# = V_{DD} , $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$	2.7	–	–	40.0	mA

Notes:

- The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
- Stresses greater than those listed under Absolute Maximum Conditions may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
- V_{DD}/V_{DDQ} terminals.
- All terminals except V_{DD} .
- The RESET# input of the device must be held at V_{DD} or V_{SS} to ensure proper device operation.
- All typical values are measured at $T_{AMB} = 25^\circ\text{C}$

DC Electrical Specifications (continued)

Parameter	Description	Condition	VDD	Min.	Typ. ^[9]	Max.	Unit
I _{DDD}	Dynamic operating – clock only	RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and CLK# switching 50% duty cycle	2.7V	–	30.0	–	μA/clock MHz
	Dynamic operating – per each data input	RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , CLK and CLK# switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycles.	2.7	–	15.0	–	μA/clock MHz /data input
r _{OH}	Output high	I _{OH} = –20 mA	2.3 to 2.7V	7	–	20	Ω
r _{OL}	Output low	I _{OL} = 20 mA	2.3 to 2.7V	7	–	20	Ω
r _{O(Δ)}	r _{OH} – r _{OL} each separate bit	I _O = 20 mA, T _A = 25°C	2.5V	–	–	4	Ω
C _i	Data Inputs	V _I = V _{REF} ± 310 mV	2.5	2.5	–	3.5	pF
	CLK and CLK#	V _{ICR} = 1.25V, V _{I(PP)} = 360 mV	2.5	2.5	–	3.5	pF
	RESET#	V _I = V _{DD} or V _{SS}	2.5	2.5	–	3.5	pF

AC Electrical Specifications

Parameter	Description		V _{DD} = 2.5V± 0.2V		Unit
			Min.	Max.	
f _{clock}	Clock Frequency		–	280	MHz
t _w	Pulse duration, CLK, CLK# high or low		2.0	–	ns
t _{act}	Differential inputs active time (data inputs must be held low after RESET# is taken high).		–	22	ns
t _{inact}	Differential inputs inactive time (data and clock inputs must be held at valid levels (not floating) after RESET# is taken low).		–	22	ns
t _{su}	Set-up time, fast slew rate ^[10, 12]	Data before CLK↑, CLK#↓	0.75	–	ns
	Set-up time, slow slew rate ^[11, 12]		0.9	–	ns
t _h	Hold time, fast slew rate ^[10, 12]	Data after CLK ↑, CLK#↓	0.75	–	ns
	Hold time, slow slew rate ^[11, 12]		0.9	–	ns

Table 2. Switching Characteristics Over Recommended Operating Conditions^[13]

Parameter	From (Input)	To (Output)	V _{DD} = 2.5V ± 0.2V		Unit
			Min.	Max.	
f _{max}			280	–	MHz
t _{PHL}	RESET#	Q		5	ns
t _{PD}	CLK and CLK#	Q	1.1	2.8	ns

Notes:

10. For data signal input slew rate ≥ 1 V/ns.
11. For data signal input slew rate ≥ V/ns and < 1V/ns.
12. CLK and CLK# signals input slew rates are ≥ 1 V/ns.
13. See test circuits and waveforms. T_A = 0°C to +85°C.

Output Buffer Characteristics

Table 3. Output Buffer Voltage vs. Current (V/I) Characteristics

Voltage (V)	Pull-Down		Pull-Up	
	Min. I(mA)	Max. I(mA)	Min. I(mA)	Max. I(mA)
0	0	0	-55	-162
0.1	6	13	-55	-161
0.2	10	25	-54	-160
0.3	15	38	-54	-159
0.4	19	49	-54	-157
0.5	23	60	-54	-156
0.6	27	71	-53	-154
0.7	30	81	-53	-152
0.8	34	91	-53	-149
0.9	36	100	-52	-146
1.0	38	108	-52	-143
1.1	40	115	-52	-140
1.2	42	123	-51	-137
1.3	43	130	-50	-134
1.4	44	137	-48	-130
1.5	44	144	-46	-125
1.6	45	150	-44	-120
1.7	45	158	-40	-112
1.8	45	165	-38	-104
1.9	45	172	-35	-96
2.0	45	179	-31	-83
2.1	46	185	-28	-72
2.2	46	191	-23	-60
2.3	46	196	-19	-49
2.4	46	201	-15	-38
2.5	46	206	-10	-27
2.6	46	211	-5	-15
2.7	46	216	0	0

Table 4. Output Buffer Slew-Rate Characteristics

dV/dt	Min.	Max.
Rise	0.85 V/ns	15.9 V/ns
Fall	1.00 V/ns	18.9 V/ns

Parameter Measurement Information^[14]

$V_{DD} = 2.5V \pm 0.2V$

Timing Diagrams

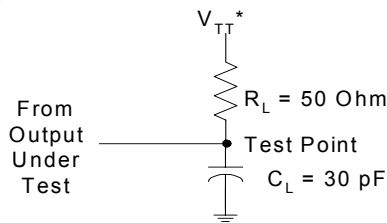


Figure 1. Load Circuit^[15]

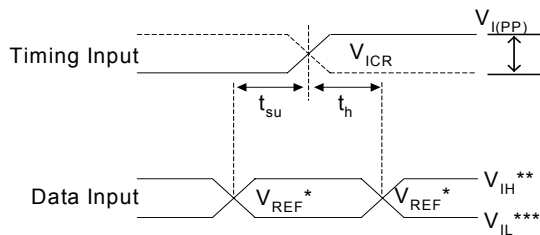


Figure 2. Voltage Waveforms Set-up and Hold Times

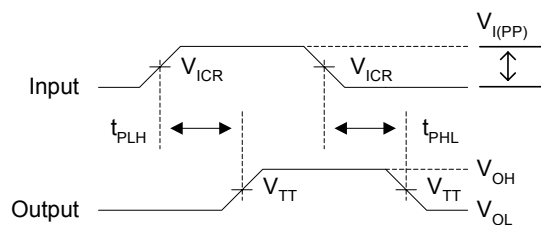


Figure 3. Voltage Waveforms Propagation Delay Times^[16, 17]

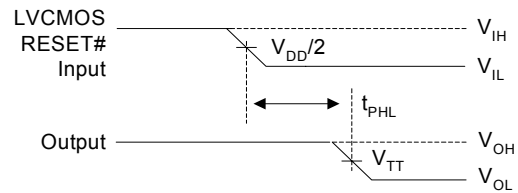


Figure 4. Voltage Waveforms Propagation Delay Times

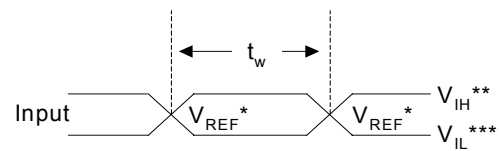


Figure 5. Voltage Waveforms Pulse Duration^[18,19]

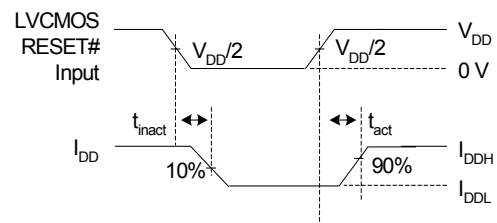


Figure 6. Voltage Waveforms Enable and Disable Times Low- and High-level Enabling

Ordering Information

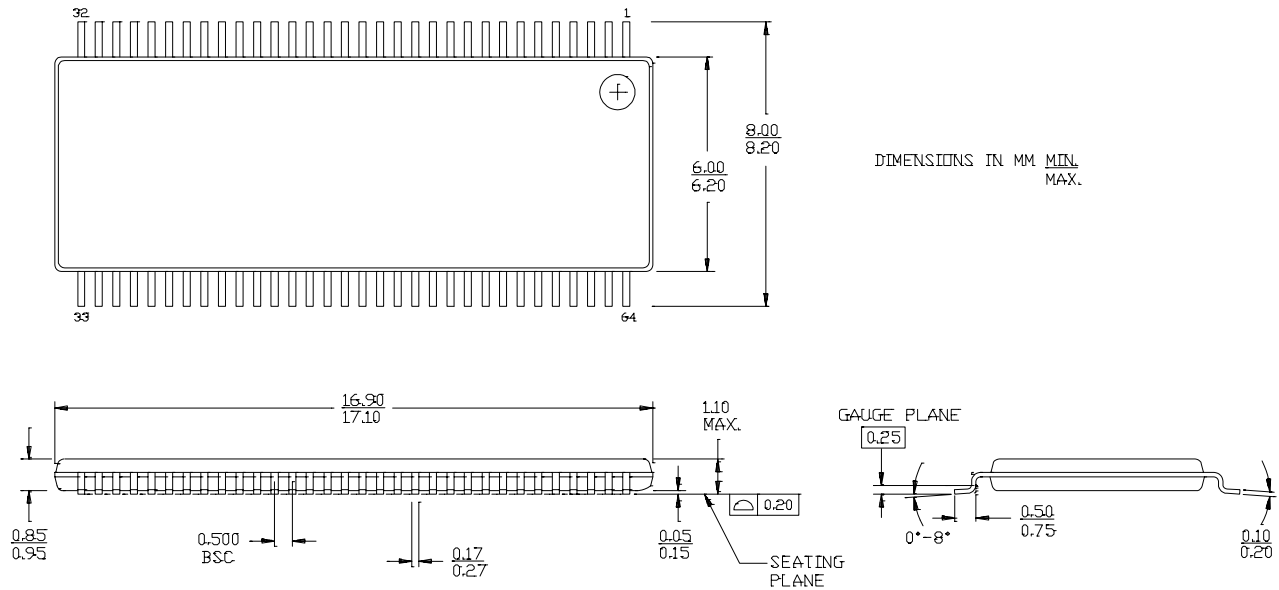
Part Number	Package Type	Product Flow
CY2SSTV16859ZC	64-pin TSSOP	Commercial, 0° to 70°C
CY2SSTV16859ZCT	64-pin TSSOP– Tape and Reel	Commercial, 0° to 70°C
CY2SSTV16859ZI	64-pin TSSOP	Industrial, –40° to 85°C
CY2SSTV16859ZIT	64-pin TSSOP – Tape and Reel	Industrial, –40° to 85°C
CY2SSTV16859LFC	56-pin QFN	Commercial, 0° to 70°C
CY2SSTV16859LFCT	56-pin QFN – Tape and Reel	Commercial, 0° to 70°C
CY2SSTV16859LFI	56-pin QFN	Industrial, –40° to 85°C
CY2SSTV16859LFIT	56-pin QFN– Tape and Reel	Industrial, –40° to 85°C

Notes:

14. All input pulses are supplied by generators having the following characteristics: PRR < 10 MHz, ZO = 50-ohm output slew rate = 1 V/ns ±20% (unless otherwise specified).
15. C_L includes probe and jig capacitance.
16. the outputs are measured one at a time with one transition per measurement.
17. *V_{TT} = V_{REF} = V_{DDQ}/2.
18. **V_{IH} = V_{REF} + 350 mV (AC voltage levels).
19. ***V_{IL} = V_{REF} - 350 mV (AC voltage levels).

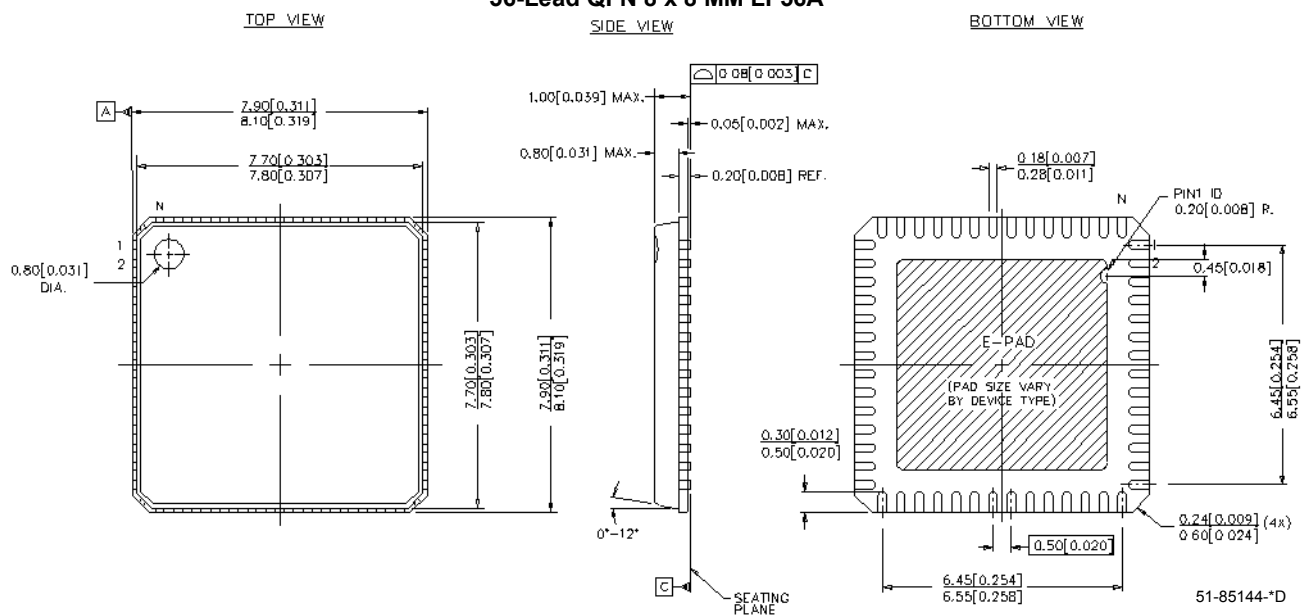
Package Drawing and Dimension

64-lead Thin Shrunk Small Outline Package (6 mm x 17 mm) Z64



51-85153-**

56-Lead QFN 8 x 8 MM LF56A



51-85144-*D

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Document History Page

Document Title: CY2SSTV16859 13-Bit to 26-Bit Registered Buffer PC2700-/PC3200-Compliant Document Number: 38-07463				
REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	123052	04/14/03	RGL	New Data Sheet
*A	126277	04/21/02	KKV	Added commercial information to ordering information table, was not added in previous rev ** Added to title "PC2700-/PC3200- Compliant"
*B	128326	07/30/03	RGL	Added 56 QFN packages (Industrial and Commercial) in the device