AN6500, AN6500S, AN6501

Built-in Reference Voltage Operational Amplifiers

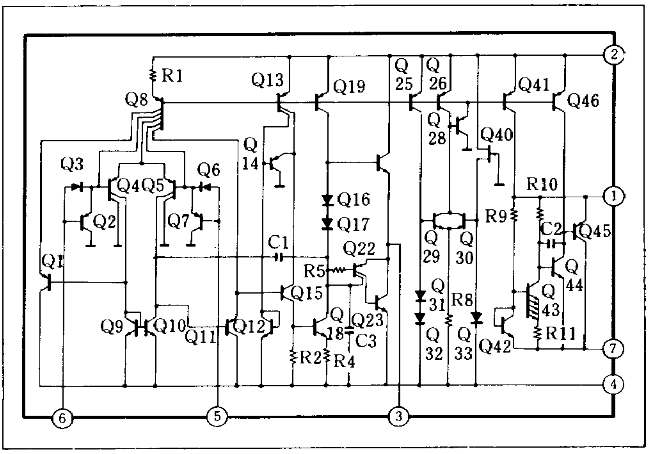
■ Outline

The AN6500, the AN6500S, and the AN6501 are high-performance operational amplifiers with reference voltage built-in, allowing single power supply voltage operation and wide application with reference voltage.

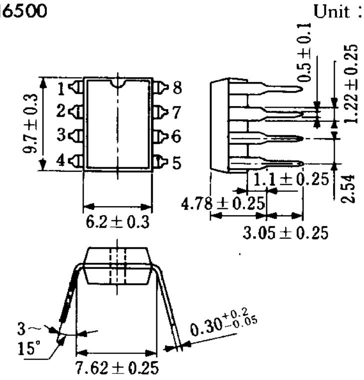
■ Features

- Wide range of operating voltage : 3~24V
- Single power supply voltage operation
- Large output current : $I_O = {}^{+120mA\ typ.}_{-110mA\ typ.}$
- Low reference voltage : V_{REF}=1.33V typ.
- Easy to compose variable regulator with reference voltage
- 3 types of packages are available
- Little cross-over distortion in operational amplifier circuit

■ Schematic Diagram

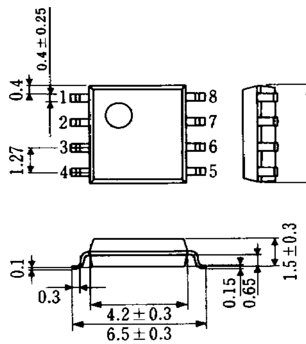


AN6500 Unit : mm



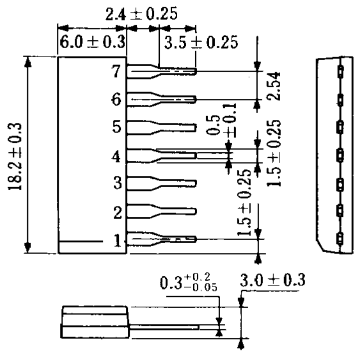
8-Lead DIL Plastic Package

AN6500S Unit : mm



8-Lead PANAFLAT Package(SO-8D)

AN6501 Unit : mm



7-Lead SIL Plastic Package

■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	Ref. Voltage(+)	5	OP. Amp. Input(+)
2	Supply Voltage	6	OP. Amp. Input(−)
3	OP. Amp. Output	7	Ref. Voltage(−)
4	GND	8	NC

■ Absolute Maximum Ratings (Ta=25℃)

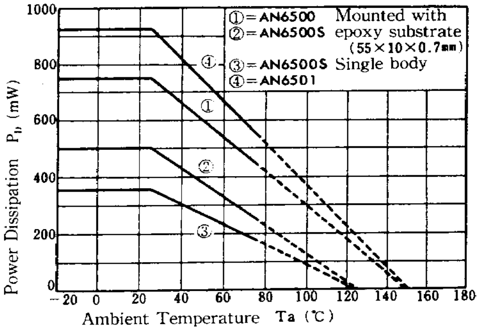
Item		Symbol	Rating	Unit
Supply Voltage		V_{CC}	24	V
Supply Current		I_{CC}	160	mA
Reference Voltage Outflow Current		$(V_{REF})-I^{*1}$	−100	μA
Reference Voltage Inflow Current		$(V_{REF})+I^{*2}$	500	μA
Common-Mode Input Voltage Range		V_{ICM}	−0.3～+24	V
Differential Input Voltage		V_{ID}	24	V
Output Sink Current		I_{SIXK}	150	mA
Power Dissipation	AN6500	$P_D{}^{*3}$	750	mW
	AN6500S		360	mW
	AN6501		925	mW
Operating Ambient Temperature		T_{opr}	−20～+75	℃
Storage Temperature	AN6500, AN6501	T_{stg}	−55～+150	℃
	AN6500S		−40～+125	℃

*1 Current flowed out from Pin①. *2 Current flowed into Pin①. *3 When enlarging output current. watch power consumption.

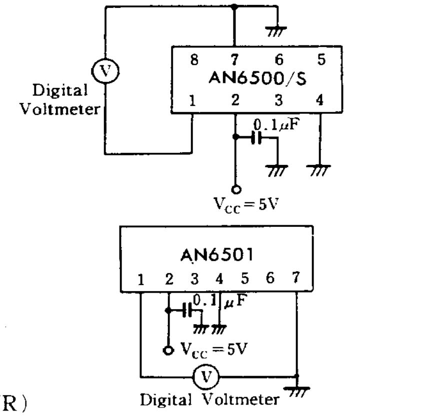
■ Electrical Characteristics (V_{CC}=15V, V_{EE}=−15V, Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Reference Voltage	V_{REF}	1		1.25	1.33	1.45	V
Reference Voltage Temperature Variation Characteristics	$\Delta V_{REF}/Ta$	1	Ta=0～50℃		−30		ppm/℃
Input Offset Voltage	$V_{I(offset)}$	2	$R_S=50\Omega$		2	7	mV
Input Bias Current	I_{Bias}	2			100	500	nA
Input Offset Current	I_{IO}	2			5	300	nA
Common-Mode Input Voltage Range	V_{CM}	3				3.5	V
Supply Current	I_{CC}	4	$R_L=\infty$		2.5	3.5	mA
Voltage Gain	G_V	2	$R_L\geqq 2k\Omega$	80	108		dB
Maximum Output Voltage(1)	$V_{O(max.)1}$	5	$R_L\leqq 2k\Omega$	3.5			V
Maximum Output Voltage(2)	$V_{O(max.)2}$	5	$V_{CC}=5V$, $I_O=70mA$	3	4.1		V
Common-Mode Rejection Ratio	CMR	2			85		dB
Supply Voltage Rejection Ratio	SVR	2			90		dB
Output Source Current	$I_{O(source)}$	6	$V_{IN}{}^+=1V$, $V_{IN}{}^-=0V$	70	110		mA
Output Sink Current	I_{SINK}	7	$V_{IN}{}^+=0V$, $V_{IN}{}^-=1V$	70	120		mA
Zero-Cross Frequency	$f_{(T)}$	8			1		MHz

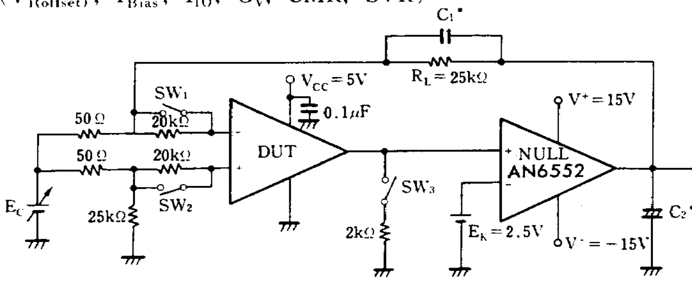
P_D—Ta



Test Circuit 1 (V_{REF}, ΔV_{REF}/Ta)



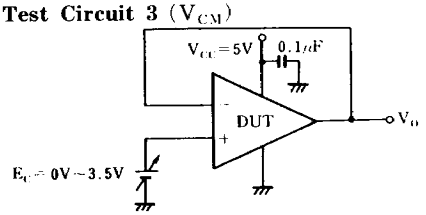
Test Circuit 2 ($V_{I(offset)}$, I_{Bias}, I_{IO}, G_V, CMR, SVR)



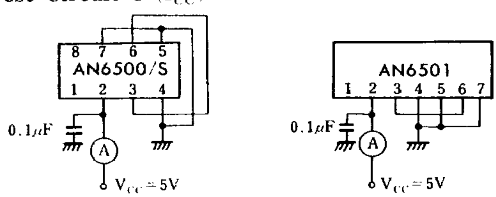
* C_1 and C_2 are for the prevention of oscillation.

Item	Measurement Conditions
Input Offset Voltage	V_{F1} is measured with both the SW_1 and SW_2 set to ON and $E_C=0$. Can be given by $V_{IO}=\frac{V_{F1}}{500}$(V)
Input Offset Current	V_{F2} is measured with both the SW_1 and SW_2 set to OFF and $E_C=0$. Can be given by $I_{IO}=\mid V_{F2}-V_{F1}\mid/10^7$(A)
Input Bias Current	V_{F3} is measured with the SW_1 set to ON and the SW_2 set to OFF. VF_4 is measured with the SW_1 set to OFF and the SW_2 set to ON. $E_C=0$. Can be given by $I_B=\mid V_{F4}-V_{F3}\mid/2\times10^7$(A)
Voltage Gain	V_{F5} is measured with the SW_1 and SW_2 set to ON and $E_K=1.4$V. V_{F5} is measured with $E_K=3.4$V. The SW_3 is set to ON. Can be given by $G_V=20\log\left(\frac{1000}{V_{F5}'-V_{F5}}\right)$
Common-Mode Rejection Ratio	The SW_1 and SW_2 are set to ON. V_{F6} is measured with E_C set to E_{C1}. V_{F7} is measured with E_C set to E_{C2}. Can be given by $CMR=20\log\left(500\times\left\lvert\frac{E_{C1}-E_{C2}}{V_{F6}-V_{F7}}\right\rvert\right)$
Supply Voltage Rejection Ratio	The SW_1 and SW_2 are set to ON with $E_C=0$. V_{F8} is measured with V_{CC} set to V_{C1}. V_{F9} is measured with V_{CC} set to V_{C2}. Can be given by $SVR=20\log\left(500\times\left\lvert\frac{V_{C1}-V_{C2}}{V_{F8}-V_{F9}}\right\rvert\right)$

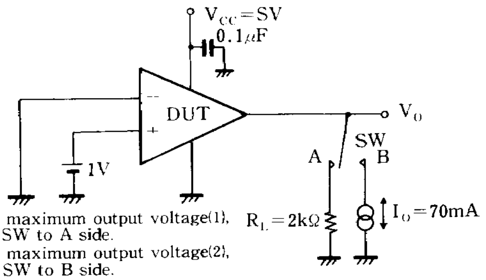
Test Circuit 3 (V_{CM})



Test Circuit 4 (I_{CC})

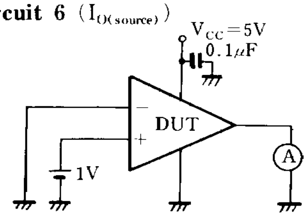


Test Circuit 5 ($V_{O(max)1}$, $V_{O(max)2}$)

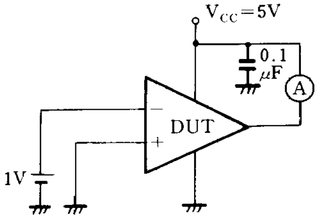


● For maximum output voltage(1), set SW to A side.
● For maximum output voltage(2), set SW to B side.

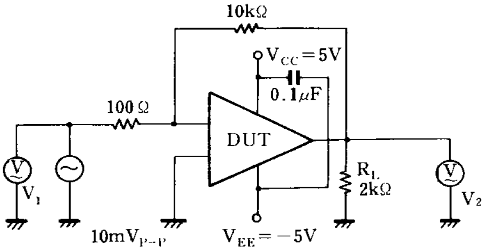
Test Circuit 6 ($I_{O(source)}$)



Test Circuit 7 (I_{SINK})

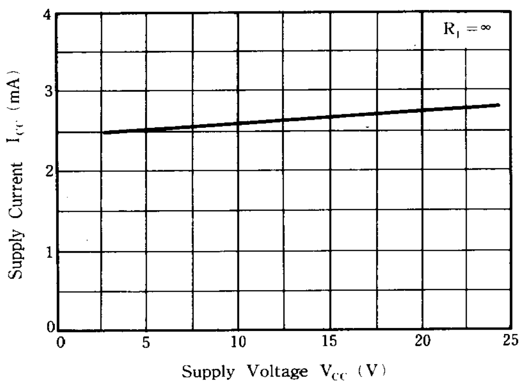


Test Circuit 8 ($f_{(T)}$)

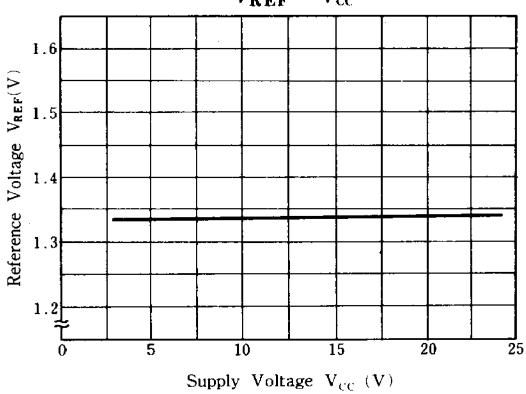


● Frequency of the oscillator when $V_1=V_2$.

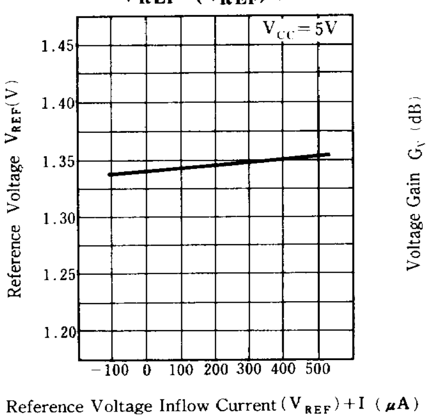
I_{CC}—V_{CC}



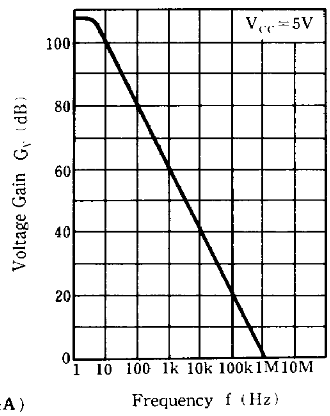
V_{REF}—V_{CC}



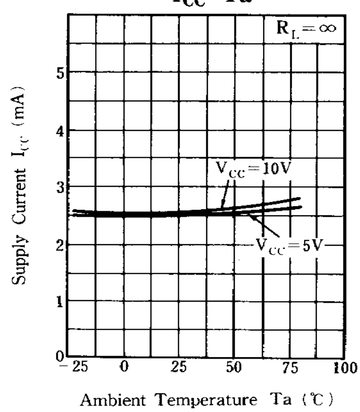
V_{REF}—(V_{REF})+I



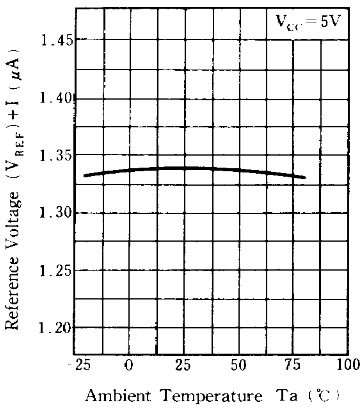
G_V—f



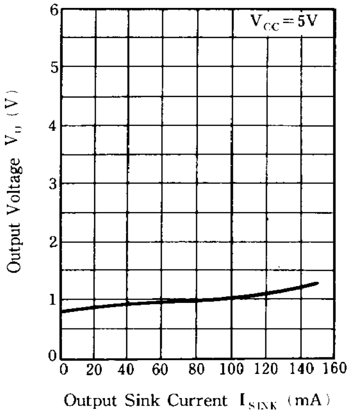
I_{CC}—Ta



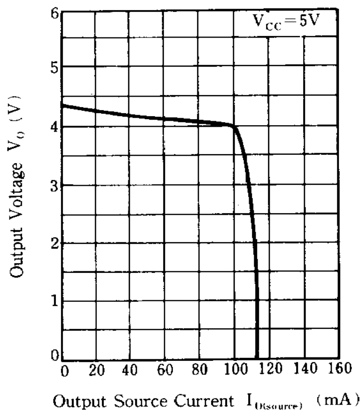
V_{REF}–Ta



V_O—I_{SINK}

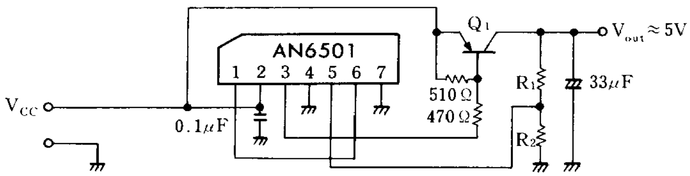


V_O—$I_{O(source)}$



■ Application Circuits

1. Voltage Regulator Circuit
High efficiency circuit with small I/O voltage difference



● Output voltage (V_{out}) is calculated by the following expression.

$$V_{out}=\frac{R_1+R_2}{R_2}V_{REF}\,(V)$$

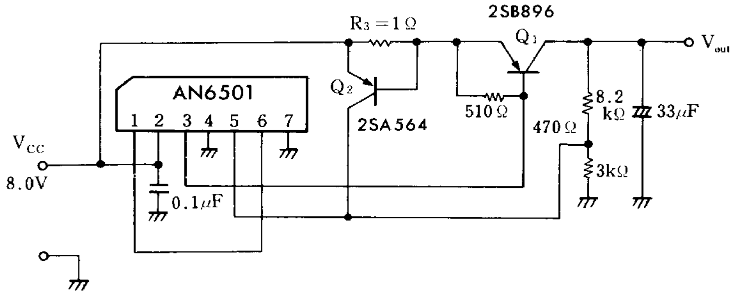
$$\fallingdotseq\frac{R_1+R_2}{R_2}\times 1.33\,(V)$$

● I/D Voltage difference

2SB896 is applied when output current is 330mA. The minimum I/O voltage difference is 0.2V.

Item	Symbol	Condition		typ.	Unit
Line Regulation	REG_{IN}	$V_{CC}=6\sim20V$, $I_O=1A$	$R_1=8.2k\Omega$ $R_2=3k\Omega$	16	mV
Load Regulation	REG_L	$V_{CC}=10V$, $I_O=5mA\sim1A$		9	mV
Ripple Rejection Ratio	RR	$V_{CC}=8\sim18V$, $I_O=100A$, f=120Hz		57.4	dB

2. Voltage Regulator Circuit
With output current limiter



● Limit Current $I_{O(Lim)}$ is calculated by the following expression.

$$I_{O(Lim)}=\frac{V_{BE}(Q_2)}{R_3}$$

When $V_{BE}(Q_2)=0.7V$, and $R_3=1\Omega$,

$$I_{O(Lim)}=\frac{0.7}{1}=0.7A$$

Panasonic