# DUAL P-CHANNEL MATCHED MOSFET PAIR



## GENERAL DESCRIPTION

The ALD1102 is a monolithic dual P-channel matched transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process.

The ALD1102 offers high input impedance and negative current temperature coefficient. The transistor pair is matched for minimum offset voltage and differential thermal response, and it is designed for switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC operating environment. When used with an ALD1101, a dual CMOS analog switch can be constructed. In addition, the ALD1102 is intended as a building block for differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1102 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 50pA at room temperature. For example, DC beta of the device at a drain current of 5mA at 25°C is = 5mA/50pA = 100,000,000.

## FEATURES

- Low threshold voltage of 0.7V
- Low input capacitance
- Low Vos grades -- 2mV, 5mV, 10mV
- High input impedance -- $10^{12}\Omega$ typical
- Low input and output leakage currents
- Negative current ($I_{DS}$) temperature coefficient
- Enhancement-mode (normally off)
- DC current gain $10^9$

## ORDERING INFORMATION

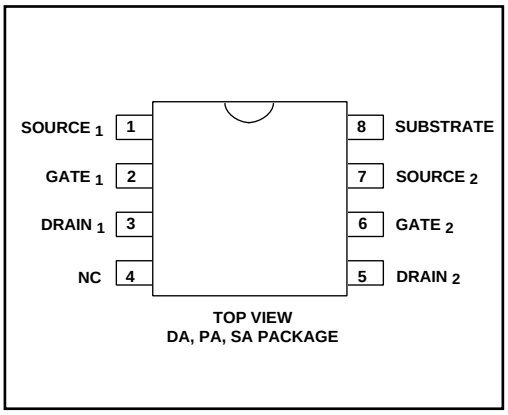
| Operating Temperature Range* | | |
|---|---|---|
| -55°C to +125°C | 0°C to +70°C | 0°C to +70°C |
| 8-Pin CERDIP Package | 8-Pin Plastic Dip Package | 8-Pin SOIC Package |
| ALD1102 DA | ALD1102A PA<br>ALD1102B PA<br>ALD1102 PA | ALD1102 SA |

* Contact factory for industrial temperature range.

## APPLICATIONS

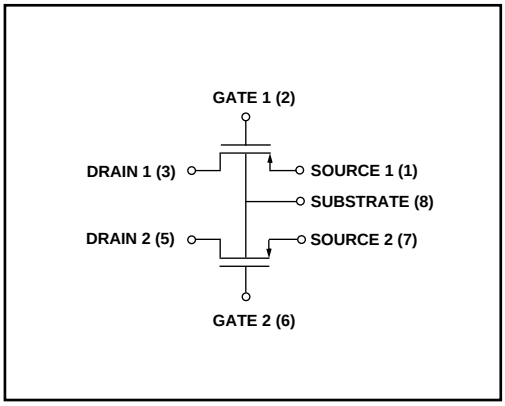
- Precision current mirrors
- Precision current sources
- Analog switches
- Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog inverter

## PIN CONFIGURATION




TOP VIEW
DA, PA, SA PACKAGE

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

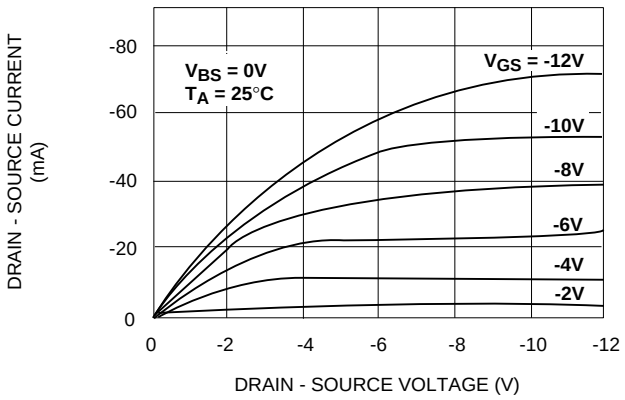
Drain-source voltage, $V_{DS}$ — -13.2V
Gate-source voltage, $V_{GS}$ — -13.2V
Power dissipation — 500 mW
Operating temperature range PA, SA package — 0°C to +70°C
DA package — -55°C to +125°C
Storage temperature range — -65°C to +150°C
Lead temperature, 10 seconds — +260°C

## OPERATING ELECTRICAL CHARACTERISTICS
**$T_A$ = 25°C unless otherwise specified**

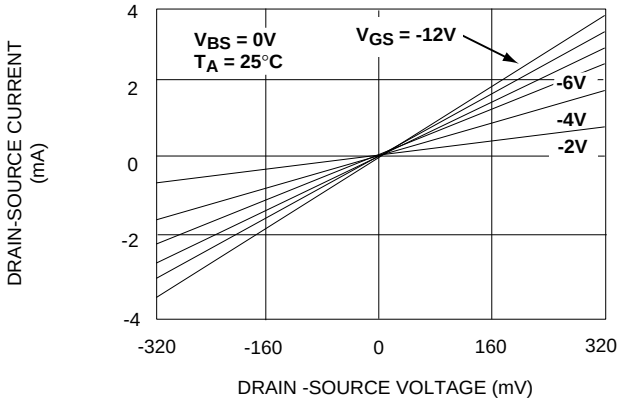
| Parameter | Symbol | 1102A | | | 1102B | | | 1102 | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| Gate Threshold Voltage | $V_T$ | -0.4 | -0.7 | -1.2 | -0.4 | -0.7 | -1.2 | -0.4 | -0.7 | -1.2 | V | $I_{DS}$ = -10µA $V_{GS} = V_{DS}$ |
| Offset Voltage $V_{GS1}$ - $V_{GS2}$ | $V_{OS}$ | | | 2 | | | 5 | | | 10 | mV | $I_{DS}$ = -100µA $V_{GS} = V_{DS}$ |
| Gate Threshold Temperature Drift | $TC_{VT}$ | | -1.3 | | | -1.3 | | | -1.3 | | mV/°C | |
| On Drain Current | $I_{DS\ (ON)}$ | -8 | -16 | | -8 | -16 | | -8 | -16 | | mA | $V_{GS} = V_{DS}$ = -5V |
| Transconductance | $G_{fs}$ | 2 | 4 | | 2 | 4 | | 2 | 4 | | mmho | $V_{DS}$ = -5V $I_{DS}$= -10mA |
| Mismatch | $\Delta G_{fs}$ | | 0.5 | | | 0.5 | | | 0.5 | | % | |
| Output Conductance | $G_{OS}$ | | 500 | | | 500 | | | 500 | | µmho | $V_{DS}$ = -5V $I_{DS}$ = -10mA |
| Drain Source ON Resistance | $R_{DS(ON)}$ | | 180 | 270 | | 180 | 270 | | 180 | 270 | Ω | $V_{DS}$ = -0.1V $V_{GS}$ = -5V |
| Drain Source ON Resistance Mismatch | $\Delta R_{DS(ON)}$ | | 0.5 | | | 0.5 | | | 0.5 | | % | $V_{DS}$ = -0.1V $V_{GS}$ = -5V |
| Drain Source Breakdown Voltage | $BV_{DSS}$ | -12 | | | -12 | | | -12 | | | V | $I_{DS}$ = -10µA $V_{GS}$ =0V |
| Off Drain Current | $I_{DS(OFF)}$ | | 0.1 | 4<br>4 | | 0.1 | 4<br>4 | | 0.1 | 4<br>4 | nA<br>µA | $V_{DS}$ =-12V $V_{GS}$ = 0V<br>$T_A$ = 125°C |
| Gate Leakage Current | $I_{GSS}$ | | 1 | 50<br>10 | | 1 | 50<br>10 | | 1 | 50<br>10 | pA<br>nA | $V_{DS}$ =0V $V_{GS}$ =-12V<br>$T_A$ = 125°C |
| Input Capacitance | $C_{ISS}$ | | 6 | 10 | | 6 | 10 | | 6 | 10 | pF | |

## TYPICAL PERFORMANCE CHARACTERISITCS

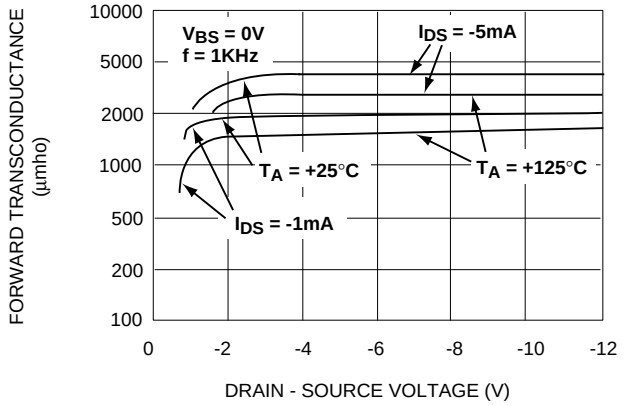
### OUTPUT CHARACTERISTICS



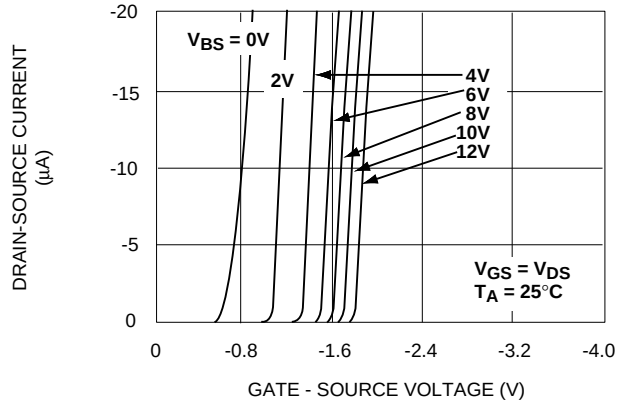

### LOW VOLTAGE OUTPUT CHARACTERISTICS



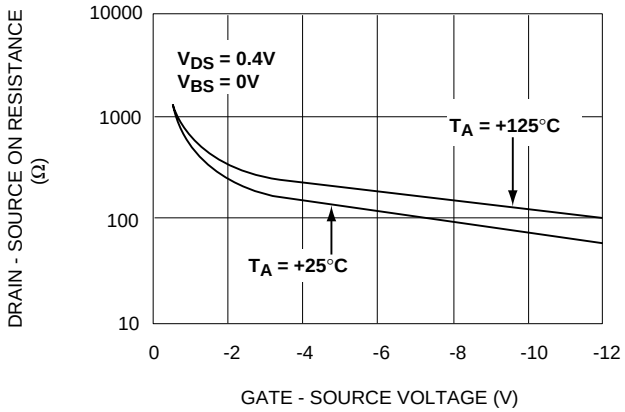

### FORWARD TRANSCONDUCTANCE vs. DRAIN - SOURCE VOLTAGE




### TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS




### $R_{DS\ (ON)}$ vs. GATE - SOURCE VOLTAGE




### OFF DRAIN - CURRENT vs. TEMPERATURE