

High-Speed CMOS Logic CMOS Programmable Divide-by-N Counter

Features

- Synchronous Programmable $\div N$ Counter $N = 3$ to 9999 or 15999
- Presetable Down-Counter
- Fully Static Operation
- Mode-Select Control of Initial Decade Counting Function ($\div 10, 8, 5, 4, 2$)
- Master Preset Initialization
- Latchable $\div N$ Output
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$

Applications

- Communications Digital Frequency Synthesizers; VHF, UHF, FM, AM, etc.
- Fixed or Programmable Frequency Division
- "Time Out" Timer for Consumer-Application Industrial Controls
- AN6374 "Application of the CMOS CD4059A Programmable Divide-by-N Counter in FM and Citizens Band Transceiver Digital Tuners"

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC4059E	-55 to 125	24 Ld PDIP	E24.3

NOTE:

1. Wafer and die is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Description

The Harris CD74HC4059 are high-speed silicon-gate devices that are pin-compatible with the CD4059A devices of the CD4000B series. These devices are divide-by-N down-counters that can be programmed to divide an input frequency by any number "N" from 3 to 15,999. The output signal is a pulse one clock cycle wide occurring at a rate equal to the input frequency divide by N. The down-counter is preset by means of 16 jam inputs.

The three Mode-Select Inputs K_a , K_b and K_c determine the modulus ("divide-by" number) of the first and last counting sections in accordance with the truth table shown on Table 1. Every time the first (fastest) counting section goes through one cycle, it reduces by 1 the number that has been preset (jammed) into the three decades of the intermediate counting section and the last counting section, which consists of flip-flops that are not needed for opening the first counting section. For example, in the $\div 2$ mode, only one flip-flop is needed in the first counting section. Therefore the last counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. If $\div 10$ is desired for the first section, K_a is set "high", K_b "high" and K_c "low". Jam inputs J1, J2, J3, and J4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD decade ($\div 10$) counters presettable by means of Jam Inputs J5 through J16.

The Mode-Select Inputs permit frequency-synthesizer channel separations of 10, 12.5, 20, 25 or 50 parts. These inputs set the maximum value of N at 9999 (when the first counting section divides by 5 or 10) or 15,999 (when the first counting section divides by 8, 4, or 2).

The three decades of the intermediate counter can be preset to a binary 15 instead of a binary 9, while their place values are still 1, 10, and 100, multiplied by the number of the $\div N$ mode. For example, in the $\div 8$ mode, the number from which counting down begins can be preset to:

3rd Decade	1500
2nd Decade	150
1st Decade	15
Last Counting Section	1000

The total of these numbers (2665) times 8 equals 12,320. The first counting section can be preset to 7. Therefore, 21,327 is the maximum possible count in the $\div 8$ mode.

The highest count of the various is shown in the column entitled Extended Counter Range of Table 1. Control inputs K_b and K_c can be used to initiate and lock the counter in the "master preset" state. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that state as long as K_b and K_c both remain low. The counter begins to count down from the preset state when a counting mode other than the master preset mode is selected.

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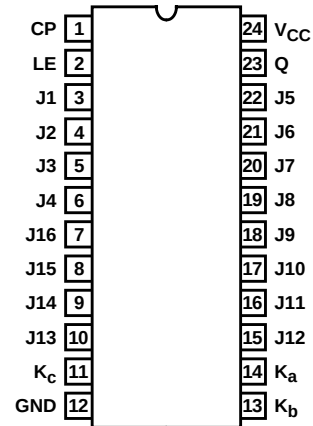
The counter should always be put in the master preset mode before the ÷5 mode is selected. Whenever the master preset mode is used, control signals K_b = "low" and K_c = "low" must be applied for at least 3 full clock pulses.

After Preset Mode inputs have been changed to one of the ÷ modes, the next positive-going clock transition changes an internal flip-flop so that the countdown can begin at the second positive-going clock transition. Thus, after an MP (Master Preset) mode, there is always one extra count before the output goes high. Figure 1 illustrates a total count of 3 (÷8 mode). If the Master Preset mode is started two clock cycles or less before an output pulse, the output pulse will appear at the time due. If the Master Preset Mode is not used, the counter jumps back to the "Jam" count when the output pulse appears.

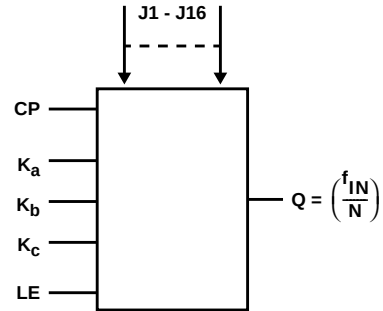
A "high" on the Latch Enable input will cause the counter output to remain high once an output pulse occurs, and to remain in the high state until the latch input returns to "low". If the Latch Enable is "low", the output pulse will remain high for only one cycle of the clock-input signal.

Pinout

CD74HC4059
(PDIP)
TOP VIEW



Functional Diagram



TRUTH TABLE

MODE SELECT INPUT			FIRST COUNTING SECTION			LAST COUNTING SECTION			COUNTER RANGE	
									DESIGN	EXTENDED
K_a	K_b	K_c	MODE DIVIDES-BY	CAN BE PRESET TO A MAX OF:	(NOTE 3) JAM INPUTS USED:	MODE DIVIDES-BY	CAN BE PRESET TO A MAX OF:	(NOTE 3) JAM INPUTS USED:	MAX	MAX
H	H	H	2	1	J1	8	7	J2, J3, J4	15,999	17,331
L	H	H	4	3	J1, J2	4	3	J3, J4	15,999	18,663
H	L	H	5 (Note 4)	4	J1, J2, J3	2	1	J4	9,999	13,329
L	L	H	8	7	J1, J2, J3	2	1	J4	15,999	21,327
H	H	L	10	9	J1, J2, J3, J4	1	0	-	9,999	16,659
X	L	L	Master Preset			Master Preset			-	-

NOTES:

- X = Don't Care
- J1 = Least Significant Bit. J4 = Most Significant Bit.
- Operation in the ÷5 mode (1st counting section) requires going through the Master Preset mode prior to going into the ÷5 mode. At power turn-on, K_c must be "low" for a period of 3 input clock pulses after V_{CC} reaches a minimum of 3V.

CD74HC4059

How to Preset the CD74HC/HCT4059 to Desired ÷N

The value N is determined as follows:

(EQ. 1)

$$N = (\text{MODE}^\dagger) (1000 \times \text{Decade 5 Preset} + 100 \times \text{Decade 4 Preset} + 10 \times \text{Decade 3 Preset} + 1 \times \text{Decade 2 Preset}) + \text{Decade 1 Preset}$$

† MODE = First counting section divider (10, 8, 5, 4 or 2)

$$\text{Preset Value} = \frac{N}{\text{Mode}}$$

(EQ. 2)

Example:

$$N = 8479, \text{ Mode} = 5$$

Mode Select = 5

K_a K_b K_c
H L H

To calculate preset values for any N count, divide the N count by the Mode. The resultant is the corresponding preset values of the 5th through 2nd decade with the remainder being equal to the 1st decade value.

$$1695 + 4 \text{ (Preset Values)}$$

$$5 \overline{) 8479}$$

Mode N

Program Jam Inputs (BCD)

4				1	5				9				6			
J1	J2	J3	J4		J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
L	L	H	H		H	L	H	L	H	L	L	H	L	H	H	L

NOTE:

To verify the results, use Equation 1:

$$N = 5 (1000 \times 1 + 100 \times 6 + 10 \times 9 + 1 \times 5) + 4$$

$$N = 8479$$

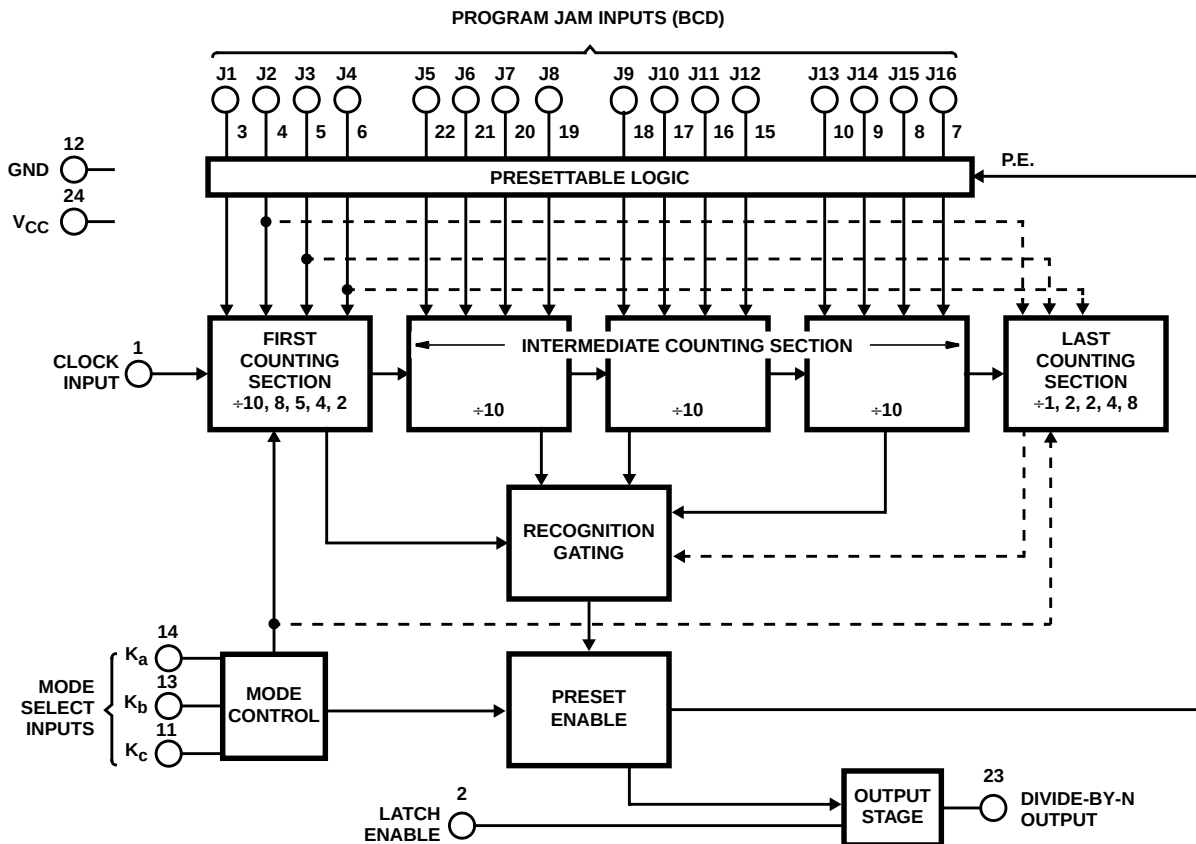


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

CD74HC4059

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} -0.5V to 7V
 DC Input Diode Current, I_{IK}
 For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ $\pm 20mA$
 DC Output Diode Current, I_{OK}
 For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ $\pm 20mA$
 DC Output Source or Sink Current per Output Pin, I_O
 For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ $\pm 25mA$
 DC V_{CC} or Ground Current, I_{CC} $\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 5) θ_{JA} ($^{\circ}C/W$)
 PDIP Package 60
 Maximum Junction Temperature (Hermetic Package or Die) ... $175^{\circ}C$
 Maximum Junction Temperature (Plastic Package) $150^{\circ}C$
 Maximum Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 Maximum Lead Temperature (Soldering 10s) $300^{\circ}C$

Operating Conditions

Temperature Range, T_A $-55^{\circ}C$ to $125^{\circ}C$
 Supply Voltage Range, V_{CC} 2V to 6V
 DC Input or Output Voltage, V_I , V_O 0V to V_{CC}
 Input Rise and Fall Time
 2V 100ns (Max)
 4.5V 500ns (Max)
 6V 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
High Level Input Voltage	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
-			-	-	-	-	-	-	-	-	V	
-4			4.5	3.98	-	-	3.84	-	3.7	-	V	
-5.2			6	5.48	-	-	5.34	-	5.2	-	V	
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
-			-	-	-	-	-	-	-	-	V	
4			4.5	-	-	0.26	-	0.33	-	0.4	V	
5.2			6	-	-	0.26	-	0.33	-	0.4	V	
Input Leakage Current	I _I	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μA

CD74HC4059

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Pulse Width CP	t _W	2	90	-	-	115	-	-	135	-	-	ns
		4.5	18	-	-	23	-	-	27	-	-	ns
		6	15	-	-	20	-	-	23	-	-	ns
Setup Time K _b , K _c to CP	t _{SU}	2	75	-	-	95	-	-	110	-	-	ns
		4.5	15	-	-	19	-	-	22	-	-	ns
		6	13	-	-	16	-	-	19	-	-	ns
CP Frequency	f _{MAX}	2	5	-	-	4	-	-	4	-	-	MHz
		4.5	27	-	-	22	-	-	18	-	-	MHz
		6	32	-	-	26	-	-	21	-	-	MHz

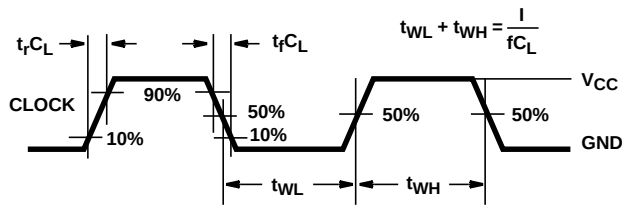
Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Propagation Delay, CP to Q	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	200	-	250	-	300	ns
			4.5	-	-	40	-	50	-	60	ns
			6	-	-	34	-	43	-	51	ns
		C _L = 15pF	5	-	17	-	-	-	-	-	ns
Propagation Delay, LE to Q	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	175	-	220	-	265	ns
			4.5	-	-	35	-	44	-	53	ns
			6	-	-	30	-	37	-	45	ns
		C _L = 15pF	5	-	14	-	-	-	-	-	ns
Output Transition Time	t _{THL} , t _{TLH}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
CP Frequency	f _{MAX}	C _L = 15pF	5	-	54	-	-	-	-	-	MHz
Input Capacitance	C _I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 6, 7)	C _{PD}	-	5	-	36	-	-	-	-	-	pF

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per package.
- $P_D = C_{PD} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 2. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

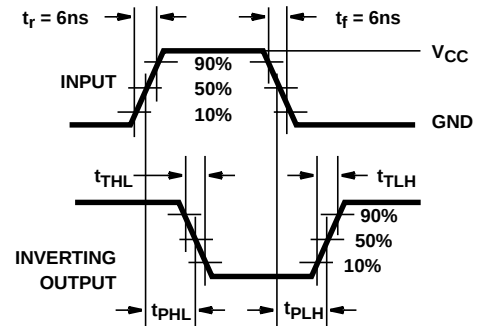


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

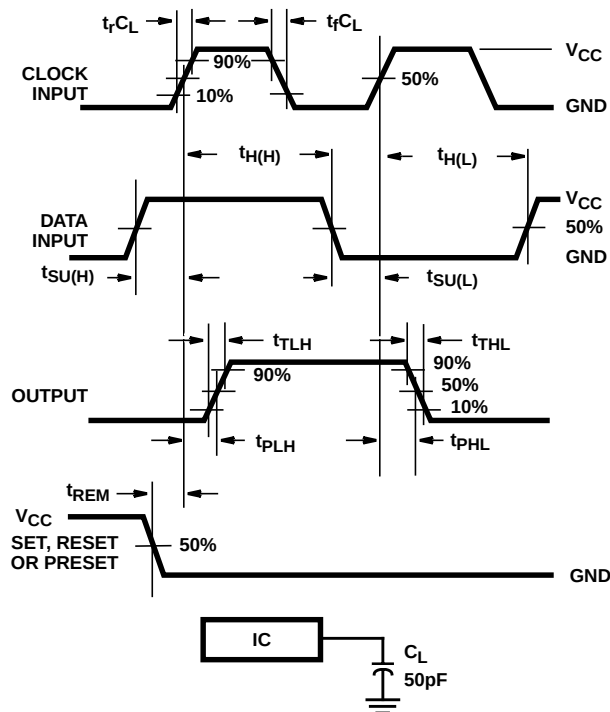


FIGURE 4. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

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