

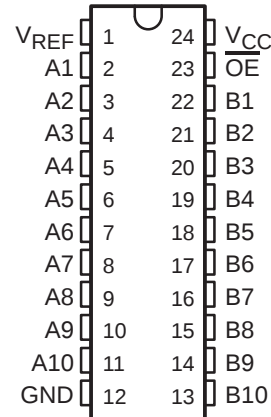
SN74CBTLV3857

LOW-VOLTAGE 10-BIT FET BUS SWITCH WITH INTERNAL PULLDOWN RESISTORS

SCDS085E – OCTOBER 1998 – REVISED OCTOBER 2003

- Enable Signal Is SSTL_2 Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Designed for Use With 200 Mbit/s Double Data-Rate (DDR) SDRAM Applications
- Switch On-State Resistance Is Designed to Eliminate Series Resistor to DDR SDRAM
- Internal 10-k Ω Pulldown Resistors to Ground on B Port
- Internal 50-k Ω Pullup Resistor on Output-Enable Input
- Rail-to-Rail Switching on Data I/O Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

This 10-bit FET bus switch is designed for 3-V to 3.6-V V_{CC} operation and SSTL_2 output-enable ($\overline{OE}$) input levels.

When $\overline{OE}$ is low, the 10-bit bus switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports. There are 10-k Ω pulldown resistors to ground on the B port.

The FET switch on-state resistance is designed to replace the series terminating resistor in the SSTL_2 data path.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – DBQ	Tape and reel	SN74CBTLV3857DBQR	CL857
	SOIC – DW	Tube	SN74CBTLV3857DW	CBTLV3857
		Tape and reel	SN74CBTLV3857DWR	
	TSSOP – PW	Tape and reel	SN74CBTLV3857PWR	CL857
	TVSOP – DGV	Tape and reel	SN74CBTLV3857DGV	CL857

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

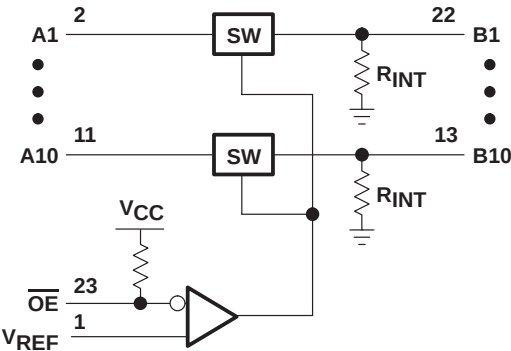
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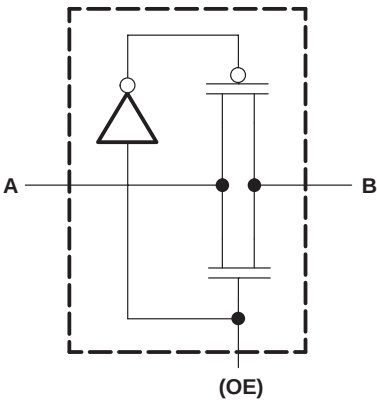
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logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range ($\overline{OE}$ only), V_I (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input voltage range (except $\overline{OE}$), V_I (see Note 1)	−0.5 V to 4.6 V
Continuous channel current	48 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DBQ package	61°C/W
DGV package	86°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{REF}	Reference voltage ($0.38 \times V_{CC}$)	1.15	1.25	1.35	V
V_{IH}	AC high-level control input voltage	$V_{REF} + 350 \text{ mV}$			V
V_{IL}	AC low-level control input voltage	$V_{REF} - 350 \text{ mV}$			V
V_{IH}	DC high-level control input voltage	$V_{REF} + 180 \text{ mV}$			V
V_{IL}	DC low-level control input voltage	$V_{REF} - 180 \text{ mV}$			V
T_A	Operating free-air temperature	-40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{IK}		$V_{CC} = 3 \text{ V}$,	$I_I = -18 \text{ mA}$			-1.2	V
I_I	$\overline{OE}$	$V_{CC} = 3.6 \text{ V}$,	$V_I = V_{CC} \text{ or GND}$			± 1	mA
	A port					± 5	μA
	B port					± 1	mA
	V_{REF}					± 5	μA
I_{CC}		$V_{CC} = 3.6 \text{ V}$,	$I_O = 0$,			25	mA
C_i	Control inputs	$V_I = 3 \text{ V or } 0$			3.5		pF
$C_{io(OFF)}$		$V_O = 3 \text{ V or } 0$,	$\overline{OE} = V_{CC}$		5		pF
$r_{on}^{\ddagger}$		$V_{CC} = 3 \text{ V}$	$V_I = 0$,	$I_I = 24 \text{ mA}$	5	8	Ω
			$V_I = 0.9 \text{ V}$,	$I_I = 24 \text{ mA}$	6	11	
			$V_I = 1.25 \text{ V}$,	$I_I = 24 \text{ mA}$	7	13	
			$V_I = 1.6 \text{ V}$,	$I_I = 24 \text{ mA}$	9	40	
$r_{off}^{\ddagger}$		$V_{CC} = 0$			1		M Ω
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$,	$V_I = 1.65 \text{ V}$,	$\overline{OE} = V_{CC}$	1		

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. Resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			MIN	MAX	
$t_{pd}^{\S}$	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B	1.4	4.2	ns
t_{dis}	$\overline{OE}$	A or B	1.4	4.8	ns

^{\S} The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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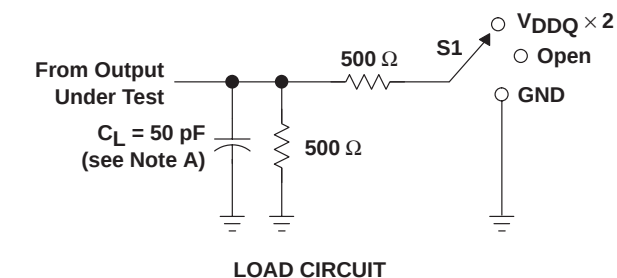
LOW-VOLTAGE 10-BIT FET BUS SWITCH

WITH INTERNAL PULLDOWN RESISTORS

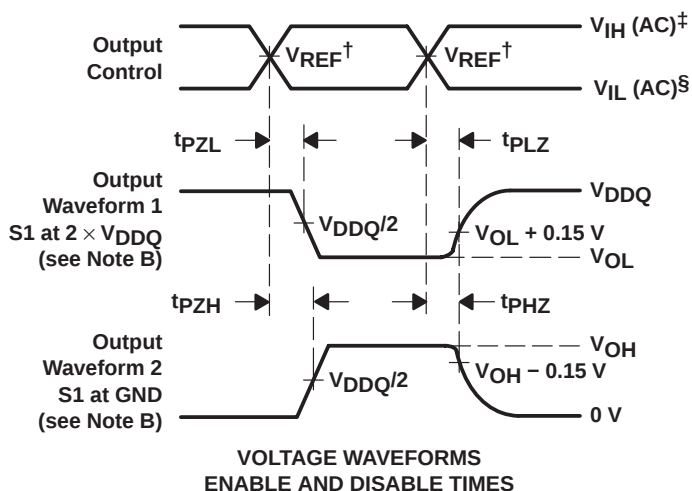
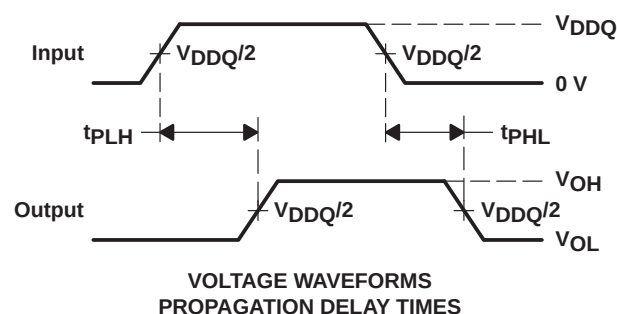
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PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ AND $V_{DDQ} = 2.5 \pm 0.2 \text{ V}$



TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open $V_{DDQ} \times 2$ GND



$\dagger V_{REF} = 0.38 \times V_{CC}$

$\ddagger V_{IH}(AC) = V_{REF} + 350 \text{ mV}$

$\S V_{IL}(AC) = V_{REF} - 350 \text{ mV}$

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.

D. The outputs are measured one at a time with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74CBTLV3857DWRE4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		Samples
74CBTLV3857DWRG4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		Samples
74CBTLV3857PWRE4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		Samples
74CBTLV3857PWRG4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		Samples
SN74CBTLV3857DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3857	Samples
SN74CBTLV3857PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL857	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTLV3857DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CBTLV3857PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

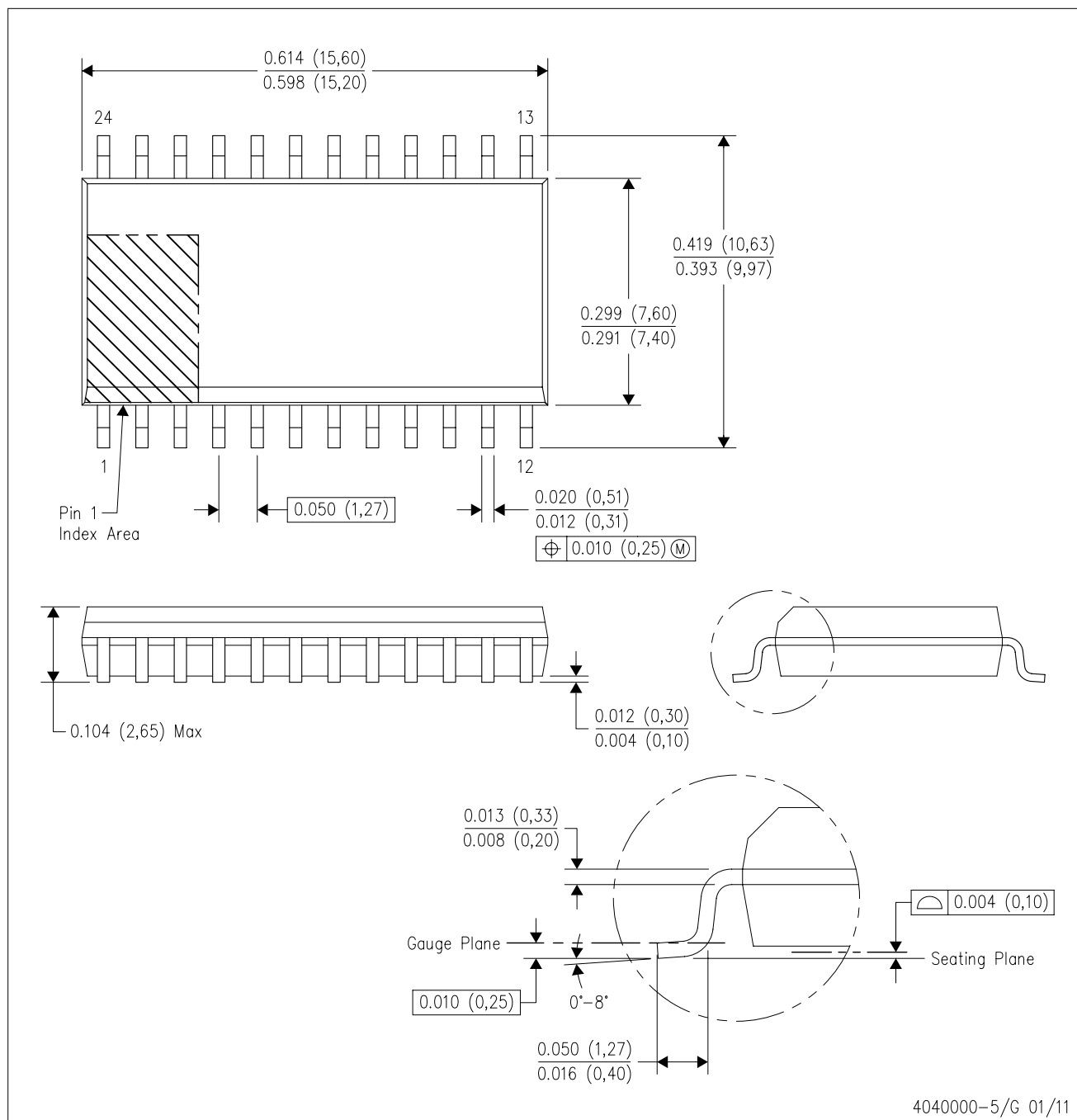


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTLV3857DWR	SOIC	DW	24	2000	367.0	367.0	45.0
SN74CBTLV3857PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

DW (R-PDSO-G24)

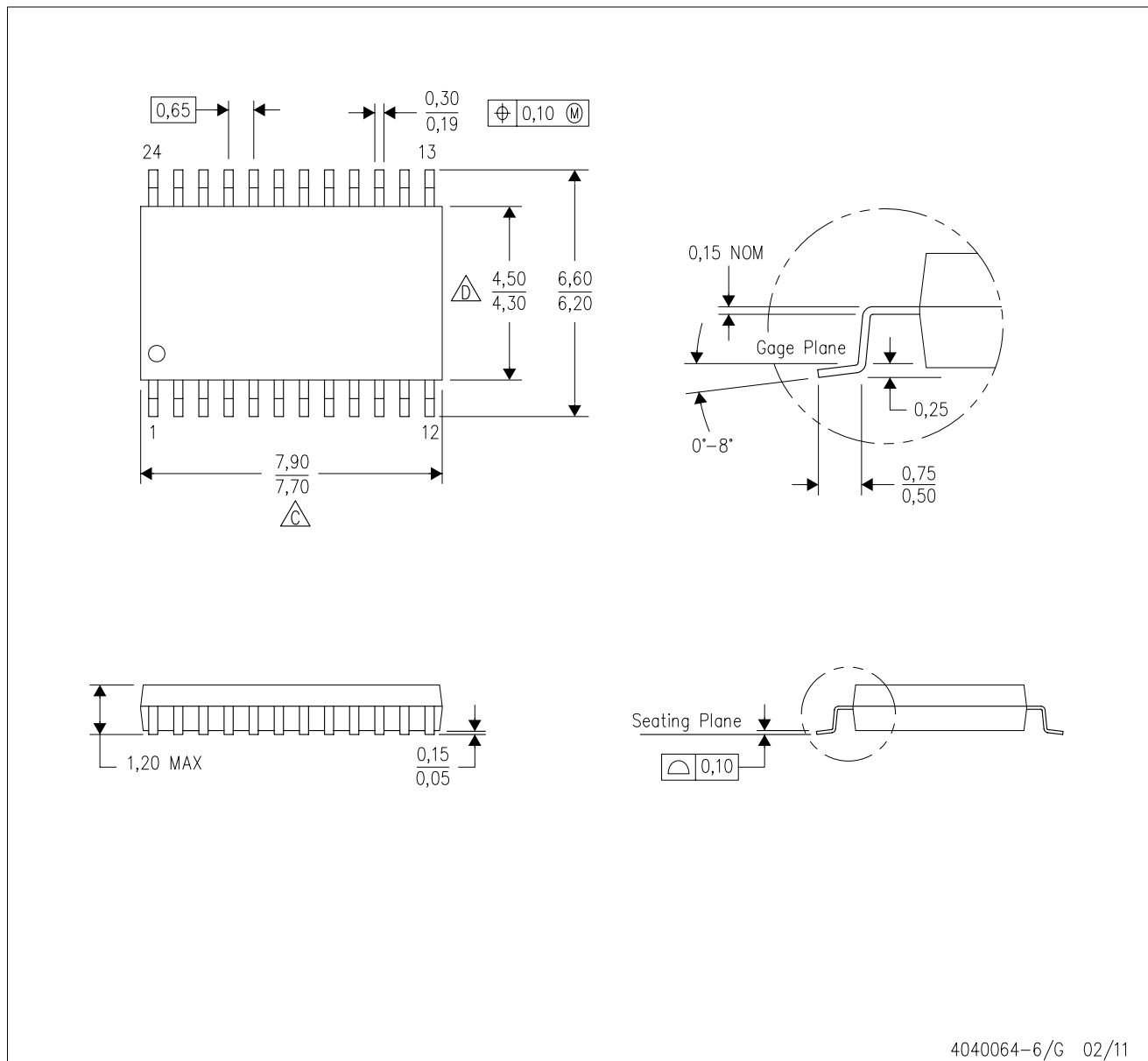
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

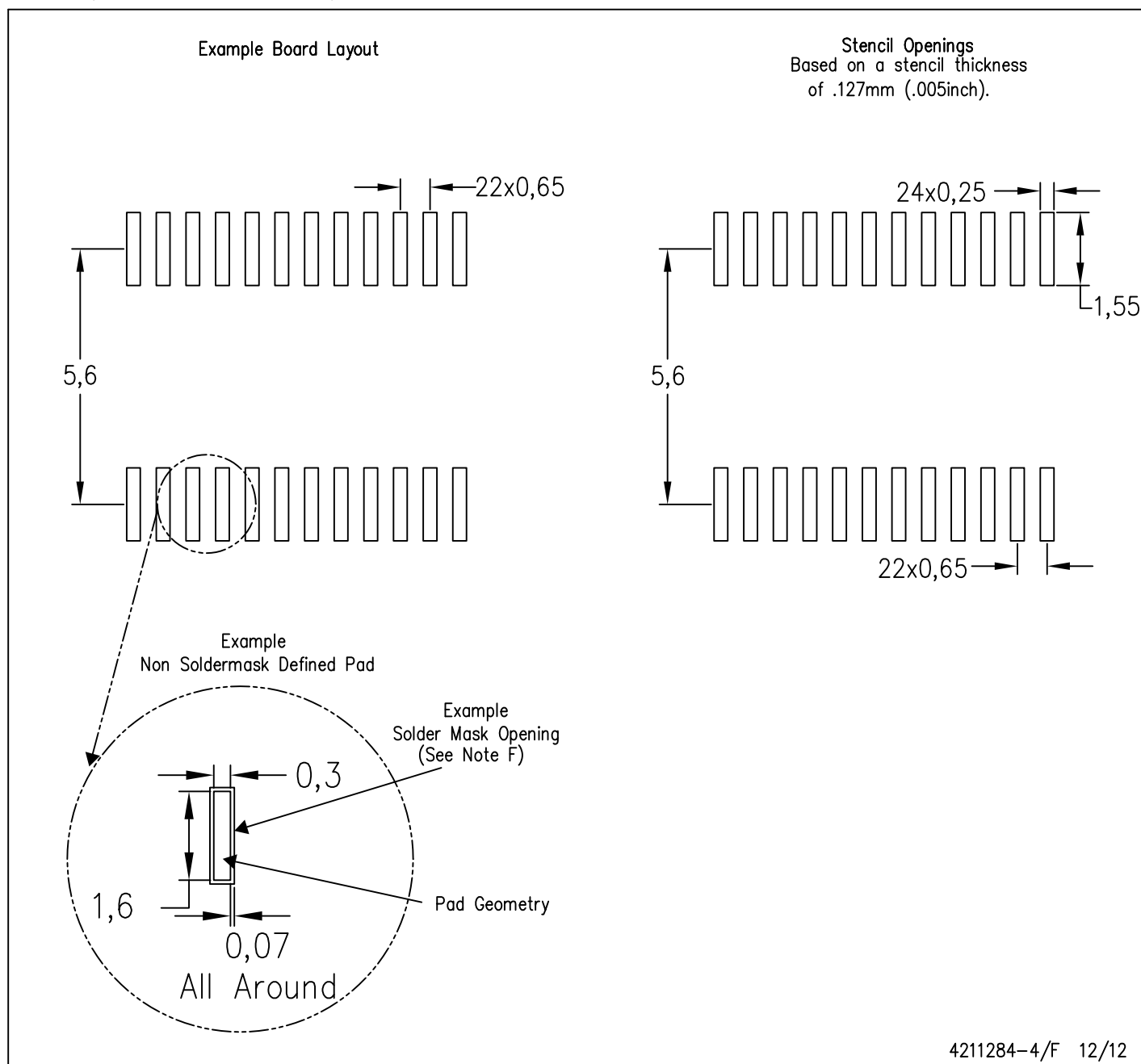


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- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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