



**128K x 36, 256K x 18
3.3V Synchronous ZBT SRAMs
3.3V I/O, Burst Counter
Pipelined Outputs**

**IDT71V3556S/XS
IDT71V3558S/XS
IDT71V3556SA/XSA
IDT71V3558SA/XSA**

Features

- ◆ 128K x 36, 256K x 18 memory configurations
- ◆ Supports high performance system speed - 200 MHz (x18) (3.2 ns Clock-to-Data Access)
- ◆ Supports high performance system speed - 166 MHz (x36) (3.5 ns Clock-to-Data Access)
- ◆ ZBT™ Feature - No dead cycles between write and read cycles
- ◆ Internally synchronized output buffer enable eliminates the need to control **OE**
- ◆ Single **R/W** (READ/WRITE) control pin
- ◆ Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications
- ◆ 4-word burst capability (interleaved or linear)
- ◆ Individual byte write (**BW**₁ - **BW**₄) control (May tie active)
- ◆ Three chip enables for simple depth expansion
- ◆ 3.3V power supply (±5%), 3.3V I/O Supply (V_{DDO})
- ◆ Optional- Boundary Scan JTAG Interface (IEEE 1149.1 compliant)
- ◆ Packaged in a JEDEC standard 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array (fBGA)

Description

The IDT71V3556/58 are 3.3V high-speed 4,718,592-bit (4.5 Megabit) synchronous SRAMs. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus, they have been given the name ZBT™, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later the associated data cycle occurs, be it read or write.

The IDT71V3556/58 contain data I/O, address and control signal registers. Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable (**CEN**) pin allows operation of the IDT71V3556/58 to be suspended as long as necessary. All synchronous inputs are ignored when (**CEN**) is high and the internal device registers will hold their previous values.

There are three chip enable pins (**CE**₁, **CE**₂, **CE**₂) that allow the user to deselect the device when desired. If any one of these three are not asserted when **ADV/LD** is low, no new memory operation can be initiated. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state two cycles after chip is deselected or a write is initiated.

Pin Description Summary

A ₀ -A ₁₇	Address Inputs	Input	Synchronous
CE ₁ , CE ₂ , CE ₂	Chip Enables	Input	Synchronous
OE	Output Enable	Input	Asynchronous
R/W	Read/Write Signal	Input	Synchronous
CEN	Clock Enable	Input	Synchronous
BW ₁ , BW ₂ , BW ₃ , BW ₄	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
ADV/LD	Advance burst address / Load new address	Input	Synchronous
LBO	Linear / Interleaved Burst Order	Input	Static
TMS	Test Mode Select	Input	Synchronous
TDI	Test Data Input	Input	Synchronous
TCK	Test Clock	Input	N/A
TDO	Test Data Output	Output	Synchronous
TRST	JTAG Reset (Optional)	Input	Asynchronous
ZZ	Sleep Mode	Input	Synchronous
I/O ₀ - I/O ₃₁ , I/O ₁ - I/O ₄	Data Input / Output	I/O	Synchronous
V_{DD} , V_{DDO}	Core Power, I/O Power	Supply	Static
V_{SS}	Ground	Supply	Static

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Description continued

The IDT71V3556/58 has an on-chip burst counter. In the burst mode, the IDT71V3556/58 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the LBO input pin. The LBO pin selects between linear and interleaved burst sequence. The ADV/LD signal is used to load a new

external address (ADV/LD = LOW) or increment the internal burst counter (ADV/LD = HIGH).

The IDT71V3556/58 SRAMs utilize IDT's latest high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA) and a 165 fine pitch ball grid array (fBGA).

Pin Definition⁽¹⁾

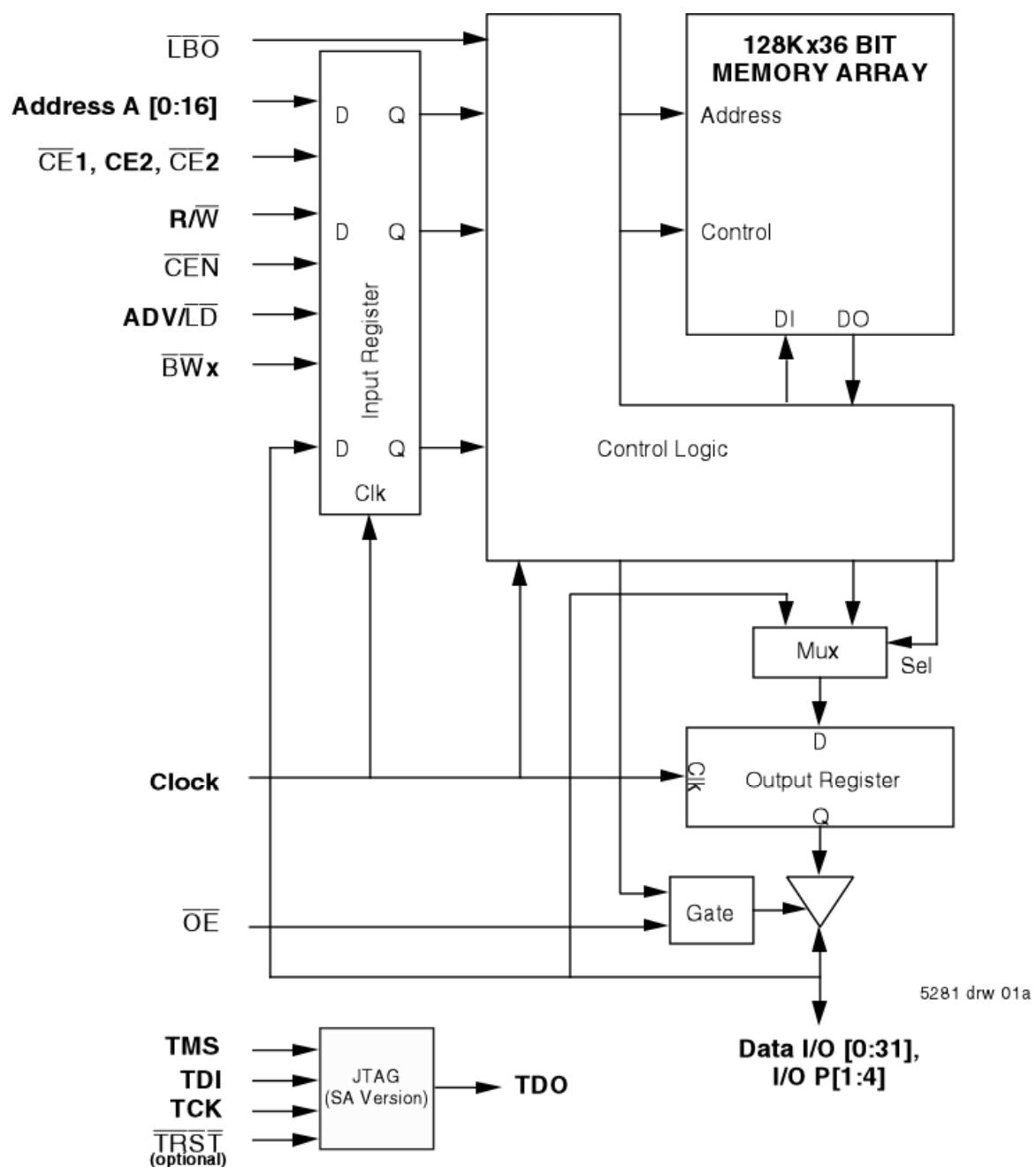
Symbol	Pin Function	I/O	Active	Description
A ₀ -A ₁₇	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/LD low, <u>CEN</u> low, and true chip enables.
ADV/LD	Advance / Load	I	N/A	ADV/LD is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/LD is low with the chip deselected, any burst in progress is terminated. When ADV/LD is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/LD is sampled high.
R/W	Read / Write	I	N/A	R/W signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place two clock cycles later.
<u>CEN</u>	Clock Enable	I	LOW	Synchronous Clock Enable Input. When <u>CEN</u> is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of <u>CEN</u> sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, <u>CEN</u> must be sampled low at rising edge of clock.
<u>BW</u> ₁ - <u>BW</u> ₄	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (When R/W and ADV/LD are sampled low) the appropriate byte write signal (<u>BW</u> ₁ - <u>BW</u> ₄) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/W is sampled high. The appropriate byte(s) of data are written into the device two cycles later. <u>BW</u> ₁ - <u>BW</u> ₄ can all be tied low if always doing write to the entire 36-bit word.
<u>CE</u> ₁ , <u>CE</u> ₂	Chip Enables	I	LOW	Synchronous active low chip enable. <u>CE</u> ₁ and <u>CE</u> ₂ are used with CE ₂ to enable the IDT71V3556/58. (<u>CE</u> ₁ or <u>CE</u> ₂ sampled high or CE ₂ sampled low) and ADV/LD low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a two cycle deselect, i.e., the data bus will tri-state two clock cycles after deselect is initiated.
CE ₂	Chip Enable	I	HIGH	Synchronous active high chip enable. CE ₂ is used with <u>CE</u> ₁ and <u>CE</u> ₂ to enable the chip. CE ₂ has inverted polarity but otherwise identical to <u>CE</u> ₁ and <u>CE</u> ₂ .
CLK	Clock	I	N/A	This is the clock input to the IDT71V3556/58. Except for <u>OE</u> , all timing references for the device are made with respect to the rising edge of CLK.
I/O ₀ -I/O ₃₁ I/O ₀ ₁ -I/O ₄	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
<u>LBO</u>	Linear Burst Order	I	LOW	Burst order selection input. When <u>LBO</u> is high the Interleaved burst sequence is selected. When <u>LBO</u> is low the Linear burst sequence is selected. <u>LBO</u> is a static input and it must not change during device operation.
<u>OE</u>	Output Enable	I	LOW	Asynchronous output enable. <u>OE</u> must be low to read data from the 71V3556/58. When <u>OE</u> is high the I/O pins are in a high-impedance state. <u>OE</u> does not need to be actively controlled for read and write cycles. In normal operation, <u>OE</u> can be tied low.
TMS	Test Mode Select	I	N/A	Gives input command for TAP controller. Sampled on rising edge of TDK. This pin has an internal pullup.
TDI	Test Data Input	I	N/A	Serial input of registers placed between TDI and TDO. Sampled on rising edge of TCK. This pin has an internal pullup.
TCK	Test Clock	I	N/A	Clock input of TAP controller. Each TAP event is clocked. Test inputs are captured on rising edge of TCK, while test outputs are driven from the falling edge of TCK. This pin has an internal pullup.
TDO	Test Data Output	O	N/A	Serial output of registers placed between TDI and TDO. This output is active depending on the state of the TAP controller.
<u>TRST</u>	JTAG Reset (Optional)	I	LOW	Optional Asynchronous JTAG reset. Can be used to reset the TAP controller, but not required. JTAG reset occurs automatically at power up and also resets using TMS and TCK per IEEE 1149.1. If not used <u>TRST</u> can be left floating. This pin has an internal pullup. Only available in BGA package.
ZZ	Sleep Mode	I	HIGH	Synchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V3556/3558 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. This pin has an internal pulldown.
V _{DD}	Power Supply	N/A	N/A	3.3V core power supply.
V _{DDQ}	Power Supply	N/A	N/A	3.3V I/O Supply.
V _{SS}	Ground	N/A	N/A	Ground.

NOTE:

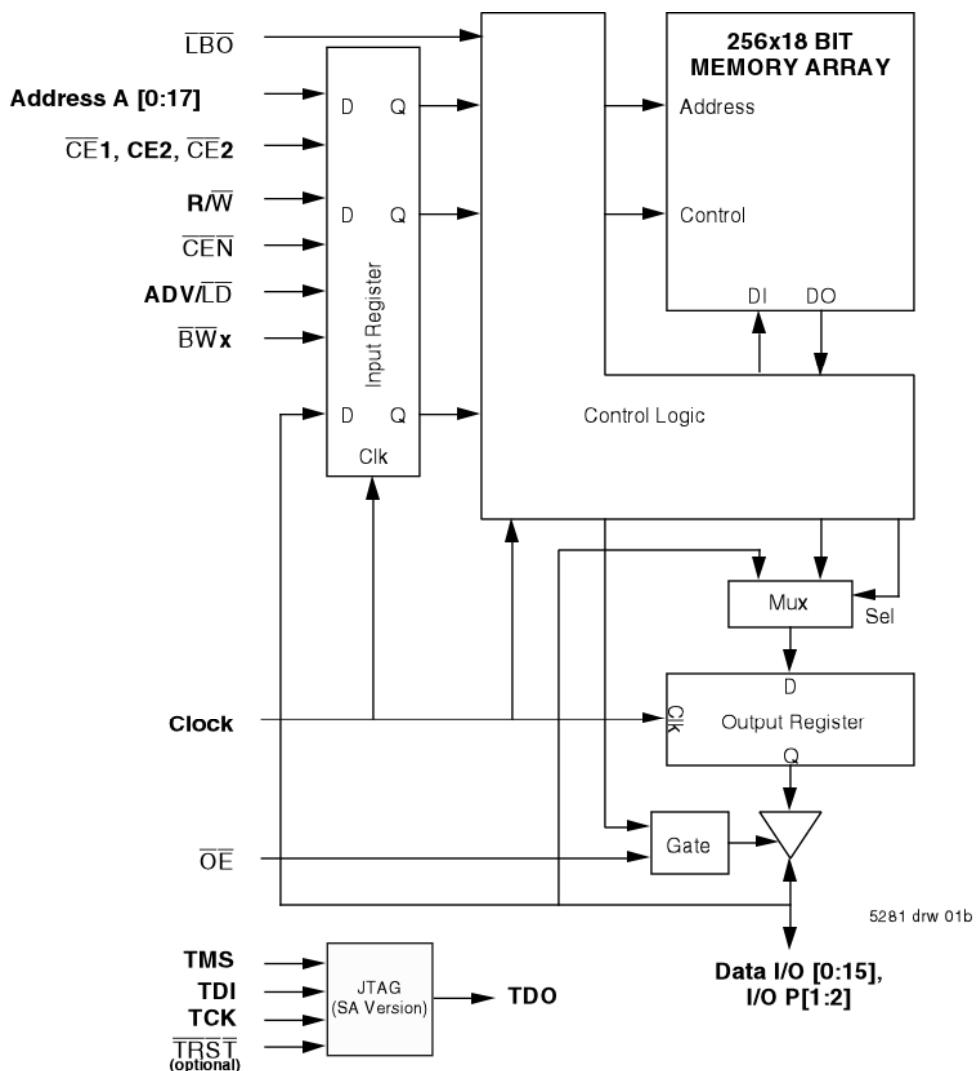
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1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Functional Block Diagram



Functional Block Diagram



Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V _{DDO}	I/O Supply Voltage	3.135	3.3	3.465	V
V _{SS}	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage - Inputs	2.0	—	V _{DD} + 0.3	V
V _{IH}	Input High Voltage - I/O	2.0	—	V _{DDO} + 0.3 ²⁾	V
V _{IL}	Input Low Voltage	-0.3 ¹⁾	—	0.8	V

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NOTES:

1. V_{IL} (min.) = -1.0V for pulse width less than t_{cyc}/2, once per cycle.
2. V_{IH} (max.) = +6.0V for pulse width less than t_{cyc}/2, once per cycle.

Recommended Operating Temperature and Supply Voltage

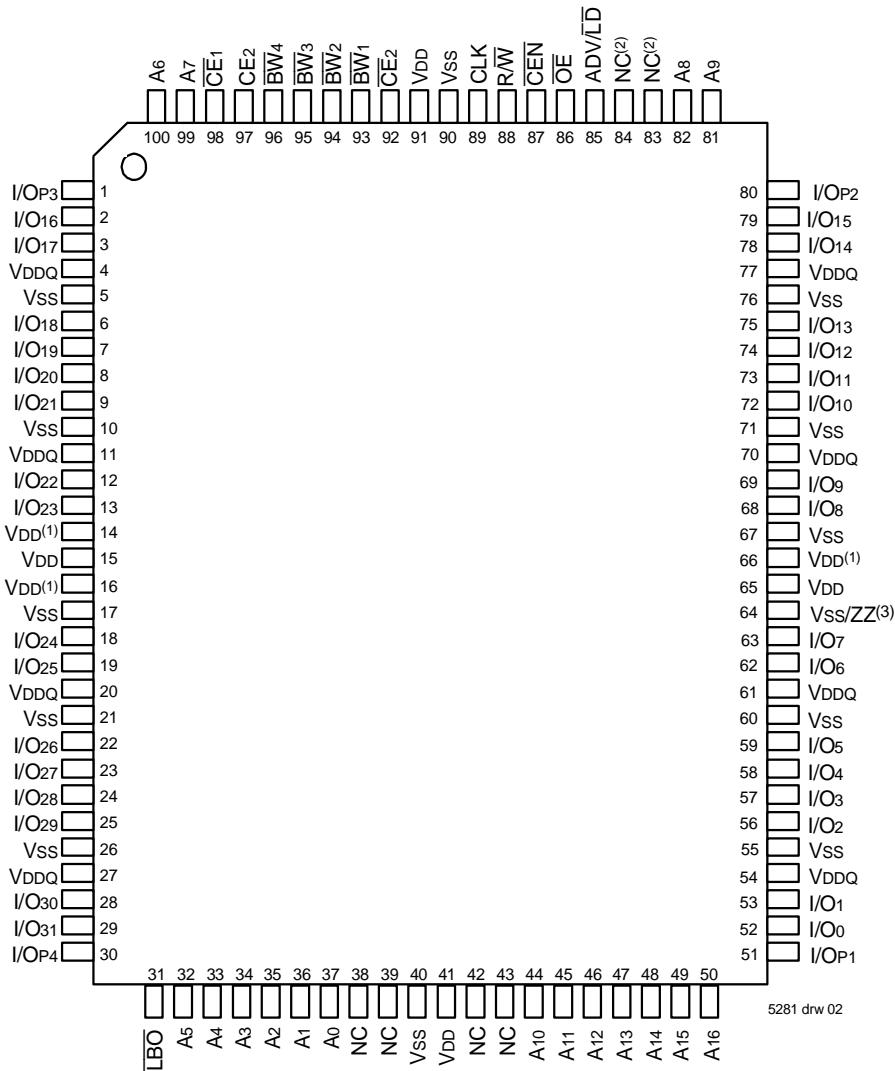
Grade	Temperature ⁽¹⁾	V _{SS}	V _{DD}	V _{DDQ}
Commercial	0°C to +70°C	0V	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	3.3V±5%

NOTES.

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1. TA is the "instant on" case temperature.

Pin Configuration - 128K x 36

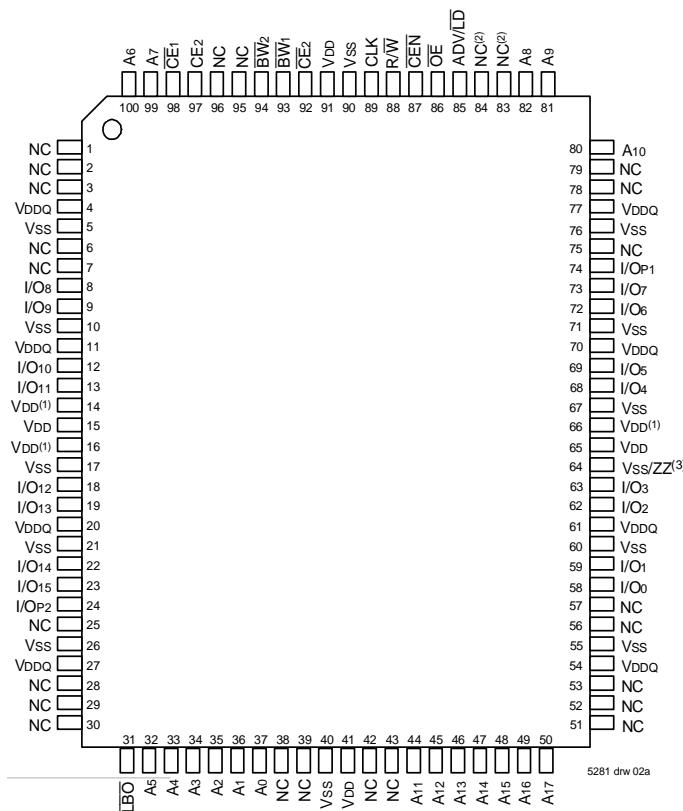


Top View 100 TOFP

NOTES:

1. Pins 14, 16 and 66 do not have to be connected directly to V_{DD} as long as the input voltage is $\geq V_{IH}$.
2. Pins 83 and 84 are reserved for future 8M and 16M respectively.
3. Pin 64 does not have to be connected directly to V_{SS} as long as the input voltage is $\leq V_{IL}$; on the latest die revision this pin supports ZZ (sleep mode).

Pin Configuration - 256K x 18



Top View
100 TQFP

NOTES:

1. Pins 14, 16 and 66 do not have to be connected directly to VDD as long as the input voltage is $\geq V_{IH}$.
2. Pins 83 and 84 are reserved for future 8M and 16M respectively.
3. Pin 64 does not have to be connected directly to VSS as long as the input voltage is $\leq V_{IL}$; on the latest die revision this pin supports ZZ (sleep mode).

100 Pin TQFP Capacitance⁽¹⁾

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 3dV$	5	pF
C_{IO}	I/O Capacitance	$V_{OUT} = 3dV$	7	pF

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165 fBGA Capacitance⁽¹⁾

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 3dV$	TBD	pF
C_{IO}	I/O Capacitance	$V_{OUT} = 3dV$	TBD	pF

5281 tbl 07b

NOTE.

NOTE: 1. This parameter is guaranteed by device characterization, but not production tested.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial Values	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
$V_{TERM}^{(3,6)}$	Terminal Voltage with Respect to GND	-0.5 to V_{DD}	V
$V_{TERM}^{(4,6)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{DD} + 0.5$	V
$V_{TERM}^{(5,6)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{DDQ} + 0.5$	V
$T_A^{(7)}$	Commercial Operating Temperature	-0 to +70	°C
	Industrial Operating Temperature	-40 to +85	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	2.0	W
I_{OUT}	DC Output Current	50	mA

5281 tbl 06

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{DDO} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDO} during power supply ramp up.
7. T_A is the "instant on" case temperature.

119 BGA Capacitance⁽¹⁾

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 3dV$	7	pF
C_{IO}	I/O Capacitance	$V_{OUT} = 3dV$	7	pF

5281 tbl 07a

Pin Configuration - 128K x 36, 119 BGA

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	NC(2)	A8	A16	VDDQ
B	NC	CE2	A3	ADV/LD	A9	CE2	NC
C	NC	A7	A2	VDD	A12	A15	NC
D	I/O16	I/OP3	VSS	NC	VSS	I/OP2	I/O15
E	I/O17	I/O18	VSS	CE1	VSS	I/O13	I/O14
F	VDDQ	I/O19	VSS	OE	VSS	I/O12	VDDQ
G	I/O20	I/O21	BW3	NC(2)	BW2	I/O11	I/O10
H	I/O22	I/O23	VSS	R/W	VSS	I/O9	I/O8
J	VDDQ	VDD	VDD(1)	VDD	VDD(1)	VDD	VDDQ
K	I/O24	I/O26	VSS	CLK	VSS	I/O6	I/O7
L	I/O25	I/O27	BW4	NC	BW1	I/O4	I/O5
M	VDDQ	I/O28	VSS	CEN	VSS	I/O3	VDDQ
N	I/O29	I/O30	VSS	A1	VSS	I/O2	I/O1
P	I/O31	I/OP4	VSS	A0	VSS	I/OP1	I/O0
R	NC	A5	LBO	VDD	VDD(1)	A13	NC
T	NC	NC	A10	A11	A14	NC	NC/ZZ ⁽⁵⁾
U	VDDQ	NC/TMS ⁽³⁾	NC/TDI ⁽³⁾	NC/TCK ⁽³⁾	NC/TDO ⁽³⁾	NC/TRST ^(3,4)	VDDQ

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Top View

Pin Configuration - 256K x 18, 119 BGA

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	NC(2)	A8	A16	VDDQ
B	NC	CE2	A3	ADV/LD	A9	CE2	NC
C	NC	A7	A2	VDD	A13	A17	NC
D	I/O8	NC	VSS	NC	VSS	I/OP1	NC
E	NC	I/O9	VSS	CE1	VSS	NC	I/O7
F	VDDQ	NC	VSS	OE	VSS	I/O6	VDDQ
G	NC	I/O10	BW2	NC(2)	VSS	NC	I/O5
H	I/O11	NC	VSS	R/W	VSS	I/O4	NC
J	VDDQ	VDD	VDD(1)	VDD	VDD(1)	VDD	VDDQ
K	NC	I/O12	VSS	CLK	VSS	NC	I/O3
L	I/O13	NC	VSS	NC	BW1	I/O2	NC
M	VDDQ	I/O14	VSS	CEN	VSS	NC	VDDQ
N	I/O15	NC	VSS	A1	VSS	I/O1	NC
P	NC	I/OP2	VSS	A0	VSS	NC	I/O0
R	NC	A5	LBO	VDD	VDD(1)	A12	NC
T	NC	A10	A15	NC	A14	A11	NC/ZZ ⁽⁵⁾
U	VDDQ	NC/TMS ⁽³⁾	NC/TDI ⁽³⁾	NC/TCK ⁽³⁾	NC/TDO ⁽³⁾	NC/TRST ^(3,4)	VDDQ

5281 drw 13B

Top View

NOTES:

1. J3, J5, and R5 do not have to be directly connected to Vdd as long as the input voltage is $\geq V_{IH}$.
2. G4 and A4 are reserved for future 8M and 16M respectively.
3. These pins are NC for the "S" version or the JTAG signal listed for the "SA" version.
4. TRST is offered as an optional JTAG reset if required in the application. If not needed, can be left floating and will internally be pulled to VDD.
5. Pin T7 does not have to be connected directly to Vss as long as the input voltage is $\leq V_{IL}$; on the latest die revision this pin supports ZZ (sleep mode).

Pin Configuration - 128K x 36, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC ⁽²⁾	A7	$\overline{CE1}$	$\overline{BW3}$	$\overline{BW2}$	$\overline{CE2}$	\overline{CEN}	ADV/LD	NC ⁽²⁾	A8	NC
B	NC	A6	CE2	$\overline{BW4}$	$\overline{BW1}$	CLK	R/W	\overline{OE}	NC ⁽²⁾	A9	NC ⁽²⁾
C	I/O ₃	NC	VDDQ	VSS	VSS	VSS	VSS	VDDQ	NC	I/O ₂	
D	I/O ₁₇	I/O ₁₆	VDDQ	VDD	VSS	VSS	VSS	VDDQ	I/O ₁₅	I/O ₁₄	
E	I/O ₁₉	I/O ₁₈	VDDQ	VDD	VSS	VSS	VDD	VDDQ	I/O ₁₃	I/O ₁₂	
F	I/O ₂₁	I/O ₂₀	VDDQ	VDD	VSS	VSS	VDD	VDDQ	I/O ₁₁	I/O ₁₀	
G	I/O ₂₃	I/O ₂₂	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O ₉	I/O ₈
H	VDD ⁽¹⁾	VDD ⁽¹⁾	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	NC/ZZ ⁽⁵⁾
J	I/O ₂₅	I/O ₂₄	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O ₇	I/O ₆
K	I/O ₂₇	I/O ₂₆	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O ₅	I/O ₄
L	I/O ₂₉	I/O ₂₈	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O ₃	I/O ₂
M	I/O ₃₁	I/O ₃₀	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O ₁	I/O ₀
N	I/O ₄	NC	VDDQ	VSS	NC/ $\overline{TRST}^{(3,4)}$	NC	VDD ⁽¹⁾	VSS	VDDQ	NC	I/O ₁
P	NC	NC ⁽²⁾	A5	A2	NC/TDI ⁽³⁾	A1	NC/TDO ⁽³⁾	A10	A13	A14	NC
R	\overline{LBO}	NC ⁽²⁾	A4	A3	NC/TMS ⁽³⁾	A0	NC/TCK ⁽³⁾	A11	A12	A15	A16

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Pin Configuration - 256K x 18, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC ⁽²⁾	A7	$\overline{CE1}$	$\overline{BW2}$	NC	$\overline{CE2}$	\overline{CEN}	ADV/LD	NC ⁽²⁾	A8	A10
B	NC	A6	CE2	NC	$\overline{BW1}$	CLK	R/W	\overline{OE}	NC ⁽²⁾	A9	NC ⁽²⁾
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VDDQ	NC	I/O ₁	
D	NC	I/O ₈	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O ₇
E	NC	I/O ₉	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O ₆
F	NC	I/O ₁₀	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O ₅
G	NC	I/O ₁₁	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O ₄
H	VDD ⁽¹⁾	VDD ⁽¹⁾	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	NC/ZZ ⁽⁵⁾
J	I/O ₁₂	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O ₃	NC
K	I/O ₁₃	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O ₂	NC
L	I/O ₁₄	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O ₁	NC
M	I/O ₁₅	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O ₀	NC
N	I/O ₂	NC	VDDQ	VSS	NC/ $\overline{TRST}^{(3,4)}$	NC	VDD ⁽¹⁾	VSS	VDDQ	NC	NC
P	NC	NC ⁽²⁾	A5	A2	NC/TDI ⁽³⁾	A1	NC/TDO ⁽³⁾	A11	A14	A15	NC
R	\overline{LBO}	NC ⁽²⁾	A4	A3	NC/TMS ⁽³⁾	A0	NC/TCK ⁽³⁾	A12	A13	A16	A17

5281 tbl 25a

NOTES:

- H1, H2, and N7 do not have to be directly connected to VDD as long as the input voltage is $\geq V_{IH}$.
- A9, B9, B11, A1, R2 and P2 are reserved for future 9M, 18M, 36M, 72M, 144M and 288M respectively.
- These pins are NC for the "S" version or the JTAG signal listed for the "SA" version.
- TRST is offered as an optional JTAG reset if required in the application. If not needed, can be left floating and will internally be pulled to VDD.
- Pin H11 does not have to be connected directly to VSS as long as the input voltage is $\leq V_{IL}$; on the latest die revision this pin supports ZZ (sleep mode).

Synchronous Truth Table ⁽¹⁾

CEN	R/W	Chip ⁽⁵⁾ Enable	ADV/LD	BWx	ADDRESS USED	PREVIOUS CYCLE	CURRENT CYCLE	I/O (2 cycles later)
L	L	Select	L	Valid	External	X	LOAD WRITE	D ⁽⁷⁾
L	H	Select	L	X	External	X	LOAD READ	Q ⁽⁷⁾
L	X	X	H	Valid	Internal	LOAD WRITE / BURST WRITE	BURST WRITE (Advance burst counter) ⁽²⁾	D ⁽⁷⁾
L	X	X	H	X	Internal	LOAD READ / BURST READ	BURST READ (Advance burst counter) ⁽²⁾	Q ⁽⁷⁾
L	X	Deselect	L	X	X	X	DESELECT or STOP ⁽³⁾	HiZ
L	X	X	H	X	X	DESELECT / NOOP	NOOP	HiZ
H	X	X	X	X	X	X	SUSPEND ⁽⁴⁾	Previous Value

5281 tbl 08

NOTES:

1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. When ADV/LD signal is sampled high, the internal burst counter is incremented. The R/W signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/W signal when the first address is loaded at the beginning of the burst cycle.
3. Deselect cycle is initiated when either (\overline{CE}_1 or \overline{CE}_2 is sampled high or CE_2 is sampled low) and ADV/LD is sampled low at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
4. When CEN is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/Os remains unchanged.
5. To select the chip requires $\overline{CE}_1 = L$, $\overline{CE}_2 = L$, $CE_2 = H$ on these chip enables. Chip is deselected if any one of the chip enables is false.
6. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.
7. Q - Data read from the device, D - data written to the device.

Partial Truth Table for Writes ⁽¹⁾

OPERATION	R/W	BW₁	BW₂	BW₃⁽³⁾	BW₄⁽³⁾
READ	H	X	X	X	X
WRITE ALL BYTES	L	L	L	L	L
WRITE BYTE 1 (I/O[0:7], I/O _{P1}) ⁽²⁾	L	L	H	H	H
WRITE BYTE 2 (I/O[8:15], I/O _{P2}) ⁽²⁾	L	H	L	H	H
WRITE BYTE 3 (I/O[16:23], I/O _{P3}) ^(2,3)	L	H	H	L	H
WRITE BYTE 4 (I/O[24:31], I/O _{P4}) ^(2,3)	L	H	H	H	L
NO WRITE	L	H	H	H	H

5281 tbl 09

NOTES:

1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.
3. N/A for X18 configuration.

Interleaved Burst Sequence Table (**LBO**=V_{DD})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address ⁽¹⁾	1	1	1	0	0	1	0	0

5281 tbl 10

NOTE:

- Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Linear Burst Sequence Table (**LBO**=V_{SS})

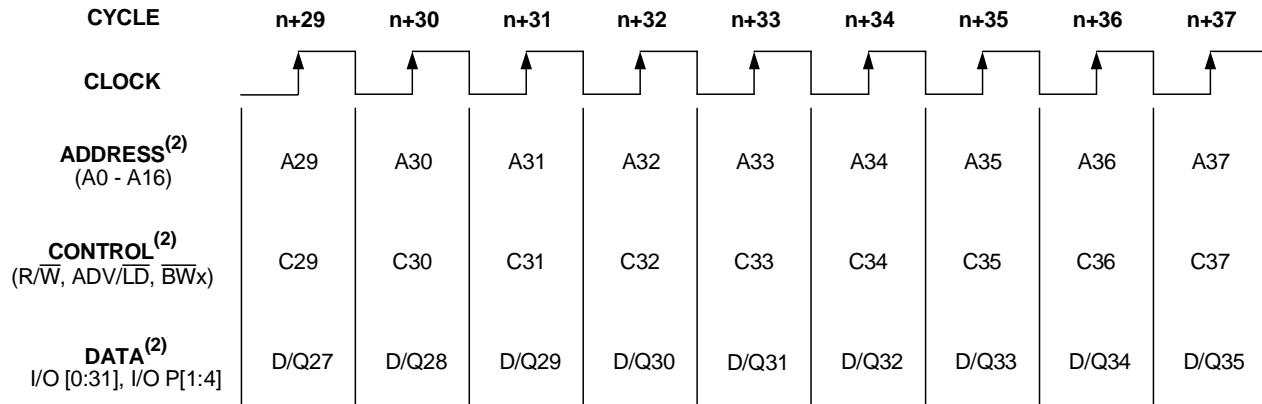
	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address ⁽¹⁾	1	1	0	0	0	1	1	0

5281 tbl 11

NOTE:

- Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Functional Timing Diagram (1)



5281 dw 03

NOTES:

- This assumes \overline{CEN} , \overline{CE}_1 , CE_2 , \overline{CE}_2 are all true.
- All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.

Device Operation - Showing Mixed Load, Burst,
Deselect and NOOP Cycles ⁽²⁾

Cycle	Address	R/W	ADV/LD	CE ⁽¹⁾	CEN	BWx	OE	I/O	Comments
n	A ₀	H	L	L	L	X	X	X	Load read
n+1	X	X	H	X	L	X	X	X	Burst read
n+2	A ₁	H	L	L	L	X	L	Q ₀	Load read
n+3	X	X	L	H	L	X	L	Q ₀₊₁	Deselect or STOP
n+4	X	X	H	X	L	X	L	Q ₁	NOOP
n+5	A ₂	H	L	L	L	X	X	Z	Load read
n+6	X	X	H	X	L	X	X	Z	Burst read
n+7	X	X	L	H	L	X	L	Q ₂	Deselect or STOP
n+8	A ₃	L	L	L	L	L	L	Q ₂₊₁	Load write
n+9	X	X	H	X	L	L	X	Z	Burst write
n+10	A ₄	L	L	L	L	L	X	D ₃	Load write
n+11	X	X	L	H	L	X	X	D ₃₊₁	Deselect or STOP
n+12	X	X	H	X	L	X	X	D ₄	NOOP
n+13	A ₅	L	L	L	L	L	X	Z	Load write
n+14	A ₆	H	L	L	L	X	X	Z	Load read
n+15	A ₇	L	L	L	L	L	X	D ₅	Load write
n+16	X	X	H	X	L	L	L	Q ₆	Burst write
n+17	A ₈	H	L	L	L	X	X	D ₇	Load read
n+18	X	X	H	X	L	X	X	D ₇₊₁	Burst read
n+19	A ₉	L	L	L	L	L	L	Q ₈	Load write

5281tbl 12

NOTES:

1. $\overline{CE} = L$ is defined as $\overline{CE}_1 = L$, $\overline{CE}_2 = L$ and $CE_2 = H$. $\overline{CE} = H$ is defined as $\overline{CE}_1 = H$, $\overline{CE}_2 = H$ or $CE_2 = L$.
2. H = High; L = Low; X = Don't Care; Z = High Impedance.

Read Operation ⁽¹⁾

Cycle	Address	R/W	ADV/LD	CE ⁽²⁾	CEN	BWx	OE	I/O	Comments
n	A ₀	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	X	X	L	Q ₀	Contents of Address A ₀ Read Out

5281tbl 13

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE} = L$ is defined as $\overline{CE}_1 = L$, $\overline{CE}_2 = L$ and $CE_2 = H$. $\overline{CE} = H$ is defined as $\overline{CE}_1 = H$, $\overline{CE}_2 = H$ or $CE_2 = L$.

Burst Read Operation (1)

Cycle	Address	R/W	ADV/LD	CE ⁽²⁾	CEN	BWx	OE	I/O	Comments
n	A ₀	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	X	X	Clock Setup Valid, Advance Counter
n+2	X	X	H	X	L	X	L	Q ₀	Address A ₀ Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	Q ₀₊₁	Address A ₀₊₁ Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	Q ₀₊₂	Address A ₀₊₂ Read Out, Inc. Count
n+5	A ₁	H	L	L	L	X	L	Q ₀₊₃	Address A ₀₊₃ Read Out, Load A ₁
n+6	X	X	H	X	L	X	L	Q ₀	Address A ₀ Read Out, Inc. Count
n+7	X	X	H	X	L	X	L	Q ₁	Address A ₁ Read Out, Inc. Count
n+8	A ₂	H	L	L	L	X	L	Q ₁₊₁	Address A ₁₊₁ Read Out, Load A ₂

5281tbl 14

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance..
2. CE = L is defined as CE₁ = L, CE₂ = L and CE₂ = H. CE = H is defined as CE₁ = H, CE₂ = H or CE₂ = L.

Write Operation (1)

Cycle	Address	R/W	ADV/LD	CE ⁽²⁾	CEN	BWx	OE	I/O	Comments
n	A ₀	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	L	X	X	D ₀	Write to Address A ₀

5281tbl 15

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance..
2. CE = L is defined as CE₁ = L, CE₂ = L and CE₂ = H. CE = H is defined as CE₁ = H, CE₂ = H or CE₂ = L.

Burst Write Operation (1)

Cycle	Address	R/W	ADV/LD	CE ⁽²⁾	CEN	BWx	OE	I/O	Comments
n	A ₀	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	X	Clock Setup Valid, Inc. Count
n+2	X	X	H	X	L	L	X	D ₀	Address A ₀ Write, Inc. Count
n+3	X	X	H	X	L	L	X	D ₀₊₁	Address A ₀₊₁ Write, Inc. Count
n+4	X	X	H	X	L	L	X	D ₀₊₂	Address A ₀₊₂ Write, Inc. Count
n+5	A ₁	L	L	L	L	L	X	D ₀₊₃	Address A ₀₊₃ Write, Load A ₁
n+6	X	X	H	X	L	L	X	D ₀	Address A ₀ Write, Inc. Count
n+7	X	X	H	X	L	L	X	D ₁	Address A ₁ Write, Inc. Count
n+8	A ₂	L	L	L	L	L	X	D ₁₊₁	Address A ₁₊₁ Write, Load A ₂

5281tbl 16

NOTES:

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance..
2. CE = L is defined as CE₁ = L, CE₂ = L and CE₂ = H. CE = H is defined as CE₁ = H, CE₂ = H or CE₂ = L.

Read Operation with Clock Enable Used ⁽¹⁾

Cycle	Address	R/W	ADV/LD	CE ⁽²⁾	CEN	BWx	OE	I/O	Comments
n	A ₀	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A ₁	H	L	L	L	X	X	X	Clock Valid
n+3	X	X	X	X	H	X	L	Q ₀	Clock Ignored. Data Q ₀ is on the bus.
n+4	X	X	X	X	H	X	L	Q ₀	Clock Ignored. Data Q ₀ is on the bus.
n+5	A ₂	H	L	L	L	X	L	Q ₀	Address A ₀ Read out (bus trans.)
n+6	A ₃	H	L	L	L	X	L	Q ₁	Address A ₁ Read out (bus trans.)
n+7	A ₄	H	L	L	L	X	L	Q ₂	Address A ₂ Read out (bus trans.)

5281 tbl 17

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.

2. CE = L is defined as CE₁ = L, CE₂ = L and CE₂ = H. CE = H is defined as CE₁ = H, CE₂ = H or CE₂ = L.

Write Operation with Clock Enable Used ⁽¹⁾

Cycle	Address	R/W	ADV/LD	CE ⁽²⁾	CEN	BWx	OE	I/O	Comments
n	A ₀	L	L	L	L	L	X	X	Address and Control meet setup.
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored.
n+2	A ₁	L	L	L	L	L	X	X	Clock Valid.
n+3	X	X	X	X	H	X	X	X	Clock Ignored.
n+4	X	X	X	X	H	X	X	X	Clock Ignored.
n+5	A ₂	L	L	L	L	L	X	D ₀	Write Data D ₀
n+6	A ₃	L	L	L	L	L	X	D ₁	Write Data D ₁
n+7	A ₄	L	L	L	L	L	X	D ₂	Write Data D ₂

5281 tbl 18

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.

2. CE = L is defined as CE₁ = L, CE₂ = L and CE₂ = H. CE = H is defined as CE₁ = H, CE₂ = H or CE₂ = L.

Read Operation with CHIP Enable Used (1)

Cycle	Address	R/ W	ADV/ LD	CE ⁽²⁾	CEN	BWx	OE	I/O ⁽³⁾	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A ₀	H	L	L	L	X	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A ₁	H	L	L	L	X	L	Q ₀	Address A ₀ Read out. Load A ₁ .
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	L	Q ₁	Address A ₁ Read out. Deselected.
n+7	A ₂	H	L	L	L	X	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	L	Q ₂	Address A ₂ Read out. Deselected.

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NOTES:

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. **CE** = L is defined as **CE**₁ = L, **CE**₂ = L and **CE**₂ = H. **CE** = H is defined as **CE**₁ = H, **CE**₂ = H or **CE**₂ = L.
3. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

Write Operation with Chip Enable Used (1)

Cycle	Address	R/ W	ADV/ LD	CE ⁽²⁾	CEN	BWx	OE	I/O ⁽³⁾	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A ₀	L	L	L	L	L	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A ₁	L	L	L	L	L	X	D ₀	Address D ₀ Write in. Load A ₁ .
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	X	D ₁	Address D ₁ Write in. Deselected.
n+7	A ₂	L	L	L	L	L	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	X	D ₂	Address D ₂ Write in. Deselected.

5281tbl 20

NOTES:

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. **CE** = L is defined as **CE**₁ = L, **CE**₂ = L and **CE**₂ = H. **CE** = H is defined as **CE**₁ = H, **CE**₂ = H or **CE**₂ = L.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD} = 3.3V \pm 5\%$)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$ I_{L1} $	Input Leakage Current	$V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$	—	5	μA
$ I_{L2} $	LBO, JTAG and ZZ Input Leakage Current ⁽¹⁾	$V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$	—	30	μA
$ I_{LO} $	Output Leakage Current	$V_{OUT} = 0V \text{ to } V_{DDQ}, \text{Device Deselected}$	—	5	μA
V_{OL}	Output Low Voltage	$I_{OL} = +8mA, V_{DD} = \text{Min.}$	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -8mA, V_{DD} = \text{Min.}$	2.4	—	V

5281 tbl 21

NOTE:

1. The \overline{LBO} , \overline{TMS} , \overline{TDI} , \overline{TCK} and \overline{TRST} pins will be internally pulled to V_{DD} and ZZ will be internally pulled if they are not actively driven in the application.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ⁽¹⁾ ($V_{DD} = 3.3V \pm 5\%$)

Symbol	Parameter	Test Conditions	200MHz ⁽⁴⁾	166MHz		133MHz		100MHz		Unit
			Com'l Only	Com'l	Ind	Com'l	Ind	Com'l	Ind	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, $ADV/LD = X, V_{DD} = \text{Max.}, V_{IN} \geq V_{IH} \text{ or } \leq V_{IL}, f = f_{MAX}^{(2)}$	400	350	360	300	310	250	255	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = 0^{(2,3)}$	40	40	45	40	45	40	45	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } < V_{LD}, f = f_{MAX}^{(2,3)}$	130	120	130	110	120	100	110	mA
I_{SB3}	Idle Power Supply Current	Device Selected, Outputs Open, $CEN \geq V_{IH}, V_{DD} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = f_{MAX}^{(2,3)}$	40	40	45	40	45	40	45	mA

NOTES:

1. All values are maximum guaranteed values.
2. At $f = f_{MAX}$, inputs are cycling at the maximum frequency of read cycles of $1/t_{cyc}$; $f=0$ means no input lines are changing.
3. For I/Os $V_{HD} = V_{DDQ} - 0.2V$, $V_{LD} = 0.2V$. For other inputs $V_{HD} = V_{DD} - 0.2V$, $V_{LD} = 0.2V$.
4. Only available in 256K x 18 configuration.

AC Test Loads

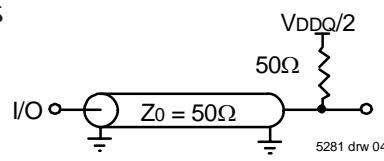


Figure 1. AC Test Load

AC Test Conditions ($V_{DDQ} = 3.3V$)

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figure 1

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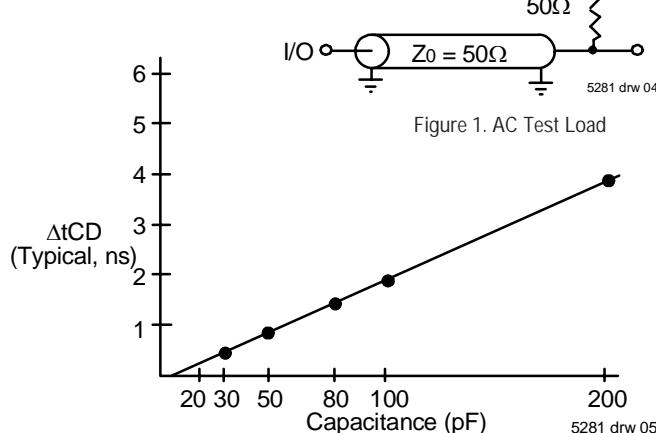


Figure 2. Lumped Capacitive Load, Typical Derating

AC Electrical Characteristics

(V_{DD} = 3.3V +/-5%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	200MHz ⁽⁶⁾		166MHz		133MHz		100MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC}	Clock Cycle Time	5	—	6	—	7.5	—	10	—	ns
t _F ⁽¹⁾	Clock Frequency	—	200	—	166	—	133	—	100	MHz
t _{CH} ⁽²⁾	Clock High Pulse Width	1.8	—	1.8	—	2.2	—	3.2	—	ns
t _{CL} ⁽²⁾	Clock Low Pulse Width	1.8	—	1.8	—	2.2	—	3.2	—	ns

Output Parameters

t _{CD}	Clock High to Valid Data	—	3.2	—	3.5	—	4.2	—	5	ns
t _{CD} C	Clock High to Data Change	1	—	1	—	1	—	1	—	ns
t _{CLZ} ^(3,4,5)	Clock High to Output Active	1	—	1	—	1	—	1	—	ns
t _{CHZ} ^(3,4,5)	Clock High to Data High-Z	1	3	1	3	1	3	1	3.3	ns
t _{OE}	Output Enable Access Time	—	3.2	—	3.5	—	4.2	—	5	ns
t _{OLZ} ^(3,4)	Output Enable Low to Data Active	0	—	0	—	0	—	0	—	ns
t _{OHZ} ^(3,4)	Output Enable High to Data High-Z	—	3.5	—	3.5	—	4.2	—	5	ns

Set Up Times

t _{SE}	Clock Enable Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t _{SA}	Address Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t _{SD}	Data In Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t _{SW}	Read/Write (R/W) Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t _{ADV}	Advance/Load (ADV/LD) Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t _{SC}	Chip Enable/Select Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns
t _{SB}	Byte Write Enable (BWx) Setup Time	1.5	—	1.5	—	1.7	—	2.0	—	ns

Hold Times

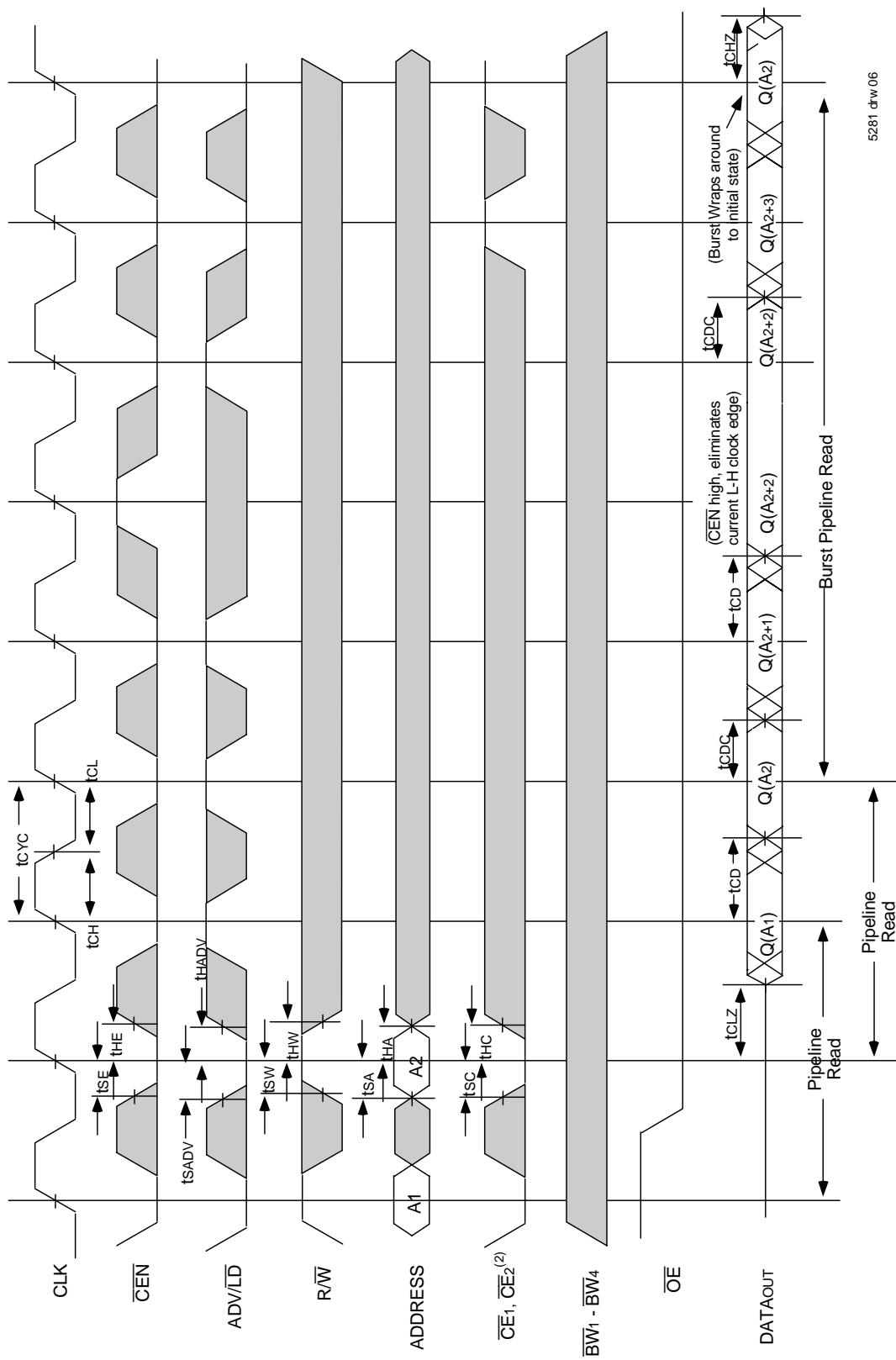
t _{HE}	Clock Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{HW}	Read/Write (R/W) Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{HADV}	Advance/Load (ADV/LD) Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
t _{HB}	Byte Write Enable (BWx) Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns

NOTES:

1. $t_f = 1/t_{cyc}$.
2. Measured as HIGH above 0.6V_{DD} and LOW below 0.4V_{DD}.
3. Transition is measured $\pm 200\text{mV}$ from steady-state.
4. These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
5. To avoid bus contention, the output buffers are designed such that t_{CHZ} (device turn-off) is about 1ns faster than t_{CLZ} (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t_{CLZ} is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 3.465V) than t_{CHZ}, which is a Max. parameter (worse case at 70 deg. C, 3.135V).
6. Commercial temperature range only. Only available in 256K x 18 configuration.

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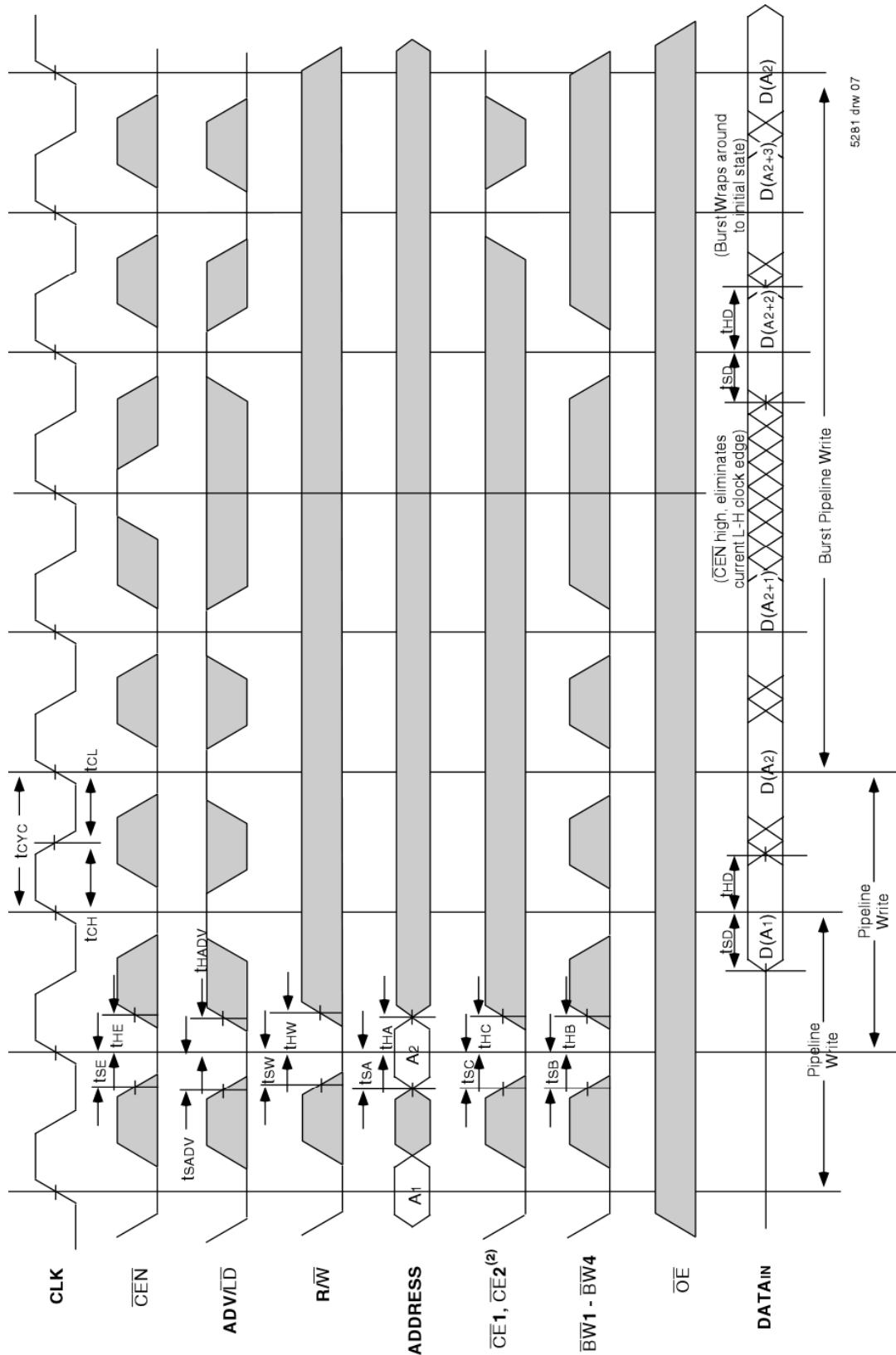
Timing Waveform of Read Cycle ^(1,2,3,4)



NOTES:

1. Q(A₁) represents the first output from the external address A₁. Q(A₂) represents the next output data in the burst sequence of the base address A₂, etc. where address bits A₀ and A₁ are advancing for the four word burst in the sequence defined by the state of the **[BO]** input.
2. CE2 timing transitions are identical but inverted to the **CE1** and **CE2** signals. For example, when **CE1** and **CE2** are LOW on this waveform, **CE2** is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD LOW.
4. R/W is don't care when the SRAM is bursting (ADV/LD sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the **R/W** signal when new address and control are loaded into the SRAM.

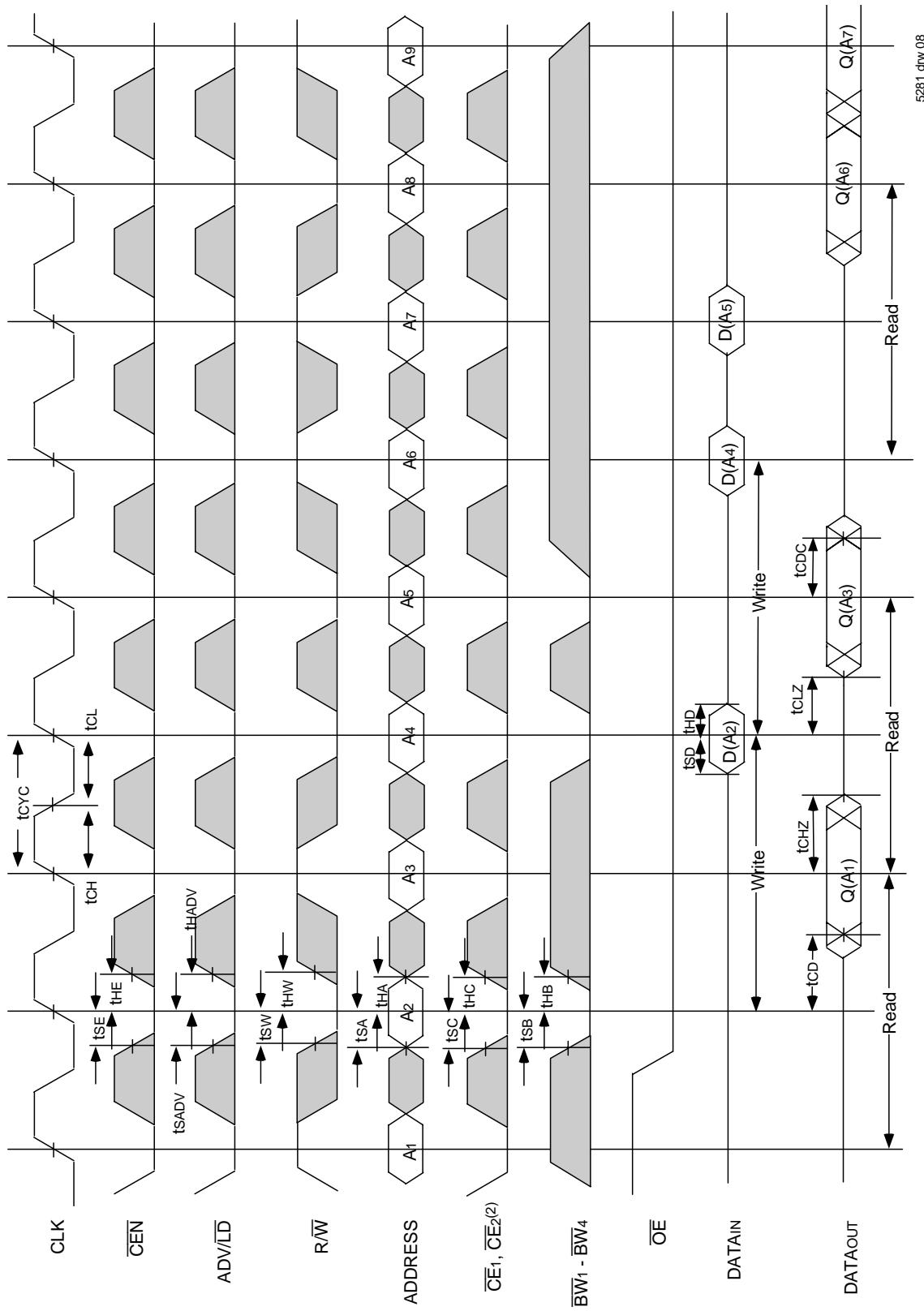
Timing Waveform of Write Cycles ^(1,2,3,4,5)



NOTES:

1. D (A1) represents the first input to the external address A1. D (A2+) represents the next input data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CE2 timing transitions are identical but inverted to the $\overline{CE1}$ and $\overline{CE2}$ signals. For example, when $\overline{CE1}$ and $\overline{CE2}$ are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/ID LOW.
4. \overline{RW} is don't care when the SRAM is bursting (ADV/ID sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the \overline{RW} signal when new address and control are loaded into the SRAM.
5. Individual Byte Write Signals (\overline{BWx}) must be valid on all write and burst-write cycles. A write cycle is initiated when \overline{RW} signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

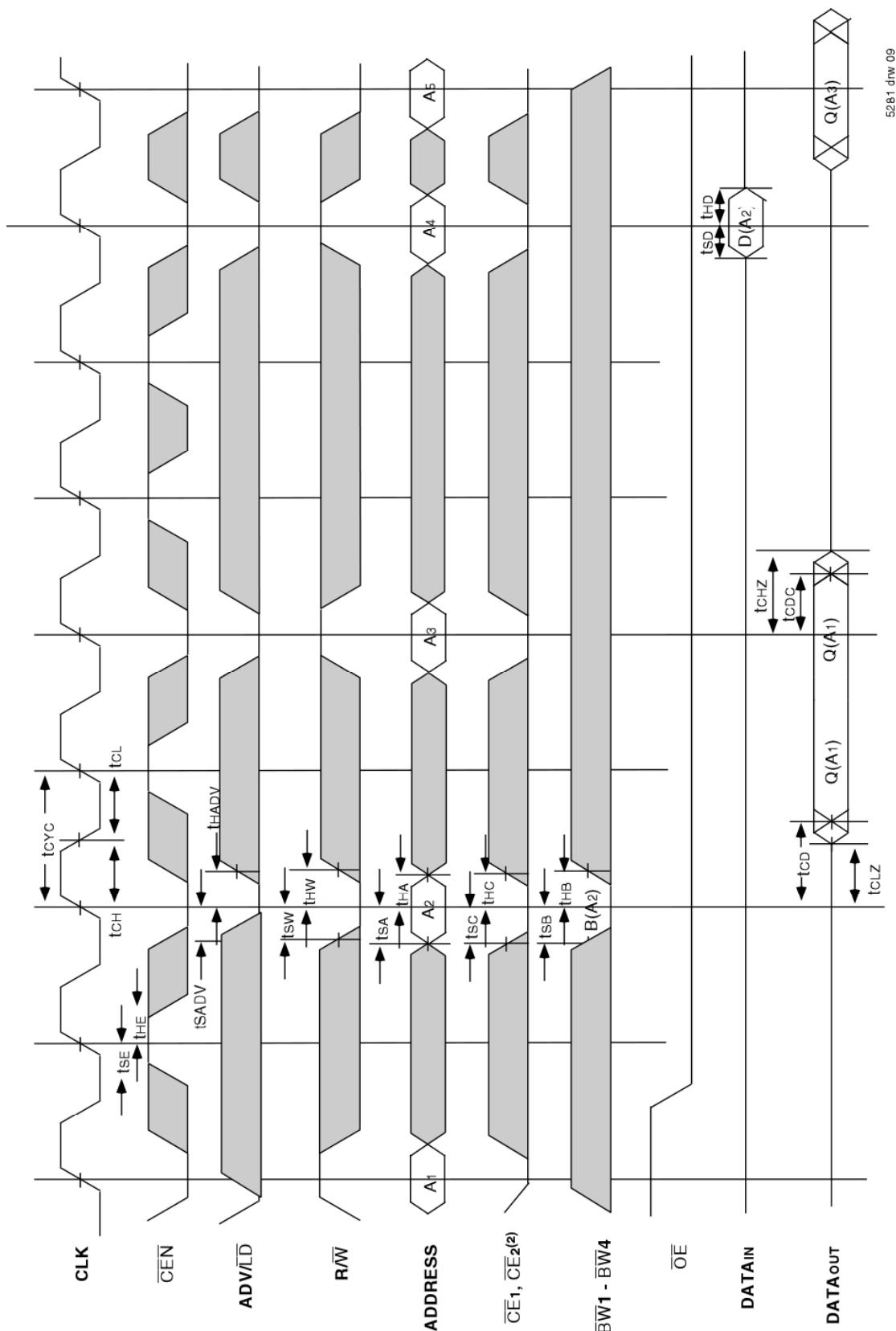
Timing Waveform of Combined Read and Write Cycles ^(1,2,3)



NOTES:

1. Q (A₁) represents the first output from the external address A₁. D (A₂) represents the input data to the SRAM corresponding to address A₂.
2. CE₁ timing transitions are identical but inverted to the $\overline{CE_1}$ and $\overline{CE_2}$ signals. For example, when $\overline{CE_1}$ and $\overline{CE_2}$ are LOW on this waveform, CE₂ is HIGH.
3. Individual Byte Write signals (\overline{BW}_X) must be valid on all write and burst write cycles. A write cycle is initiated when $R\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

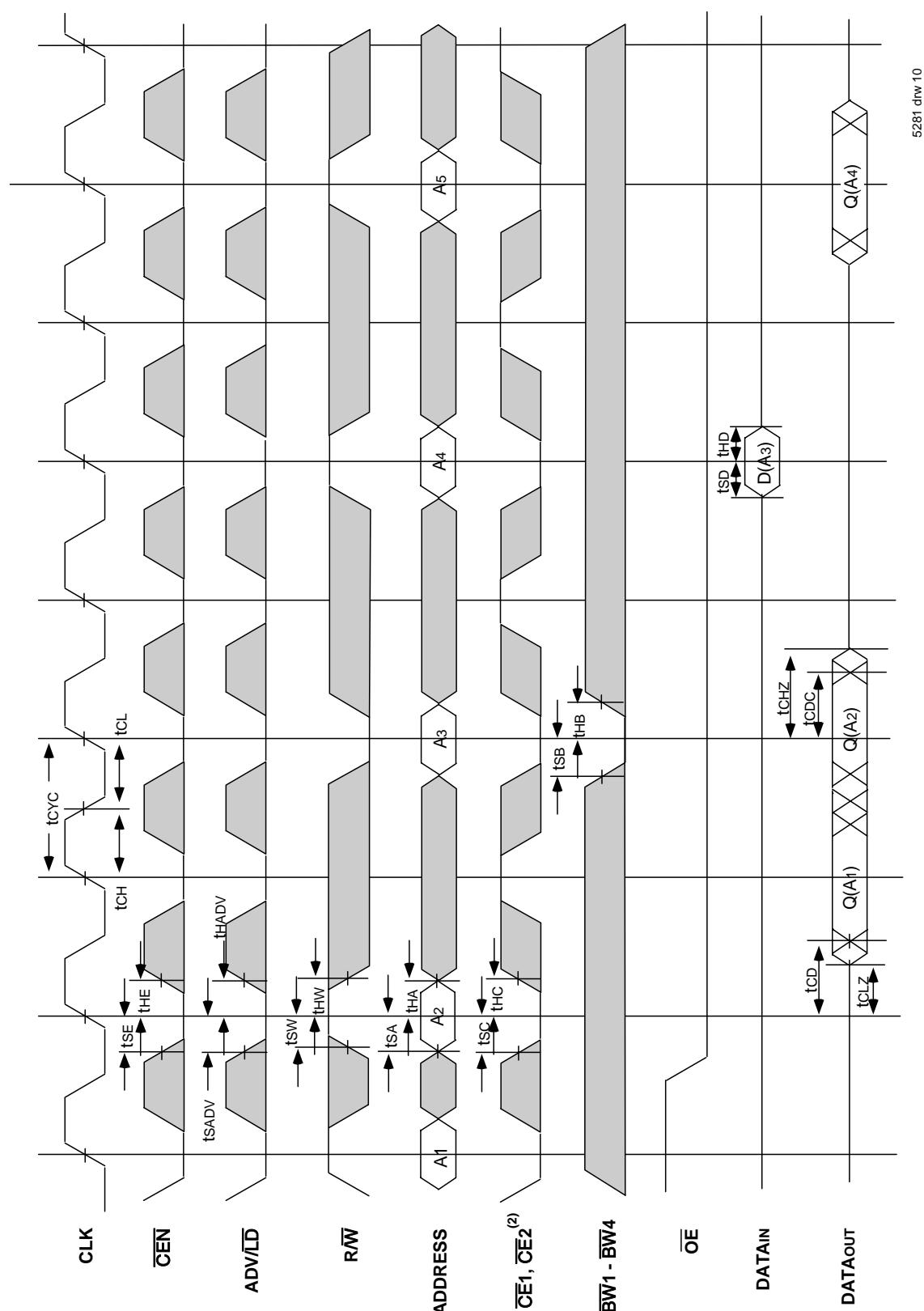
Timing Waveform of **CEN** Operation ^(1,2,3,4)



NOTES:

1. $Q(A_1)$ represents the first output from the external address A_1 . $D(A_2)$ represents the input data to the SRAM corresponding to address A_2 .
2. CE_2 timing transitions are identical but inverted to the \overline{CE}_1 and \overline{CE}_2 signals. For example, when \overline{CE}_1 and \overline{CE}_2 are LOW on this waveform, CE_2 is HIGH.
3. \overline{CEN} when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals (\overline{BW}_i) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

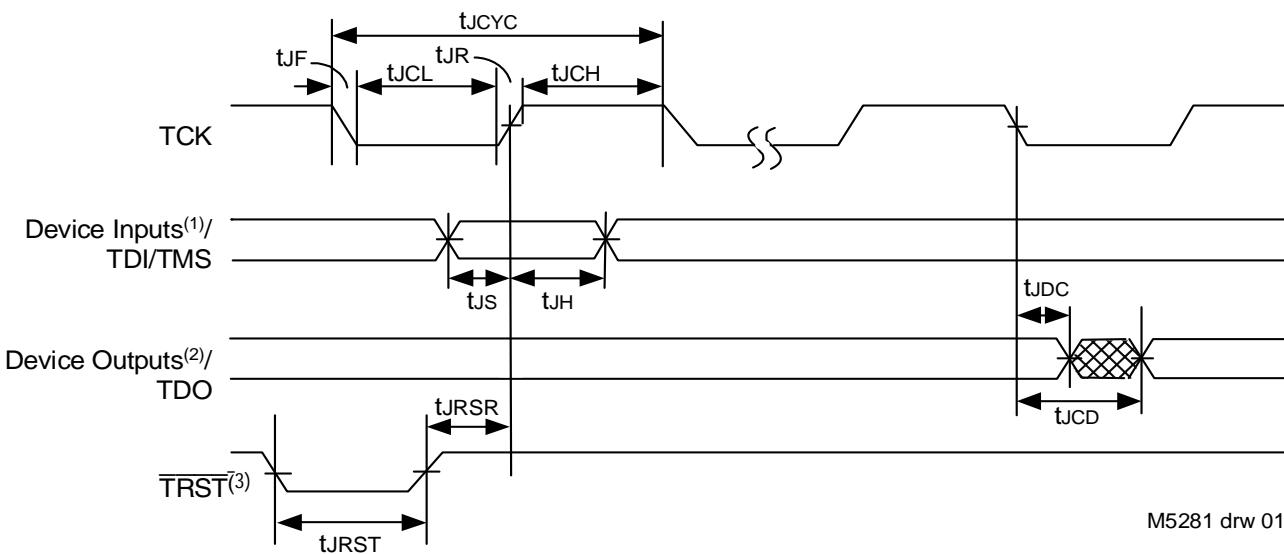
Timing Waveform of **CS** Operation ^(1,2,3,4)



NOTES:

1. Q(A₁) represents the first output from the external address A₁. D(A₃) represents the input data to the SRAM corresponding to address A₃.
2. CE₂ timing transitions are identical but inverted to the \overline{CE}_1 and \overline{CE}_2 signals. For example, when \overline{CE}_1 and \overline{CE}_2 are LOW on this waveform, CE₂ is HIGH.
3. \overline{CEN} when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals (\overline{BW}_X) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

JTAG Interface Specification (SA Version only)



M5281 drw 01

NOTES:

1. Device inputs = All device inputs except TDI, TMS and $\overline{\text{TRST}}$.
2. Device outputs = All device outputs except TDO.
3. During power up, $\overline{\text{TRST}}$ could be driven low or not be used since the JTAG circuit resets automatically. $\overline{\text{TRST}}$ is an optional JTAG reset.

JTAG AC Electrical
Characteristics^(1,2,3,4)

Symbol	Parameter			
		Min.	Max.	Units
t _{JCYC}	JTAG Clock Input Period	100	—	ns
t _{JCH}	JTAG Clock HIGH	40	—	ns
t _{JCL}	JTAG Clock Low	40	—	ns
t _{JR}	JTAG Clock Rise Time	—	5 ⁽¹⁾	ns
t _{JF}	JTAG Clock Fall Time	—	5 ⁽¹⁾	ns
t _{JRST}	JTAG Reset	50	—	ns
t _{JRSR}	JTAG Reset Recovery	50	—	ns
t _{JCD}	JTAG Data Output	—	20	ns
t _{JDC}	JTAG Data Output Hold	0	—	ns
t _{JS}	JTAG Setup	25	—	ns
t _{JH}	JTAG Hold	25	—	ns

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NOTES:

1. Guaranteed by design.
2. AC Test Load (Fig. 1) on external output signals.
3. Refer to AC Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
JTAG Identification (JIDR)	32
Boundary Scan (BSR)	Note (1)

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NOTE:

1. The Boundary Scan Descriptive Language (BSDL) file for this device is available by contacting your local IDT sales representative.

JTAG Identification Register Definitions (SA Version only)

Instruction Field	Value	Description
Revision Number (31:28)	0x2	Reserved for version number.
IDT Device ID (27:12)	0x208, 0x20A	Defines IDT part number 71V3556SA and 71V3558SA, respectively.
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT.
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register.

i5281tbl 02

Available JTAG Instructions

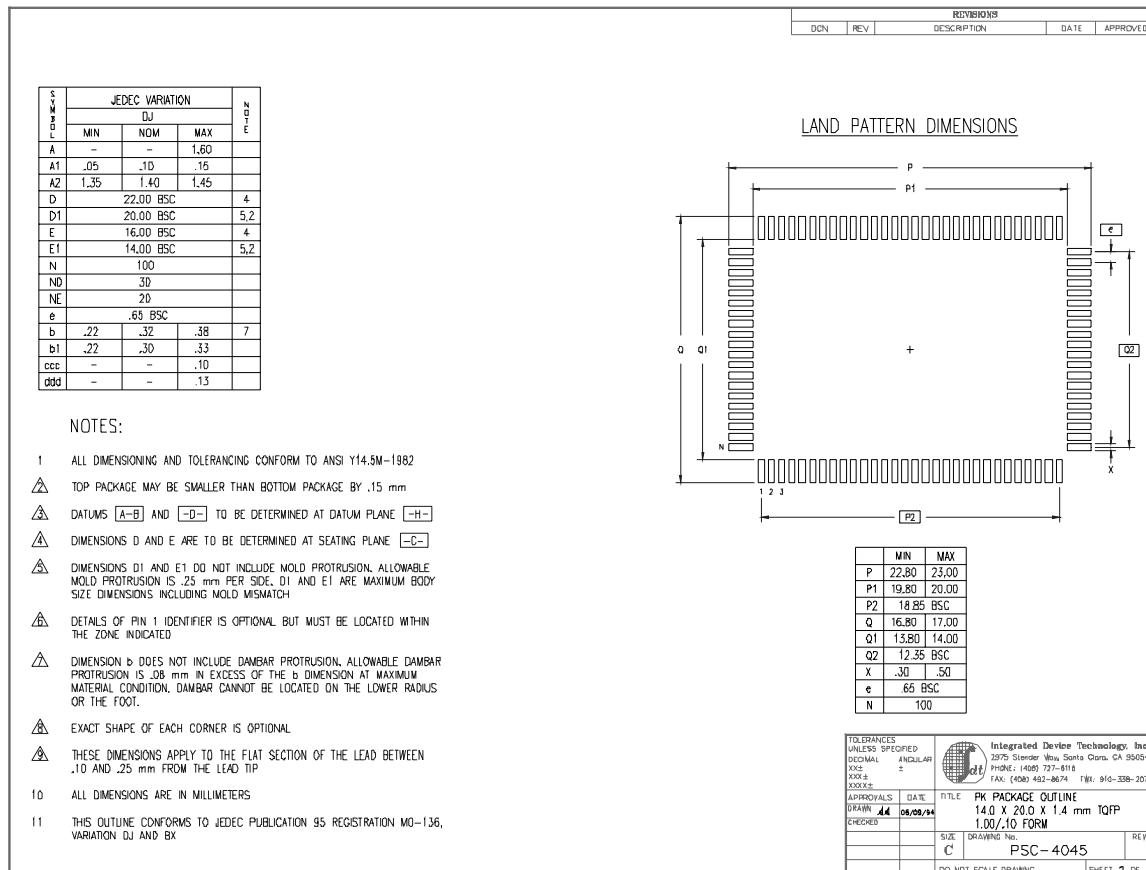
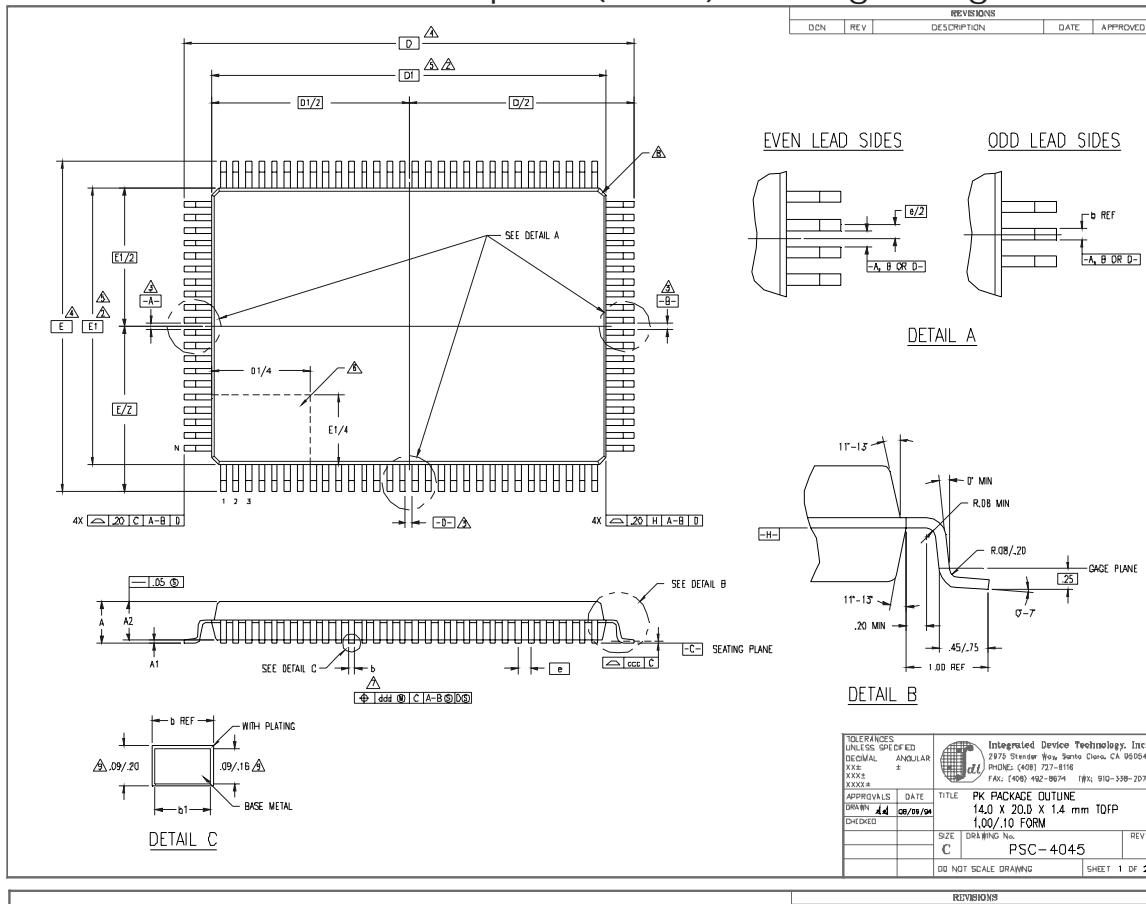
Instruction	Description	OPCODE
EXTEST	Forces contents of the boundary scan cells onto the device outputs ⁽¹⁾ . Places the boundary scan register (BSR) between TDI and TDO.	0000
SAMPLE/PRELOAD	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs ⁽²⁾ and outputs ⁽¹⁾ to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.	0001
DEVICE_ID	Loads the JTAG ID register (JIDR) with the vendor ID code and places the register between TDI and TDO.	0010
HIGHZ	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.	0011
RESERVED	Several combinations are reserved. Do not use codes other than those identified for EXTEST, SAMPLE/PRELOAD, DEVICE_ID, HIGHZ, CLAMP, VALIDATE and BYPASS instructions.	0100
RESERVED		0101
RESERVED		0110
RESERVED		0111
CLAMP	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.	1000
RESERVED	Same as above.	1001
RESERVED		1010
RESERVED		1011
RESERVED		1100
VALIDATE	Automatically loaded into the instruction register whenever the TAP controller passes through the CAPTURE-IR state. The lower two bits '01' are mandated by the IEEE std. 1149.1 specification.	1101
RESERVED	Same as above.	1110
BYPASS	The BYPASS instruction is used to truncate the boundary scan register as a single bit in length.	1111

i5281tbl 04

NOTES:

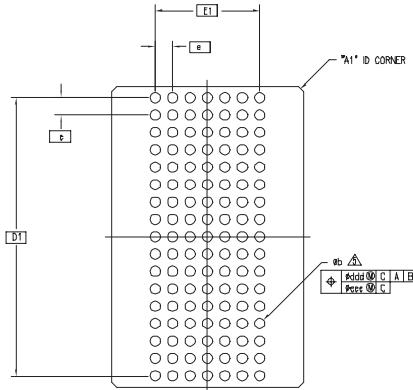
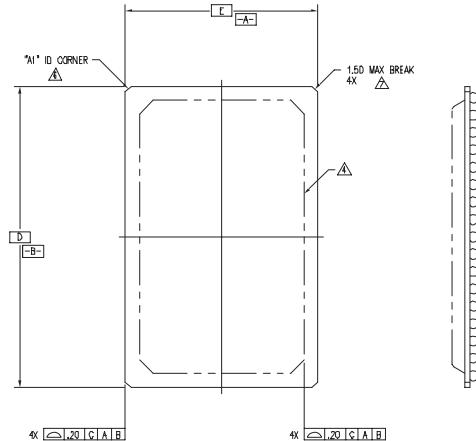
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{\text{TRST}}$.

100-Pin Plastic Thin Quad Flatpack (TQFP) Package Diagram Outline

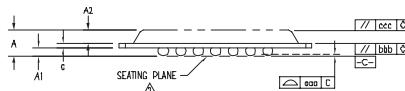


119 Ball Grid Array (BGA) Package Diagram Outline

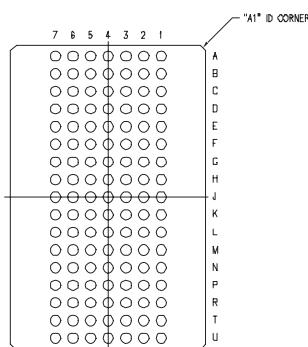
REVISIONS				
DOC	REV	DESCRIPTION	DATE	APPROVED
60626	00	INITIAL RELEASE	10/15/97	T. VU
	01	SWITCH E & D DIMENSIONS	04/25/00	



(119 BALL SHOWN)



TOLERANCES UNLESS SPECIFIED		 Integrated Device Technology, Inc. 2870 Sherwood Way, Santa Clara, CA 95051 (408) 727-2110 FAX: (408) 492-5774 TWX: 910-358-2074	
DECIMAL	ANGULAR		
X±X	±		
XX±XX	XX±XX		
APPROVALS		DATE	TITLE
DRAWN	70	10/19/01	BG PACKAGE OUTLINE
CHECKED			14.0 X 22.0 mm BODY
			PQCA
SIZE		DRAWING No.	REV.
C		PSC-4063	01
DO NOT SCALE DRAWING			
SHEET 1 OF 1			



{119 BALL}

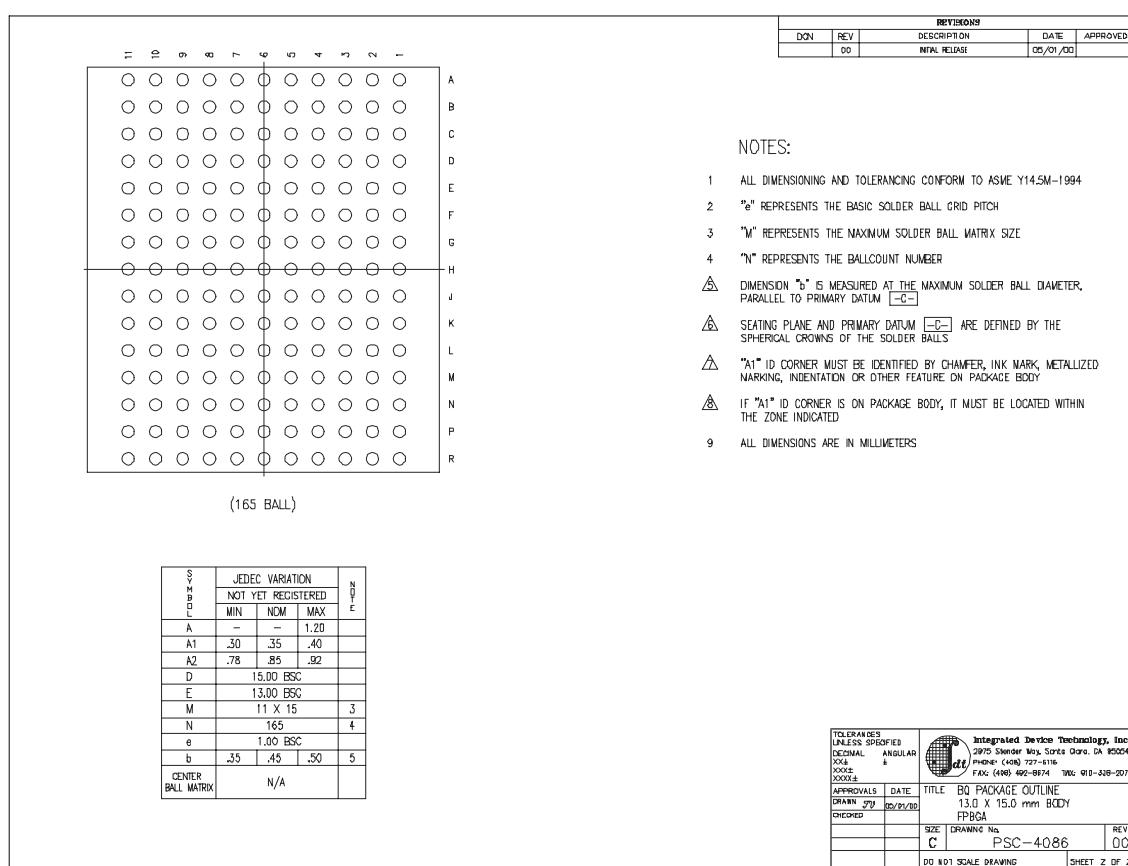
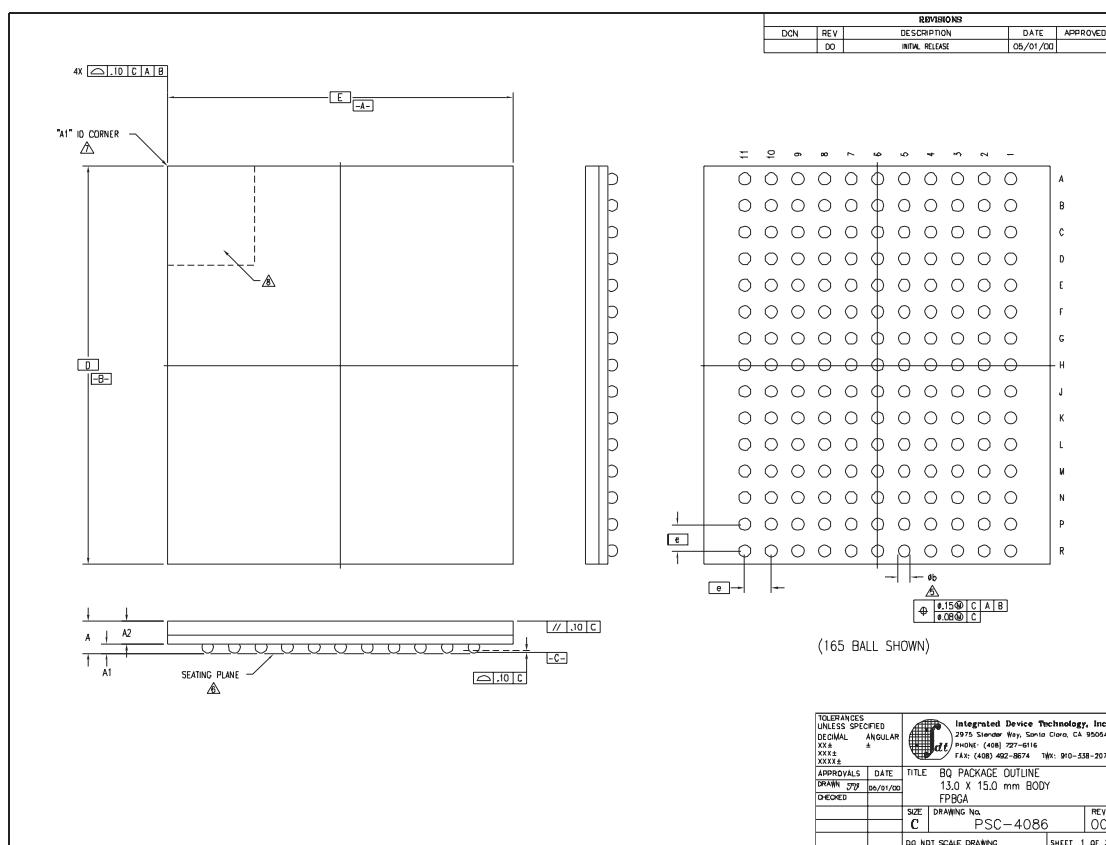
SYMBOL	JEDEC VARIATION		
	AA	MIN	NOM
		NOM	MAX
A	—	.215	.236
A1	.50	.60	.70
A2	—	—	1.20
D	22.00	BSC	
D1	20.32	BSC	
E	14.00	BSC	
E1	7.62	BSC	
MD	17		3
ME	7		3
N	119		3
e	1.27	BSC	
b	.60	.75	.90
c	.51	.56	.61
aaa	—	—	.15
bbb	—	—	.25
ccc	—	—	.35
ddd	—	—	.30
		—	—

NOTES:

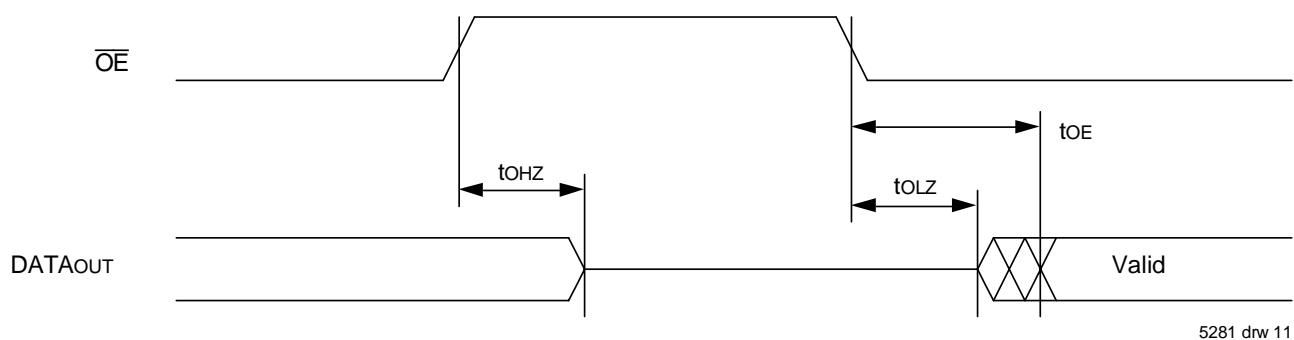
- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- 2 **SEATING PLANE AND PRIMARY DATUM** **[C]** **ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS**
- 3 **"MD"** **IS THE BALL MATRIX SIZE IN THE "D" DIRECTION**
"ME" **IS THE BALL MATRIX SIZE IN THE "E" DIRECTION**
"N" **IS THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS**
- 4 **PACKAGE MAY EXTEND TO EDGE PERIPHERY AND MAY CONSIST OF MOLDING COMPOUND, EPOXY, METAL, CERAMIC OR OTHER MATERIAL**
- 5 **DIMENSION "B" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM** **[C]**
- 6 **"A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY. MARK MUST BE VISIBLE FROM TOP SURFACE**
- 7 **ACTUAL SHAPE OF THIS FEATURE IS OPTIONAL**
- 8 **ALL DIMENSIONS ARE IN MILLIMETERS**
- 9 **THIS DRAWING CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-028, VARIATION AA**

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.		
DECIMAL	ANGULAR	2900 Technology Way, Santa Clara, CA 95051		
MM	DEGREES	TEL: (408) 927-2000		
XXXX	XXXX	FAX: (408) 927-0674		
APPROVALS		TOLL FREE: 1-800-347-2077		
DRAWN SP9	RE- SP9	TITLE: B5 PACKAGE OUTLINE		
CHECKED		14.0 X 22.0 mm BODY		
		PCPA		
SIZE	DRAWING NO.	REV.		
C	PSC-4063	D2		
DO NOT SCALE DRAWING				
SHEET 2 OF 2				

165 Fine Pitch Ball Grid Array (fBGA) Package Diagram Outline



Timing Waveform of **OE** Operation ⁽¹⁾



NOTE:

1. A read operation is assumed to be in progress.

Ordering Information

XXXX	X	XX	XX	XX	X	X
Device Type	Power	Speed	Package	Process/Temperature Range	Temperature Range	
					Blank	Commercial (0°C to +70°C) Industrial (-40°C to +85°C)
				G		Restricted Hazardous Substance Device
				PF** BG BQ		100-pin Plastic Thin Quad Flatpack (TQFP) 119 Ball Grid Array (BGA) 165 Fine Pitch Ball Grid Array (fBGA)
				200* 166 133 100		Clock Frequency in Megahertz
				S SA		Standard Power Standard Power with JTAG interface
				X		X Generation Die Step Optional
				IDT71V3556 IDT71V3558		128Kx36 Pipelined ZBT SRAM with 3.3V I/O 256Kx18 Pipelined ZBT SRAM with 3.3V I/O

5281 dw 12

* Commercial temperature range only. Only available in 256K x 18 configuration.
** JTAG (SA Version) is not available with 100-pin TQFP package

Datasheet Document History

6/30/99		Updated to new format
8/23/99		Added Smart ZBT functionality
	Pg. 4, 5	Added Note 4 and changed Pins 38, 42, and 43 to DNU
	Pg. 6	Changed U2-U6 to DNU
	Pg. 14	Added Smart ZBT AC Electrical Characteristics
	Pg. 15	Improved tCD and tOE(MAX) at 166MHz Revised tCHZ(MIN) for f ≤ 133 MHz Revised tOHZ (MAX) for f ≤ 133 MHz Improved tCH, tCL for f ≤ 166 MHz Improved setup times for 100–200 MHz
	Pg. 22	Added BGA package diagrams
	Pg. 24	Added Datasheet Document History
10/4/99	Pg. 14	Revised AC Electrical Characteristics table
12/31/99	Pg. 15	Revised tCHZ to match tCL and tCD at 133MHz and 100MHz Removed Smart functionality
04/30/00	Pg. 5, 6	Added Industrial Temperature range offerings at the 100 to 166MHz speed grades. Insert clarification note to Recommended Operating Temperature and Absolute Max Ratings tables
	Pg. 6	Add BGA capacitance table
	Pg. 5, 6, 7	Add note to TQFP and BGA Pin Configurations; corrected typo in pinout
05/26/00	Pg. 21	Add 100pinTQFP package Diagram Outline
07/26/00	Pg. 23	Add new package offering, 13 x 15mm 165 fBGA
	Pg. 5-8	Correct 119BGA Package Diagram Outline
	Pg. 8	Add ZZ sleep mode reference note to BG119, PK100 and BO165 pinouts
	Pg. 23	Update BO165 pinout
10/25/00		Update BG119 package diagram outline dimensions
	Pg. 8	Remove Preliminary status
1/24/02	Pg. 1-8, 15,22,23,27	Add note to pin N5 on BO165, reserved for JTAG \overline{TRST}
9/30/04	Pg. 7	Added JTAG "SA" version functionality
	Pg. 27	Updated pin configuration for the 119 BGA-reordered I/O signals on P6, P7 (128K x 36) and P7, N6, L6, K7, H6, G7, F6, E7, D6 (256K x 18).
10/18/06	Pg. 1, 26	Adding "Restricted hazardous substance device" to ordering information.
08/11/08	Pg. 1, 15, 16, 27	Added X generation die step to data sheet.
10/14/10	Pg. 28	Remove 200MHz on 128K x 36 configuration. Removed IDT from the ordering information



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