

*RoHS Compliant*

*Value Added* **Compact Flash Series III**  
*Specification for Industrial CF*

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*Version 1.0*



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## Features:

- **Compact Flash Association Specification Revision 3.0 Standard Interface**
  - ATA command set compatible
  - ATA mode support for up to:
    - PIO Mode-6
    - Multiword DMA Mode-4
    - Ultra DMA Mode-4
- **Connector Type**
  - 50 pins female
- **Low power consumption (typical)**
  - Supply voltage: 3.3V & 5V
  - Active mode: 80 mA/95 mA (3.3V/5.0V)
  - Sleep mode: 700  $\mu$ A/900  $\mu$ A (3.3V/5.0V)
- **Performance\*\***
  - Sustained read: 30 MB/sec
  - Sustained write:
    - Standard: 5 MB/sec
    - High Speed: 15 MB/sec
- **Capacity**
  - Standard:
    - 128, 256, 512 MB
    - 1, 2, 16 GB
  - High Speed:
    - 256, 512 MB
    - 1, 2, 4, 8 GB
- **NAND Flash Type: SLC**
- **Temperature ranges**
  - Operation:
    - Standard: 0°C to 70°C
    - ET\*: -40°C to 85°C
  - Storage: -40°C to 100°C
- **Flash management**
  - Intelligent endurance design
    - Advanced wear-leveling algorithms*
    - S.M.A.R.T. Technology*
    - Built-in Hardware ECC*
    - Enhanced Data Integrity*
  - Intelligent power failure recovery
- **RoHS compliant**

\*Extended Temperature

\*\*Performance varies with flash configurations

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## Table of Contents

|                                                                           |           |
|---------------------------------------------------------------------------|-----------|
| <b>1. GENERAL DESCRIPTION .....</b>                                       | <b>3</b>  |
| 1.1 PERFORMANCE-OPTIMIZED CONTROLLER .....                                | 3         |
| 1.1.1 Power Management Unit (PMU) .....                                   | 3         |
| 1.1.2 SRAM Buffer .....                                                   | 3         |
| <b>2. FUNCTIONAL BLOCK .....</b>                                          | <b>4</b>  |
| <b>3. PIN ASSIGNMENTS .....</b>                                           | <b>5</b>  |
| <b>4. CAPACITY SPECIFICATION .....</b>                                    | <b>7</b>  |
| 4.1 PERFORMANCE SPECIFICATION .....                                       | 7         |
| 4.2 ENVIRONMENTAL SPECIFICATIONS .....                                    | 8         |
| <b>5. FLASH MANAGEMENT .....</b>                                          | <b>9</b>  |
| 5.1 INTELLIGENT ENDURANCE DESIGN .....                                    | 9         |
| 5.1.1 Advanced wear-leveling algorithms .....                             | 9         |
| 5.1.2 S.M.A.R.T. technology .....                                         | 9         |
| 5.1.3 Built-in hardware ECC .....                                         | 9         |
| 5.1.4 Enhanced data integrity .....                                       | 9         |
| 5.2 INTELLIGENT POWER FAILURE RECOVERY .....                              | 10        |
| <b>6. SOFTWARE INTERFACE .....</b>                                        | <b>11</b> |
| 6.1 COMMAND SET .....                                                     | 11        |
| <b>7. ELECTRICAL SPECIFICATION .....</b>                                  | <b>13</b> |
| 7.1 DC CHARACTERISTICS .....                                              | 14        |
| 7.2 AC CHARACTERISTICS .....                                              | 15        |
| 7.2.1 Attribute Memory Read Timing Specification .....                    | 16        |
| 7.2.2 Configuration Register (Attribute Memory) Write Specification ..... | 17        |
| 7.2.3 Common Memory Read Timing Specification .....                       | 18        |
| 7.2.4 Common Memory Write Timing Specification .....                      | 19        |
| 7.2.5 I/O Input (Read) Timing Specification .....                         | 20        |
| 7.2.6 I/O Output (Write) Timing Specification .....                       | 21        |
| 7.2.7 Ultra DMA Mode Data Transfer Input/Output (Read/Write) Timing ..... | 22        |
| 7.2.8 Media Side Interface I/O Timing Specifications .....                | 34        |
| <b>8. PHYSICAL CHARACTERISTICS .....</b>                                  | <b>37</b> |
| 8.1 DIMENSION .....                                                       | 37        |
| <b>9. PRODUCT ORDERING INFORMATION .....</b>                              | <b>38</b> |
| 9.1 PRODUCT CODE DESIGNATIONS .....                                       | 38        |
| 9.2 VALID COMBINATIONS .....                                              | 39        |

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## **1. General Description**

Apacer's Industrial Compact Flash Card (CFC) offers the most reliable and high performance storage which is compatible with CF Type I and Type II device. Unlike the ordinary consumer Compact Flash cards, Apacer Industrial Compact Flash card provides solid traceability to ensure all products HW/SW are the same as you qualified.

Apacer's CFC provides complete PCMCIA - ATA functionality and compatibility. Apacer's Compact Flash technology is designed for use in Point of Sale (POS) terminals, telecom, IP-STB, medical instruments, surveillance systems, industrial PCs and handheld applications.

Featuring technologies as Advanced Wear-leveling algorithms, S.M.A.R.T, Enhanced Data Integrity, Built-in Hardware ECC, and Intelligent Power Failure Recovery, Apacer's Industrial Compact Flash Card assures users of a versatile device on data storage.

### **1.1 Performance-Optimized Controller**

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The Compact Flash Card Controller translates standard CF signals into flash media data and control signals.

#### **1.1.1 Power Management Unit (PMU)**

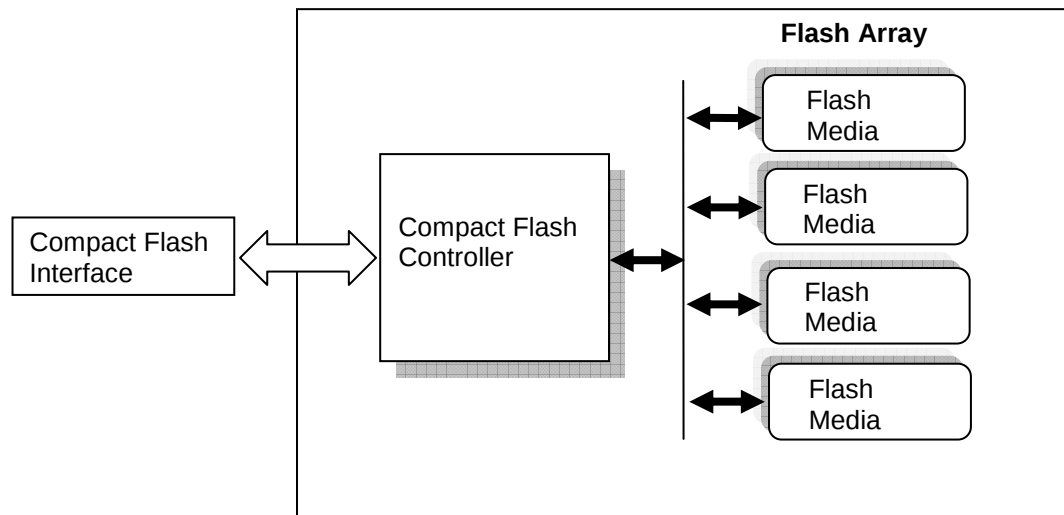
The power management unit (PMU) controls the power consumption of the Compact Flash card controller. It reduces the power consumption of the Compact Flash Card Controller by putting circuitry not in operation into sleep mode. The PMU has zero wake-up latency.

#### **1.1.2 SRAM Buffer**

The Compact Flash Card Controller performs as an SRAM buffer to optimize the host's data transfer to and from the flash media.

## 2. Functional Block

The Compact Flash Card (CFC) includes a controller and flash media, as well as the Compact Flash standard interface. Figure 2-1 shows the functional block diagram.



**Figure 2-1:** Functional block diagram

## 3. Pin Assignments

Table 3-1 lists the pin assignments with respective signal names for the 50-pin configuration. A “#” suffix indicates the active low signal. The pin type can be input, output or input/output.

**Table 3-1:** Pin assignments (1 of 2)

| Pin No. | Memory card mode |              | I/O card mode |              | True IDE mode    |              |
|---------|------------------|--------------|---------------|--------------|------------------|--------------|
|         | Signal name      | Pin I/O type | Signal name   | Pin I/O type | Signal name      | Pin I/O type |
| 1       | GND              | -            | GND           | -            | GND              | -            |
| 2       | D3               | I/O          | D3            | I/O          | D3               | I/O          |
| 3       | D4               | I/O          | D4            | I/O          | D4               | I/O          |
| 4       | D5               | I/O          | D5            | I/O          | D5               | I/O          |
| 5       | D6               | I/O          | D6            | I/O          | D6               | I/O          |
| 6       | D7               | I/O          | D7            | I/O          | D7               | I/O          |
| 7       | #CE1             | I            | #CE1          | I            | #CS0             | I            |
| 8       | A10              | I            | A10           | I            | A10 <sup>1</sup> | I            |
| 9       | #OE              | I            | #OE           | I            | #ATA SEL         | I            |
| 10      | A9               | I            | A9            | I            | A9 <sup>1</sup>  | I            |
| 11      | A8               | I            | A8            | I            | A8 <sup>1</sup>  | I            |
| 12      | A7               | I            | A7            | I            | A7 <sup>1</sup>  | I            |
| 13      | VCC              | -            | VCC           | -            | VCC              | -            |
| 14      | A6               | I            | A6            | I            | A6 <sup>1</sup>  | I            |
| 15      | A5               | I            | A5            | I            | A5 <sup>1</sup>  | I            |
| 16      | A4               | I            | A4            | I            | A4 <sup>1</sup>  | I            |
| 17      | A3               | I            | A3            | I            | A3 <sup>1</sup>  | I            |
| 18      | A2               | I            | A2            | I            | A2               | I            |
| 19      | A1               | I            | A1            | I            | A1               | I            |
| 20      | A0               | I            | A0            | I            | A0               | I            |
| 21      | D0               | I/O          | D0            | I/O          | D0               | I/O          |
| 22      | D1               | I/O          | D1            | I/O          | D1               | I/O          |
| 23      | D2               | I/O          | D2            | I/O          | D2               | I/O          |
| 24      | WP               | O            | #IOIS16       | O            | #IOCS16          | O            |
| 25      | #CD2             | O            | #CD2          | O            | #CD2             | O            |
| 26      | #CD1             | O            | #CD1          | O            | #CD1             | O            |
| 27      | D11              | I/O          | D11           | I/O          | D11              | I/O          |
| 28      | D12              | I/O          | D12           | I/O          | D12              | I/O          |
| 29      | D13              | I/O          | D13           | I/O          | D13              | I/O          |
| 30      | D14              | I/O          | D14           | I/O          | D14              | I/O          |
| 31      | D15              | I/O          | D15           | I/O          | D15              | I/O          |
| 32      | #CE2             | I            | #CE2          | I            | #CS1             | I            |
| 33      | #VS1             | O            | #VS1          | O            | #VS1             | O            |
| 34      | #IORD            | I            | #IORD         | I            | #IORD            | I            |
| 35      | #IOWR            | I            | #IOWR         | I            | #IOWR            | I            |
| 36      | #WE              | I            | #WE           | I            | #WE              | I            |
| 37      | RDY/-BSY         | O            | #IREQ         | O            | INTRQ            | O            |
| 38      | VCC              | -            | VCC           | -            | VCC              | -            |
| 39      | #CSEL            | I            | #CSEL         | I            | #CSEL            | I            |
| 40      | #VS2             | O            | #VS2          | O            | #VS2             | O            |
| 41      | RESET            | I            | RESET         | I            | #RESET           | I            |

**Value Added Compact Flash III series**  
**AP-CFxxxxxE3XR-XXXXXXK**



**Table 3-1:** Pin assignments (2 of 2)

| Pin No. | Memory card mode |              | I/O card mode |              | True IDE mode      |              |
|---------|------------------|--------------|---------------|--------------|--------------------|--------------|
|         | Signal name      | Pin I/O type | Signal name   | Pin I/O type | Signal name        | Pin I/O type |
| 42      | #WAIT            | O            | #WAIT         | O            | IORDY              | O            |
| 43      | #INPACK          | O            | #INPACK       | O            | DMARQ <sup>2</sup> | O            |
| 44      | #REG             | I            | #REG          | I            | DMACK <sup>2</sup> | I            |
| 45      | BVD2             | O            | #SPKR         | O            | #DASP              | O            |
| 46      | BVD1             | O            | #STSCHG       | O            | #PDIAG             | O            |
| 47      | D8               | I/O          | D8            | I/O          | D8                 | I/O          |
| 48      | D9               | I/O          | D9            | I/O          | D9                 | I/O          |
| 49      | D10              | I/O          | D10           | I/O          | D10                | I/O          |
| 50      | GND              | -            | GND           | -            | GND                | -            |

1. The signal should be grounded by the host.

2. Connection required when UDMA is in use.

## 4. Capacity Specification

Capacity specification of the Compact Flash Card series (CFC) is available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

**Table 4-1:** Capacity specifications

| Capacity | Total bytes*   | Cylinders | Heads | Sectors | Max LBA    |
|----------|----------------|-----------|-------|---------|------------|
| 128 MB   | 128,450,560    | 980       | 8     | 32      | 250,880    |
| 256 MB   | 256,901,120    | 980       | 16    | 32      | 501,760    |
| 512 MB   | 512,483,328    | 993       | 16    | 63      | 1,000,944  |
| 1GB      | 1,024,966,656  | 1,986     | 16    | 63      | 2,001,888  |
| 2GB      | 2,048,901,120  | 3,970     | 16    | 63      | 4,001,760  |
| 4GB      | 4,110,188,544  | 7,964     | 16    | 63      | 8,027,712  |
| 8GB      | 8,195,604,480  | 15,880    | 16    | 63      | 16,007,040 |
| 16GB     | 16,391,208,960 | 16,383**  | 16    | 63      | 32,014,080 |

\*Display of total bytes varies from file systems.

\*\*Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies

### 4.1 Performance Specification

Performances of the Standard and High Speed ATA-Flash Disk are listed in Table 4-2 and Table 4-3.

**Table 4-2:** Standard Performance specifications

| Capacity               | 128 MB / 256 MB<br>512 MB / 1 GB | 2 GB | 16 GB |
|------------------------|----------------------------------|------|-------|
| Performance            |                                  |      |       |
| Sustained read (MB/s)  | 15                               | 20   | 20    |
| Sustained write (MB/s) | 5                                | 5    | 5     |

**Table 4-3:** High Speed Performance specifications

| Capacity               | 256 MB | 512 MB | 1 GB | 2 GB | 4 GB | 8 GB |
|------------------------|--------|--------|------|------|------|------|
| Performance            |        |        |      |      |      |      |
| Sustained read (MB/s)  | 25     | 25     | 25   | 25   | 30   | 30   |
| Sustained write (MB/s) | 5      | 5      | 5    | 5    | 10   | 15   |

Note: Performance varies from flash configurations.

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## 4.2 Environmental Specifications

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Environmental specification of the Compact Flash Card series (CFC) which follows the MIL-STD-810F standards is available as shown in Table 4-4.

**Table 4-4:** Environmental specifications

| Environment               |           | Specification                                                        |
|---------------------------|-----------|----------------------------------------------------------------------|
| Temperature               | Operation | 0℃ to 70 ℃ (Standard) ; -40℃ to 85 ℃ (Extended Temperature)          |
|                           | Storage   | -40℃ to 100℃                                                         |
| Humidity                  |           | 5% to 95% RH (Non-condensing)                                        |
| Vibration (Non-Operation) |           | Sine wave: 10~2000Hz, 15G (X, Y, Z axes)                             |
| Shock (Non-Operation)     |           | Half sine wave, Peak acceleration 50 G, 11 ms (X, Y, Z ; All 6 axes) |

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## **5. Flash Management**

### **5.1 Intelligent Endurance Design**

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#### **5.1.1 Advanced wear-leveling algorithms**

The NAND flash devices are limited by a certain number of write cycles. When using a file system, frequent file table updates is mandatory. If some area on the flash wears out faster than others, it would significantly reduce the lifetime of the whole device, even if the erase counts of others are far from the write cycle limit. Thus, if the write cycles can be distributed evenly across the media, the lifetime of the media can be prolonged significantly. The scheme is achieved both via buffer management and Apacer-specific advanced wear leveling to ensure that the lifetime of the flash media can be increased, and the disk access performance is optimized as well.

#### **5.1.2 S.M.A.R.T. technology**

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure. Apacer SMART feature adopts the standard SMART command B0h to read data from the drive. When the Apacer SMART Utility running on the host, it analyzes and reports the disk status to the host before the device is in critical condition.

#### **5.1.3 Built-in hardware ECC**

The ATA-Disk Module uses BCH Error Detection Code (EDC) and Error Correction Code (ECC) algorithms which correct up to eight random single-bit errors for each 512-byte block of data. High performance is fulfilled through hardware-based error detection and correction.

#### **5.1.4 Enhanced data integrity**

The properties of NAND flash memory make it ideal for applications that require high integrity while operating in challenging environments. The integrity of data to NAND flash memory is generally maintained through ECC algorithms and bad block management. Flash controllers can support up to 8 bits ECC capability for accuracy of data transactions, and bad block management is a preventive mechanism from loss of data by retiring unusable media blocks and relocating the data to the other blocks, along with the integration of advanced wear leveling algorithms, so that the lifespan of device can be expanded.

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## **5.2 Intelligent Power Failure Recovery**

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The Low Power Detection on the controller initiates cached data saving before the power supply to the device is too low. This feature prevents the device from crash and ensures data integrity during an unexpected blackout. Once power was failure before cached data writing back into flash, data in the cache will lost. The next time the power is on, the controller will check these fragmented data segment, and, if necessary, replace them with old data kept in flash until programmed successfully.

## 6. Software Interface

### 6.1 Command Set

Table 6-1 summarizes the command set with the paragraphs that follow describing the individual commands and the task file for each.

**Table 6-1:** Command set (1 of 2)

| Command                     | Code       | FR <sup>1</sup> | SC <sup>2</sup> | SN <sup>3</sup> | CY <sup>4</sup> | DH <sup>5</sup> | LBA <sup>6</sup> |
|-----------------------------|------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|
| Check-Power-Mode            | E5H or 98H | -               | -               | -               | -               | D <sup>8</sup>  | -                |
| Execute-Drive-Diagnostic    | 90H        | -               | -               | -               | -               | D               | -                |
| Erase Sector(s)             | C0H        | -               | Y               | Y               | Y               | Y               | Y                |
| Flush-Cache                 | E7H        | -               | -               | -               | -               | D               | -                |
| Format Track                | 50H        | -               | Y <sup>7</sup>  | -               | Y               | Y <sup>8</sup>  | Y                |
| Identify-Drive              | ECH        | -               | -               | -               | -               | D               | -                |
| Idle                        | E3H or 97H | -               | Y               | -               | -               | D               | -                |
| Idle-Immediate              | E1H or 95H | -               | -               | -               | -               | D               | -                |
| Initialize-Drive-Parameters | 91H        | -               | Y               | -               | -               | Y               | -                |
| NOP                         | 00H        | -               | -               | -               | -               | D               | -                |
| Read-Buffer                 | E4H        | -               | -               | -               | -               | D               | -                |
| Read-DMA                    | C8H or C9H | -               | Y               | Y               | Y               | Y               | Y                |
| Read-Multiple               | C4H        | -               | Y               | Y               | Y               | Y               | Y                |
| Read-Sector(s)              | 20H or 21H | -               | Y               | Y               | Y               | Y               | Y                |
| Read-Verify-Sector(s)       | 40H or 41H | -               | Y               | Y               | Y               | Y               | Y                |
| Recalibrate                 | 1XH        | -               | -               | -               | -               | D               | -                |
| Request-Sense               | 03H        | -               | -               | -               | -               | D               | -                |
| Seek                        | 7XH        | -               | -               | Y               | Y               | Y               | Y                |
| Set-Features                | EFH        | Y <sup>7</sup>  | -               | -               | -               | D               | -                |

**Value Added Compact Flash III series**  
**AP-CFxxxxxE3XR-XXXXXXK**



**Table 6-1:** Command set (2 of 2)

| Command                      | Code       | FR <sup>1</sup> | SC <sup>2</sup> | SN <sup>3</sup> | CY <sup>4</sup> | DH <sup>5</sup> | LBA <sup>6</sup> |
|------------------------------|------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|
| SMART                        | B0H        | Y               | Y               | Y               | Y               | D               |                  |
| Set-Multiple-Mode            | C6H        | -               | Y               | -               | -               | D               | -                |
| Set-Sleep-Mode               | E6H or 99H | -               | -               | -               | -               | D               | -                |
| Standby                      | E2H or 96H | -               | -               | -               | -               | D               | -                |
| Standby-Immediate            | E0H or 94H | -               | -               | -               | -               | D               | -                |
| Translate-Sector             | 87H        | -               | Y               | Y               | Y               | Y               | Y                |
| Write-Buffer                 | E8H        | -               | -               | -               | -               | D               | -                |
| Write-DMA                    | CAH or CBH | -               | Y               | Y               | Y               | Y               | Y                |
| Write-Multiple               | C5H        | -               | Y               | Y               | Y               | Y               | Y                |
| Write-Multiple-Without-Erase | CDH        | -               | Y               | Y               | Y               | Y               | Y                |
| Write-Sector(s)              | 30H or 31H | -               | Y               | Y               | Y               | Y               | Y                |
| Write-Sector-Without-Erase   | 38H        | -               | Y               | Y               | Y               | Y               | Y                |
| Write-Verify                 | 3CH        | -               | Y               | Y               | Y               | Y               | Y                |

1. FR - Features register

2. SC - Sector Count register

3. SN - Sector Number register

4. CY - Cylinder registers

5. DH - Drive/Head register

6. LBA - Logical Block Address mode supported (see command descriptions for use)

7. Y - The register contains a valid parameter for this command

8. For the Drive/Head register:

Y means both the CFC and Head parameters are used

D means only the CFC parameter is valid and not the Head parameter

## 7. Electrical Specification

**Caution: Absolute Maximum Stress Ratings** – Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

**Table 7-1:** Operating range

| Range                | Ambient Temperature | 3.3V         | 5V         |
|----------------------|---------------------|--------------|------------|
| Standard             | 0°C to +70°C        | 3.135-3.465V | 4.75-5.25V |
| Extended Temperature | -40°C to +85°C      |              |            |

**Table 7-2:** Absolute maximum power pin stress ratings

| Parameter                                                     | Symbol          | Conditions                                |
|---------------------------------------------------------------|-----------------|-------------------------------------------|
| Input Power                                                   | V <sub>DD</sub> | -0.3V min. to 6.5V max.                   |
| Voltage on any pin except V <sub>DD</sub> with respect to GND | V               | -0.5V min. to V <sub>DD</sub> + 0.5V max. |

**Table 7-3:** Recommended system power-up timing

| Symbol                             | Parameter                   | Typical | Maximum | Units |
|------------------------------------|-----------------------------|---------|---------|-------|
| T <sub>PU-READY</sub> <sup>1</sup> | Power-up to Ready Operation | 200     | 1000    | ms    |
| T <sub>PU-WRITE</sub> <sup>1</sup> | Power-up to Write Operation | 200     | 1000    | ms    |

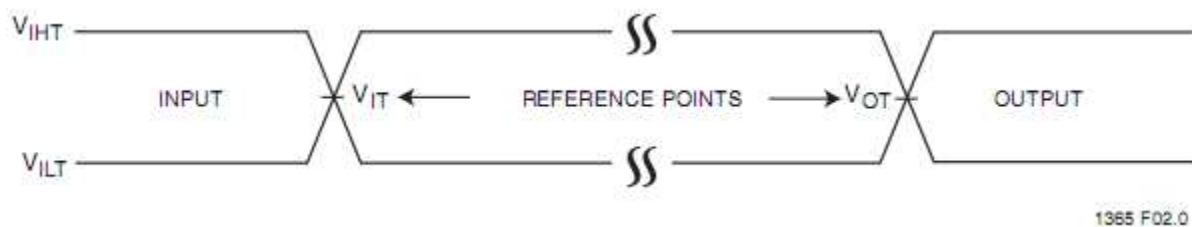
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

## 7.1 DC Characteristics

**Table 7-4: DC Characteristics**

| Symbol                 | Type | Parameter                                                                     | Min  | Max  | Units   | Conditions                                                        |
|------------------------|------|-------------------------------------------------------------------------------|------|------|---------|-------------------------------------------------------------------|
| $V_{IH1}$<br>$V_{IL1}$ | I1   | Input Voltage                                                                 | 2.0V | 0.8V | V       | $V_{DDQ}=V_{DDQ} \text{ Max}$<br>$V_{DDQ}=V_{DDQ} \text{ Min}$    |
| $I_{IL1}$              | I1Z  | Input Leakage Current                                                         | -10  | 10   | $\mu A$ | $V_{IN}=GND \text{ to } V_{DDQ}$<br>$V_{DDQ}=V_{DDQ} \text{ Max}$ |
| $I_{U1}$               | I1U  | Input Pull-Up Current                                                         | -110 | -1   | $\mu A$ | $V_{OUT}=GND$ ,<br>$V_{DDQ}=V_{DDQ} \text{ Max}$                  |
| $V_{T+2}$<br>$V_{T-2}$ | I2   | Input Voltage Schmitt Trigger                                                 | 0.8  | 2.0  | V       | $V_{DDQ}=V_{DDQ} \text{ Max}$<br>$V_{DDQ}=V_{DDQ} \text{ Min}$    |
| $I_{IL2}$              | I2Z  | Input Leakage Current                                                         | -10  | 10   | $\mu A$ | $V_{IN}=GND \text{ to } V_{DDQ}$<br>$V_{DDQ}=V_{DDQ} \text{ Max}$ |
| $I_{U2}$               | I2U  | Input Pull-Up Current                                                         | -110 | -1   | $\mu A$ | $V_{OUT}=GND$ ,<br>$V_{DDQ}=V_{DDQ} \text{ Max}$                  |
| $V_{OH1}$<br>$V_{OL1}$ | O1   | Output Voltage                                                                | 2.4  | 0.4  | V       | $I_{OH1}=I_{OH1} \text{ Min}$<br>$I_{OL1}=I_{OL1} \text{ Max}$    |
| $I_{OH1}$              |      | Output Current                                                                | -4   |      | mA      | $V_{DDQ}=V_{DDQ} \text{ Min}$                                     |
| $I_{OL1}$              |      | Output Current                                                                |      | 4    | mA      | $V_{DDQ}=V_{DDQ} \text{ Min}$                                     |
| $V_{OH2}$<br>$V_{OL2}$ | O2   | Output Voltage                                                                | 2.4  | 0.4  | V       | $I_{OH2}=I_{OH2} \text{ Min}$<br>$I_{OL2}=I_{OL2} \text{ Max}$    |
| $I_{OH2}$              |      | Output Current                                                                | -6   |      | mA      | $V_{DDQ}=3.135V-3.465V$                                           |
| $I_{OL2}$              |      | Output Current                                                                |      | 6    | mA      | $V_{DDQ}=3.135V-3.465V$                                           |
| $I_{OH2}$              |      | Output Current                                                                | -8   |      | mA      | $V_{DDQ}=4.5V-5.5V$                                               |
| $I_{OL2}$              |      | Output Current                                                                |      | 8    | mA      | $V_{DDQ}=4.5V-5.5V$                                               |
| $V_{OH6}$<br>$V_{OL6}$ | O6   | Output Voltage for DASP# pin                                                  | 2.4  | 0.4  | V       | $I_{OH6}=I_{OH6} \text{ Min}$<br>$I_{OL6}=I_{OL6} \text{ Max}$    |
| $I_{OH6}$              |      | Output Current for DASP# pin                                                  | -3   |      | mA      | $V_{DDQ}=3.135V-3.465V$                                           |
| $I_{OL6}$              |      | Output Current for DASP# pin                                                  |      | 8    | mA      | $V_{DDQ}=3.135V-3.465V$                                           |
| $I_{OH6}$              |      | Output Current for DASP# pin                                                  | -3   |      | mA      | $V_{DDQ}=4.5V-5.5V$                                               |
| $I_{OL6}$              |      | Output Current for DASP# pin                                                  |      | 12   | mA      | $V_{DDQ}=4.5V-5.5V$                                               |
| $I_{DD}^{1,2}$         | PWR  | Power supply current<br>( $T_a = 0^\circ C \text{ to } +70^\circ C$ )         |      | 50   | mA      | $V_{DD}=V_{DD} \text{ Max}$<br>$V_{DDQ}=V_{DDQ} \text{ Max}$      |
| $I_{DD}^{1,2}$         | PWR  | Power supply current<br>( $T_a = -40^\circ C \text{ to } +85^\circ C$ )       |      | 75   | mA      | $V_{DD}=V_{DD} \text{ Max}$<br>$V_{DDQ}=V_{DDQ} \text{ Max}$      |
| $I_{SP}$               | PWR  | Sleep/Standby/Idle current<br>( $T_a = 0^\circ C \text{ to } +70^\circ C$ )   |      | 75   | $\mu A$ | $V_{DD}=V_{DD} \text{ Max}$<br>$V_{DDQ}=V_{DDQ} \text{ Max}$      |
| $I_{SP}$               | PWR  | Sleep/Standby/Idle current<br>( $T_a = -40^\circ C \text{ to } +85^\circ C$ ) |      | 200  | $\mu A$ | $V_{DD}=V_{DD} \text{ Max}$<br>$V_{DDQ}=V_{DDQ} \text{ Max}$      |

## 7.2 AC Characteristics



**Figure 7-1: AC Input/Output Reference Waveforms**

AC test inputs are driven at VIHT (0.9 VDD) for a logic "1" and VILT (0.1 VDD) for a logic "0". Measurement reference points for inputs and outputs are VIT (0.5 VDD) and VOT (0.5 VDD). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note:  $V_{IT}$  -  $V_{INPUT}$  Test  
 $V_{OT}$  -  $V_{OUTPUT}$  Test  
 $V_{IHT}$  -  $V_{INPUT\ HIGH}$  Test  
 $V_{ILT}$  -  $V_{INPUT\ LOW}$  Test

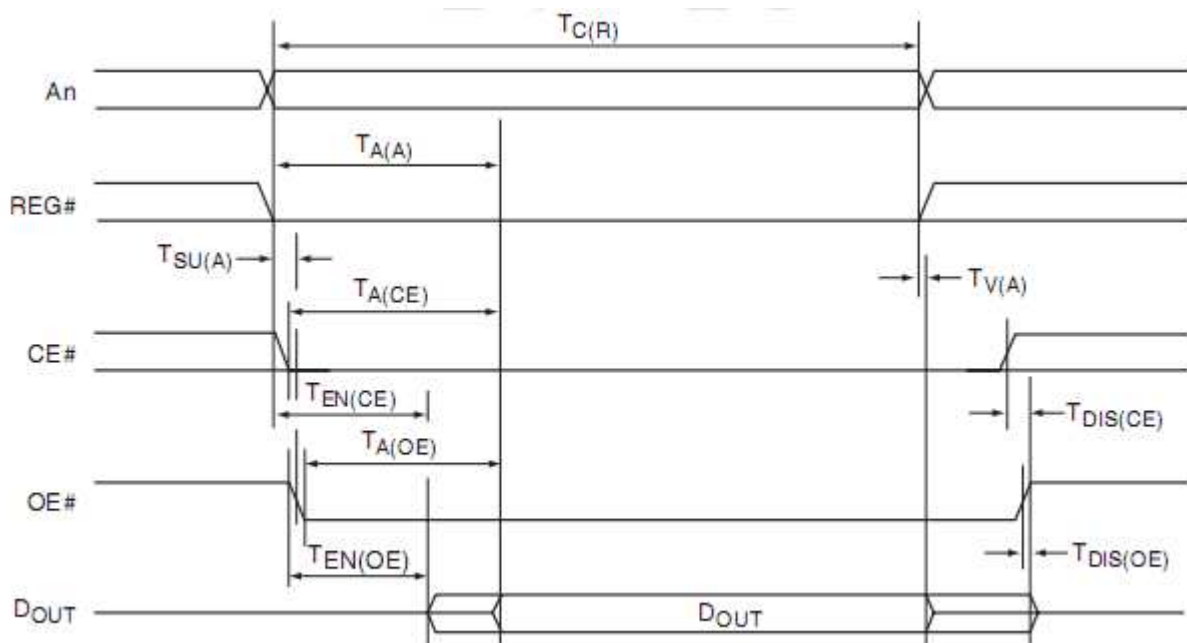
### 7.2.1 Attribute Memory Read Timing Specification

The Attribute Memory access time is defined as 100 ns. Detailed timing specifications are shown in the table below.

Table 7-5: Attribute Memory Read Timing Specification

| Speed Version                  |               |             | 100 ns |      |       |
|--------------------------------|---------------|-------------|--------|------|-------|
| Item                           | Symbol        | IEEE Symbol | Min*   | Max* | Units |
| Read Cycle Time                | $T_{C(R)}$    | tAVAV       | 100    |      | ns    |
| Address Access Time            | $T_{A(A)}$    | tAVQV       |        | 100  | ns    |
| Card Enable Access Time        | $T_{A(CE)}$   | tELQV       |        | 100  | ns    |
| Output Enable Access Time      | $T_{A(OE)}$   | tGLQV       |        | 50   | ns    |
| Output Disable Time from CE#   | $T_{DIS(CE)}$ | tEHQZ       |        | 50   | ns    |
| Output Disable Time from OE#   | $T_{DIS(OE)}$ | tGHQZ       |        | 50   | ns    |
| Address Setup Time             | $T_{SU(A)}$   | tAVGL       | 10     |      | ns    |
| Output Enable Time from CE#    | $T_{EN(CE)}$  | tELQNZ      | 5      |      | ns    |
| Output Enable Time from OE#    | $T_{EN(OE)}$  | tGLQNZ      | 5      |      | ns    |
| Data Valid from Address Change | $T_{V(A)}$    | tAXQZ       | 0      |      | ns    |

\*D<sub>OUT</sub> signifies data provided by the Compact Flash card to the system. The CE# signal or both the OE# signal and the WE# signal must be de-asserted between consecutive cycle operations. All AC specifications are guaranteed by design.



1365 F03.0

Figure 7-2: Attribute Memory Read Timing Diagram

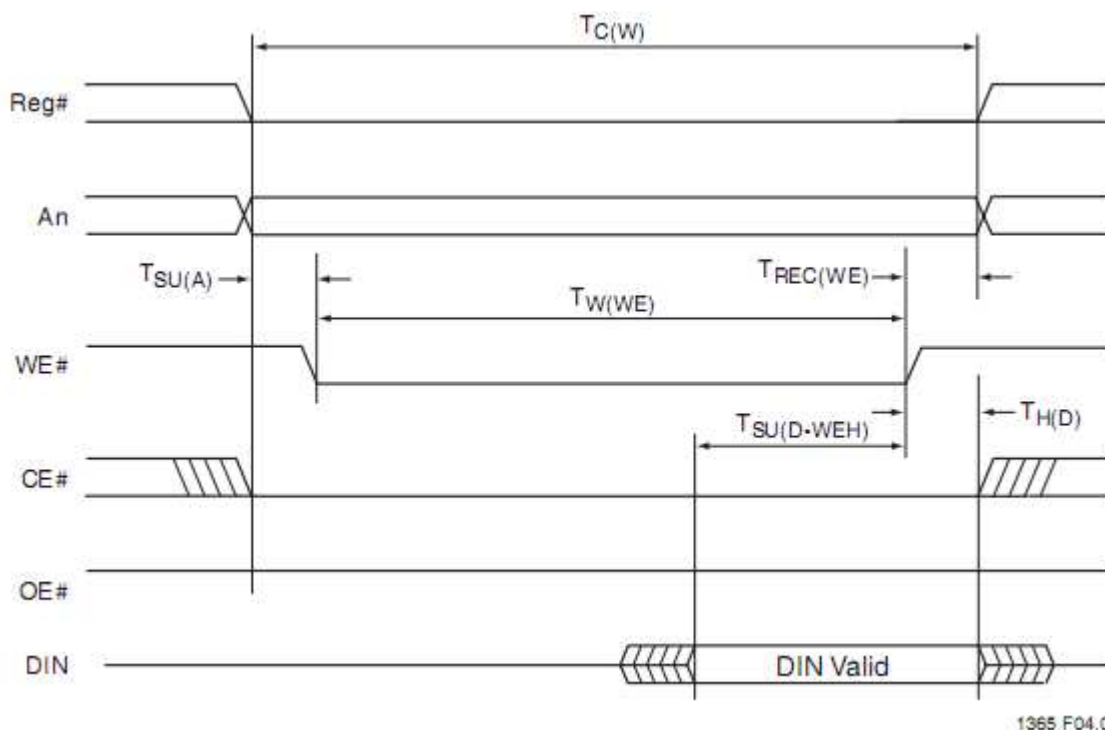
### 7.2.2 Configuration Register (Attribute Memory) Write Specification

The card configuration write access time is defined as 100 ns. Detailed timing specifications are shown in the table below.

**Table 7-6:** Configuration Register (Attribute Memory) Write Timing

| Speed Version          |                  |             | 100 ns |      |       |
|------------------------|------------------|-------------|--------|------|-------|
| Item                   | Symbol           | IEEE Symbol | Min*   | Max* | Units |
| Write Cycle Time       | $T_{C(W)}$       | tAVAV       | 100    |      | ns    |
| Write Pulse Width      | $T_{W(WE)}$      | tWLWH       | 60     |      | ns    |
| Address Setup Time     | $T_{SU(A)}$      | tAVWL       | 10     |      | ns    |
| Write Recover Time     | $T_{REC(WE)}$    | tWMAX       | 15     |      | ns    |
| Data Setup Time for WE | $T_{SU(DWE\#H)}$ | tDVWH       | 40     |      | ns    |
| Data Hold Time         | $T_{H(D)}$       | tWMDX       | 15     |      | ns    |

\*D<sub>IN</sub> signifies data provided by the system to the Compact Flash card. All AC specifications are guaranteed by design.



**Figure 7-3:** Configuration Register (Attribute Memory) Write Timing Diagram

### 7.2.3 Common Memory Read Timing Specification

Table 7-7: Common Memory Read Timing

| Item                        | Symbol        | IEEE Symbol | Min* | Max* | Units |
|-----------------------------|---------------|-------------|------|------|-------|
| Output Enable Access Time   | $T_{A(OE)}$   | tGLQV       |      | 50   | ns    |
| Output Disable Time from OE | $T_{DIS(OE)}$ | tGHQZ       |      | 50   | ns    |
| Address Setup Time          | $T_{SU(A)}$   | tAVGL       | 10   |      | ns    |
| Address Hold Time           | $T_{REC(WE)}$ | tGHAX       | 15   |      | ns    |
| CE Setup before OE          | $T_{SU(CE)}$  | tELGL       | 0    |      | ns    |
| CE Hold following OE        | $T_{H(CE)}$   | tGHEH       | 15   |      | ns    |

\*All AC specifications are guaranteed by design.

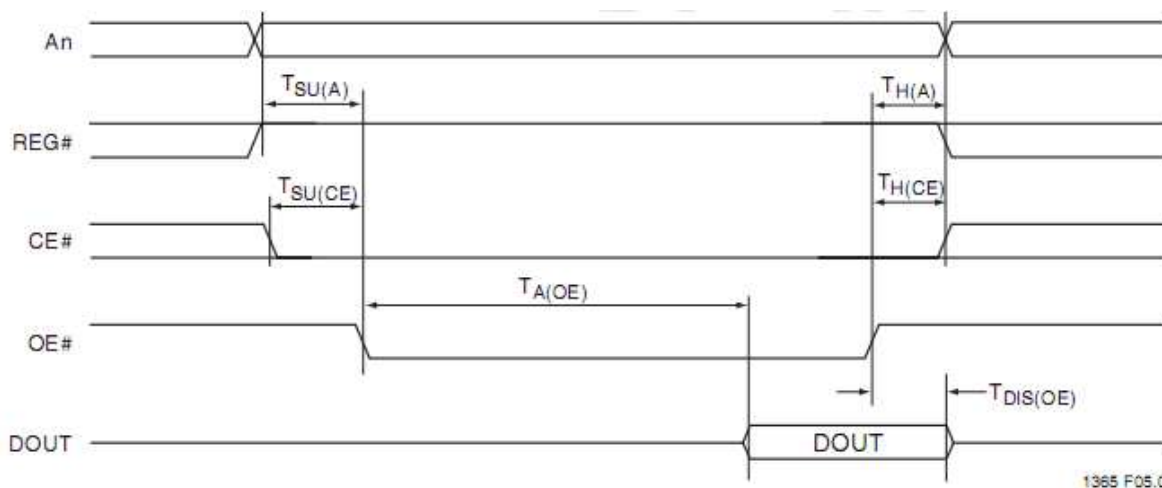


Figure 7-4: Common Memory Read Timing Diagram

## 7.2.4 Common Memory Write Timing Specification

Table 7-8: Common Memory Write Timing

| Item                   | Symbol           | IEEE Symbol | Min* | Max* | Units |
|------------------------|------------------|-------------|------|------|-------|
| Data Setup before WE   | $T_{SU(DWE\#H)}$ | tDVWH       | 40   |      | ns    |
| Data Hold following WE | $T_{H(D)}$       | tWMDX       | 15   |      | ns    |
| WE Pulse Width         | $T_{W(WE)}$      | tWLWH       | 60   |      | ns    |
| Address Setup Time     | $T_{SU(A)}$      | tAVWL       | 10   |      | ns    |
| CE Setup before WE     | $T_{SU(CE)}$     | tELWL       | 0    |      | ns    |
| Write Recovery Time    | $T_{REC(WE)}$    | tWMAX       | 15   |      | ns    |
| Address Hold Time      | $T_{H(A)}$       | tGHAX       | 15   |      | ns    |
| CE Hold following WE   | $T_{H(CE)}$      | tGHEH       | 15   |      | ns    |

\*All AC specifications are guaranteed by design.

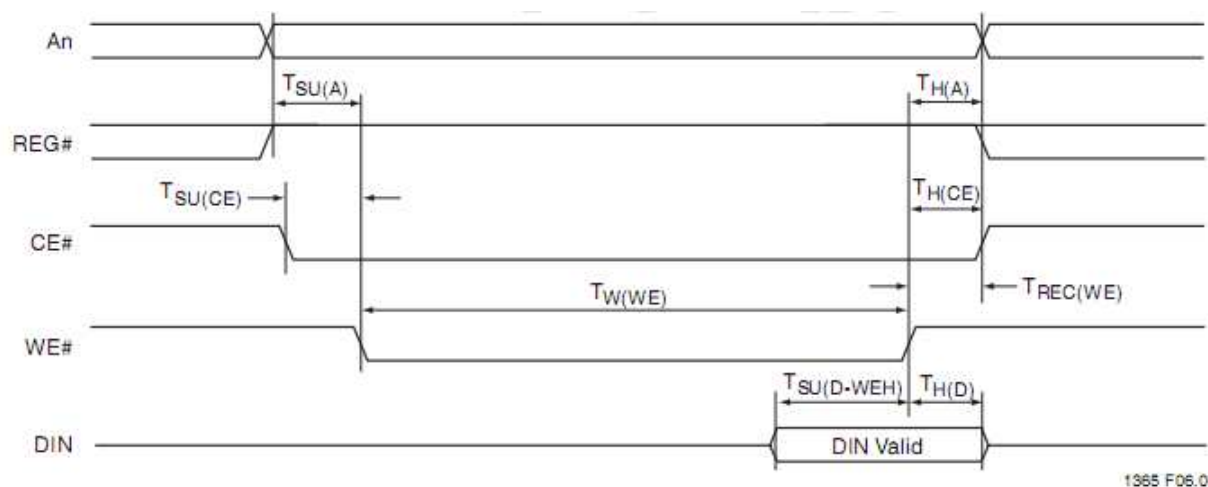


Figure 7-5: Common Memory Write Timing Diagram

## 7.2.5 I/O Input (Read) Timing Specification

Table 7-9: I/O Read Timing

| Item                              | Symbol               | IEEE Symbol | Min* | Max* | Units |
|-----------------------------------|----------------------|-------------|------|------|-------|
| Data Delay after IORD             | $T_{D(IORD)}$        | tIGLQV      |      | 100  | ns    |
| Data Hold following IORD          | $T_{H(IORD)}$        | tIGHQX      | 0    |      | ns    |
| IORD Width Time                   | $T_{W(IORD)}$        | tIGLIGH     | 165  |      | ns    |
| Address Setup before IORD         | $T_{SUA(IORD)}$      | tAVIGL      | 70   |      | ns    |
| Address Hold following IORD       | $T_{HA(IORD)}$       | tIGHAX      | 20   |      | ns    |
| CE Setup before IORD              | $T_{SUCE(IORD)}$     | tELIGL      | 5    |      | ns    |
| CE Hold following IORD            | $T_{HCE(IORD)}$      | tIGHEH      | 20   |      | ns    |
| REG Setup before IORD             | $T_{SUREG(IORD)}$    | tRGLIGL     | 5    |      | ns    |
| REG Hold following IORD           | $T_{HREG(IORD)}$     | tIGHRGH     | 0    |      | ns    |
| INPACK Delay Falling from IORD    | $T_{DFINPACK(IORD)}$ | tIGLIAL     | 0    | 45   | ns    |
| INPACK Delay Rising from IORD     | $T_{DRINPACK(IORD)}$ | tIGHIAH     |      | 45   | ns    |
| IOIS16 Delay Falling from Address | $T_{DFIOIS16(ADR)}$  | tAVISL      |      | 35   | ns    |
| IOIS16 Delay Rising from Address  | $T_{DRIOIS16(ADR)}$  | tAVISH      |      | 35   | ns    |

\*All AC specifications are guaranteed by design.

Note: The maximum load on -INPACK and IOIS16# is 1 LSTTL with 50pF total load.

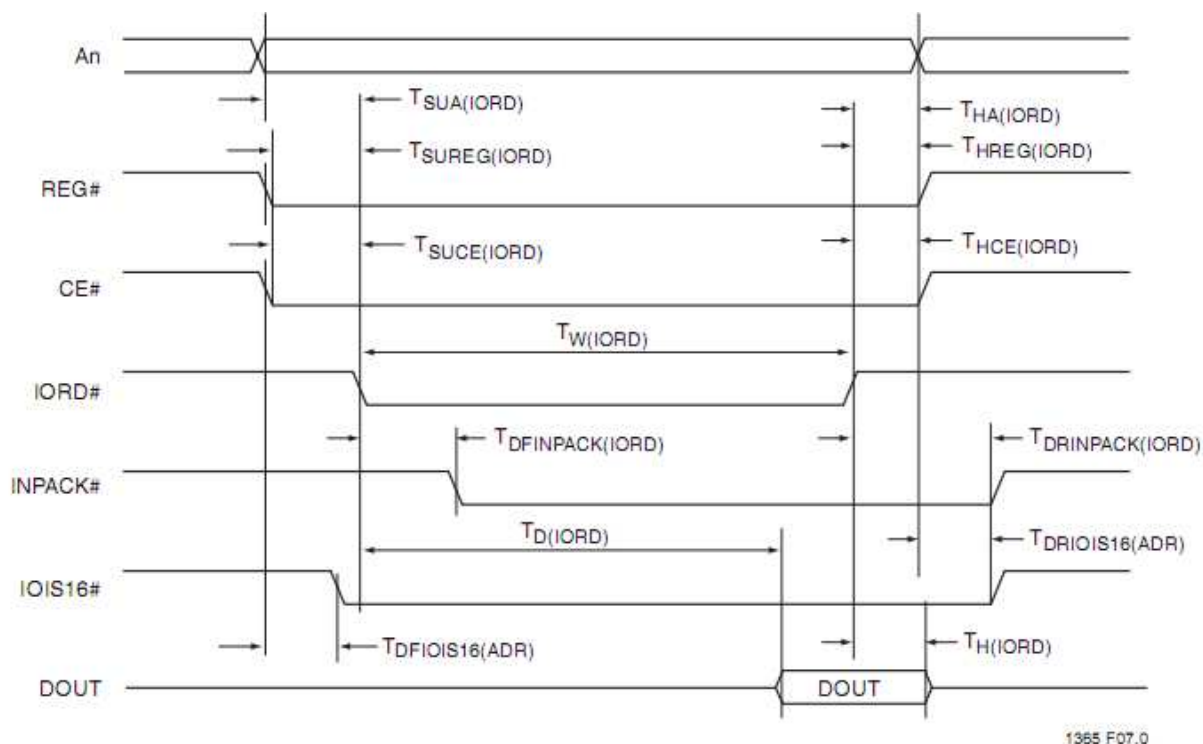


Figure 7-6: I/O Read Timing Diagram

## 7.2.6 I/O Output (Write) Timing Specification

Table 7-10: I/O Write Timing

| Item                              | Symbol              | IEEE Symbol | Min* | Max* | Units |
|-----------------------------------|---------------------|-------------|------|------|-------|
| Data Setup before IOWR            | $T_{SU(IOWR)}$      | tDVIWH      | 60   |      | ns    |
| Data Hold following IOWR          | $T_{H(IOWR)}$       | tIWHDX      | 30   |      | ns    |
| IOWR Width Time                   | $T_{W(IOWR)}$       | tIWL IWH    | 165  |      | ns    |
| Address Setup before IOWR         | $T_{SUA(IOWR)}$     | tAVIWL      | 70   |      | ns    |
| Address Hold following IOWR       | $T_{HA(IOWR)}$      | tIWHAX      | 20   |      | ns    |
| CE Setup before IOWR              | $T_{SUCE(IOWR)}$    | tELIWL      | 5    |      | ns    |
| CE Hold following IOWR            | $T_{HCE(IOWR)}$     | tIWHEH      | 20   |      | ns    |
| REG Setup before IOWR             | $T_{SUREG(IOWR)}$   | tRGLIWL     | 5    |      | ns    |
| REG Hold following IOWR           | $T_{HREG(IOWR)}$    | tIWHRGH     | 0    |      | ns    |
| IOIS16 Delay Falling from Address | $T_{DFIOIS16(ARD)}$ | tAVISL      |      | 35   | ns    |
| IOIS16 Delay Rising from Address  | $T_{DRIOIS16(ADR)}$ | tAVISH      |      | 35   | ns    |

\*All AC specifications are guaranteed by design.

Note: The maximum load on  $\overline{\text{INPACK}}$  and IOIS16# is 1 LSTTL with 50pF total load.

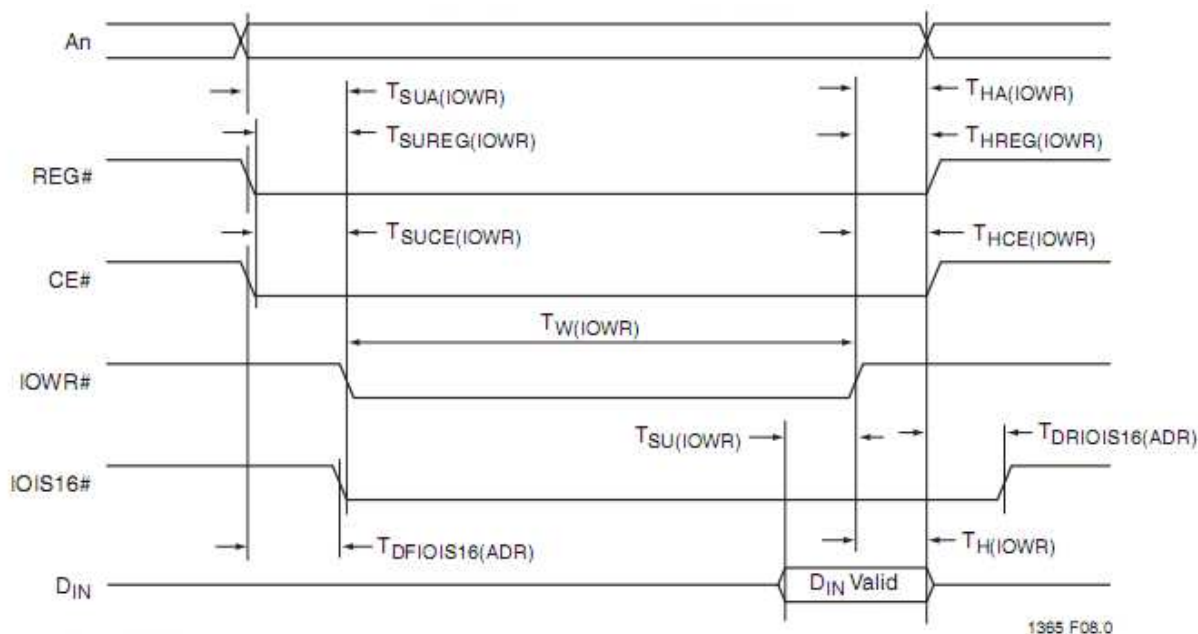


Figure 7-7: I/O Write Timing Diagram

## 7.2.7 Ultra DMA Mode Data Transfer Input/Output (Read/Write) Timing

**Table 7-11:** Ultra DMA Data Burst Timing Specifications<sup>1</sup>

| Name                 | Descriptions                                                                                                                             | Mode 4 |     | Unit | Measurement Location <sup>2</sup> |
|----------------------|------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|------|-----------------------------------|
|                      |                                                                                                                                          | Min    | Max |      |                                   |
| T <sub>2CYCTYP</sub> | Typical sustained average two cycle time                                                                                                 | 60     |     | ns   | Sender                            |
| T <sub>CYC</sub>     | Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)                                                 | 25     |     | ns   | Note <sup>3</sup>                 |
| T <sub>2CYC</sub>    | Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)  | 57     |     | ns   | Sender                            |
| T <sub>DS</sub>      | Data setup time at recipient (from data valid until STROBE edge) <sup>4,5</sup>                                                          | 5.0    |     | ns   | Recipient                         |
| T <sub>DH</sub>      | Data hold time at Recipient (from STROBE edge until data becomes invalid) <sup>1,2</sup>                                                 | 5.0    |     | ns   | Recipient                         |
| T <sub>DVS</sub>     | Data valid setup time for Sender (from data valid until STROBE edge) <sup>6</sup>                                                        | 6.0    |     | ns   | Sender                            |
| T <sub>DVH</sub>     | Data valid hold time at Sender (from STROBE edge until data becomes invalid) <sup>3</sup>                                                | 6.0    |     | ns   | Sender                            |
| T <sub>CS</sub>      | CRC word setup time at device <sup>1</sup>                                                                                               | 5.0    |     | ns   | Device                            |
| T <sub>CH</sub>      | CRC word hold time at device <sup>1</sup>                                                                                                | 5.0    |     | ns   | Device                            |
| T <sub>CVS</sub>     | CRC word valid setup time at host (from CRC valid until DMACK negation) <sup>3</sup>                                                     | 6.7    |     | ns   | Host                              |
| T <sub>CVH</sub>     | CRC word valid hold time at Sender (from DMACK negation until CRC becomes invalid) <sup>3</sup>                                          | 6.2    |     | ns   | Host                              |
| T <sub>ZFS</sub>     | Time from STROBE output released-to-driving until the first transition of critical timing                                                | 0      |     | ns   | Device                            |
| T <sub>DZFS</sub>    | Time from data output released-to-driving until the first transition of critical timing                                                  | 6.7    |     | ns   | Sender                            |
| T <sub>FS</sub>      | First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)                                                  |        | 120 | ns   | Device                            |
| T <sub>LI</sub>      | Limited interlock time <sup>7</sup>                                                                                                      | 0      | 100 | ns   | Note <sup>8</sup>                 |
| T <sub>MLI</sub>     | Interlock time with minimum <sup>4</sup>                                                                                                 | 20     |     | ns   | Host                              |
| T <sub>UI</sub>      | Unlimited interlock time <sup>4</sup>                                                                                                    | 0      |     | ns   | Host                              |
| T <sub>AZ</sub>      | Maximum time allowed for output drivers to release (from asserted to negated)                                                            |        | 10  | ns   | Note <sup>9</sup>                 |
| T <sub>ZAH</sub>     | Minimum delay time required for output                                                                                                   | 20     |     | ns   | Host                              |
| T <sub>ZAD</sub>     | Drivers to assert or negate (from released)                                                                                              | 0      |     | ns   | Device                            |
| T <sub>ENV</sub>     | Envelope time (from DMACK# to STOP and HDMARDY# during data in burst initiation and from DMACK to STOP during data our burst initiation) | 20     | 55  | ns   | Host                              |
| T <sub>RFS</sub>     | Ready-to-final STROBE time (no STROBE edge are sent this long after negation of DMARDY)                                                  |        | 60  | ns   | Sender                            |
| T <sub>RP</sub>      | Ready-to-pause time (Recipient waits to pause until after negating DMARDY)                                                               | 100    |     | ns   | Recipient                         |
| T <sub>IORDYZ</sub>  | Maximum time before releasing IORDY                                                                                                      |        | 20  | ns   | Device                            |
| T <sub>ZIORDY</sub>  | Minimum time before driving IORDY <sup>10</sup>                                                                                          | 0      |     | ns   | Device                            |
| T <sub>ACK</sub>     |                                                                                                                                          | 20     |     | ns   | Host                              |
| T <sub>SS</sub>      |                                                                                                                                          | 50     |     | ns   | Sender                            |

## Value Added Compact Flash III series

### AP-CFxxxxxE3XR-XXXXXXK

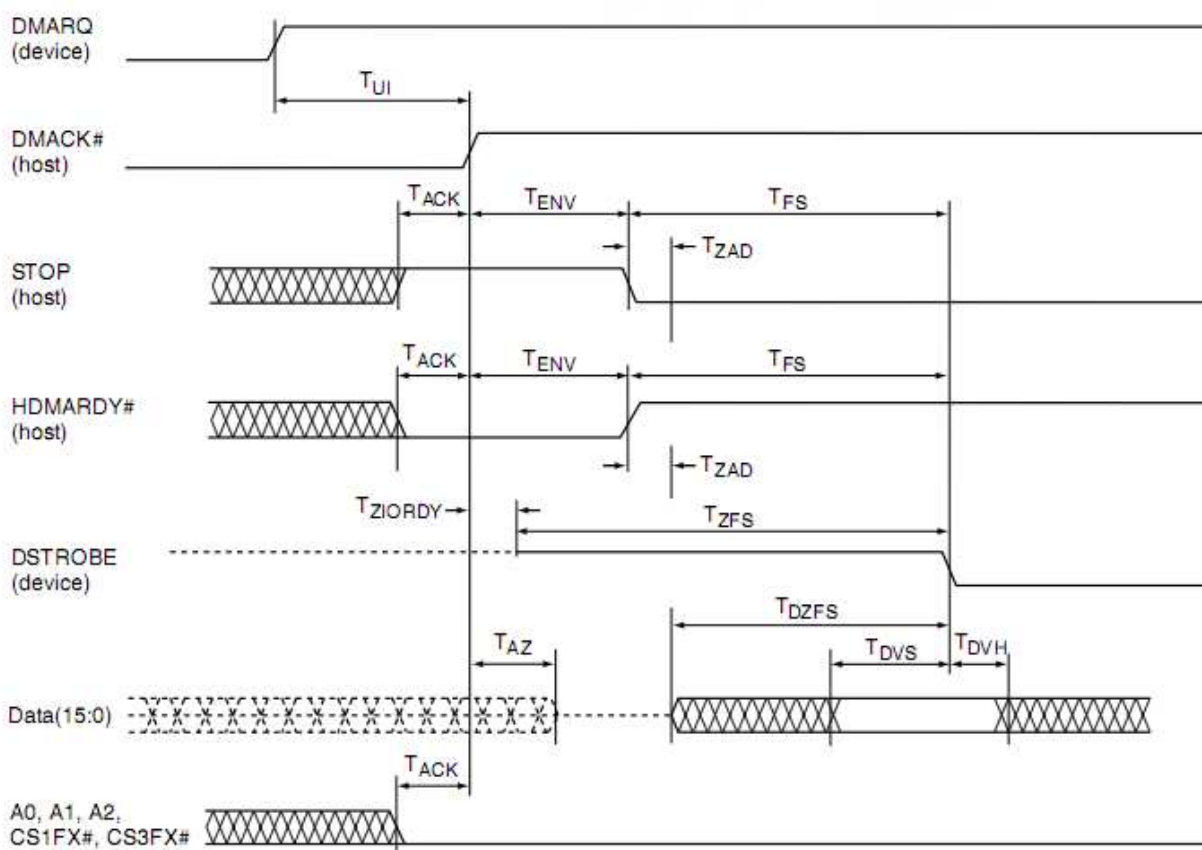


- 
1. All timing measurement switching points (low-to-high and high-to-low) are taken at 1.5V.
  2. All signal transitions for a timing parameter are measured at the connector specified in the measurement location column. For example, in the case of TRFS, both STROBE and DMARDY Transitions are measured at the Sender connector.
  3. The parameter TCYC is measured at the recipient's connector farthest from the Sender.
  4. 80-Conductor cabling is required in order to meet sup (TDS, TCS) and hold (TDH, TCH) times in modes greater than two.
  5. The parameters TDS and TDH for Mode 5 are defined for a Recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for TDS and TDH for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.
  6. Timing for TDVS, TDVH, TCVS, and TCVH are met for lumped capacitive loads of 15 and 50 pf at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.
  7. The parameters TUI, TMLI, and TLI indicate Sender-to-Recipient or Recipient-to-Sender interlocks. For example, one agent (either Sender or Recipient) is waiting for the other agent to respond with a signal before proceeding; TUI is an unlimited interlock that has no maximum time value, TMLI is a limited time-out that has a defined minimum, and TLI is a limited time-out that has a defined maximum.
  8. The parameter TLI is measured at the connector of the Sender or Recipient that is responding to an incoming transition from the Recipient or Sender respectively. Both the incoming signal and the outgoing response are measured at the same connector.
  9. The parameter TAZ is measured at the connector of the Sender or Recipient that is driving the bus but must release the bus that allow for a bus turnaround.
  10. For all modes the parameter TZIORDY may be greater than TENV because the host has a pull-on IORDY giving it a known state when released.

**Table 7-12:** Ultra DMA Sender and Recipient IC Timing Specifications<sup>1</sup>

| Name        | Descriptions                                                                           | Mode 4 |     | Unit |
|-------------|----------------------------------------------------------------------------------------|--------|-----|------|
|             |                                                                                        | Min    | Max |      |
| $T_{DSIC}$  | Recipient IC data setup time (from data valid until STROBE edge) <sup>2</sup>          | 4.8    |     | ns   |
| $T_{DHIC}$  | Recipient IC data hold time (from STROBE edge until data becomes invalid) <sup>1</sup> | 4.8    |     | ns   |
| $T_{DVSIC}$ | Sender IC data valid setup time (from data valid until STROBE edge) <sup>3</sup>       | 9.5    |     | ns   |
| $T_{DVHIC}$ |                                                                                        | 9.0    |     | ns   |

1. All timing measurement switching point (low-to-high and high-to-low)
2. The correct data value is captured by the Recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at  $T_{DSIC}$  and  $T_{DHIC}$  timing (as measured through 1.5 V).
3. The parameters  $T_{DVSIC}$  and  $T_{DVHIC}$  are met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.



**Figure 7-8:** Initiating an Ultra DMA Data-In Burst

Notes:

1. The definitions for the DIOW::STOP, DIOR::HDMARDY::HSTROBE, and IORDY::DDRARDY:: DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

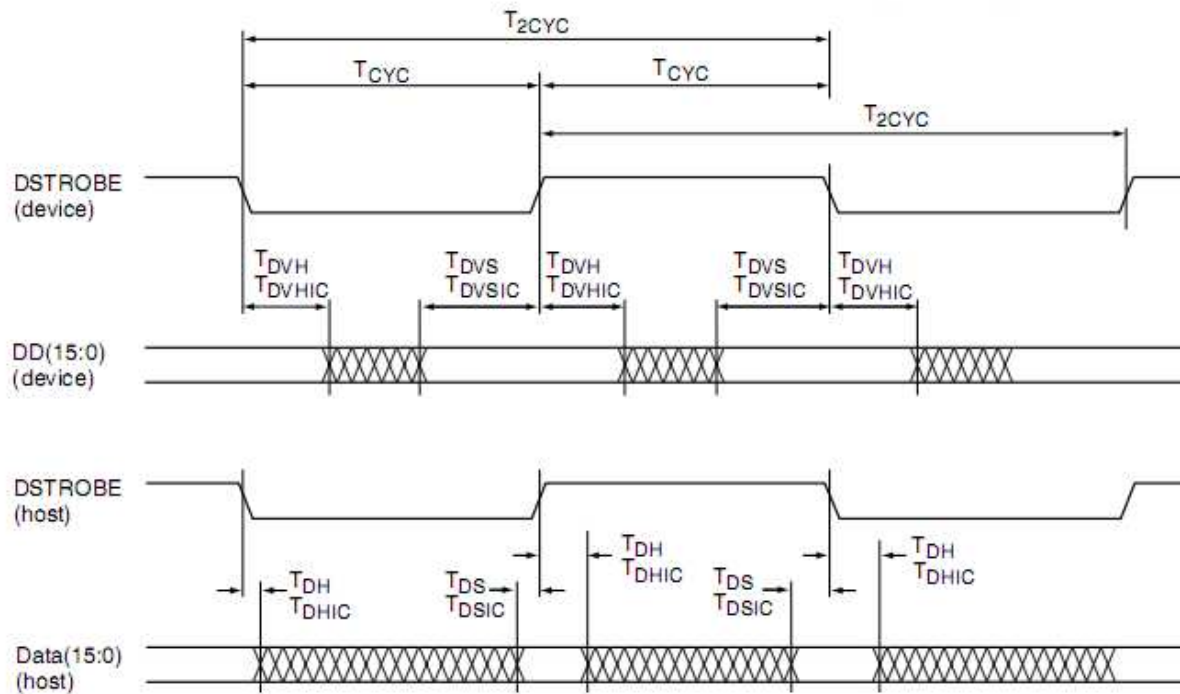
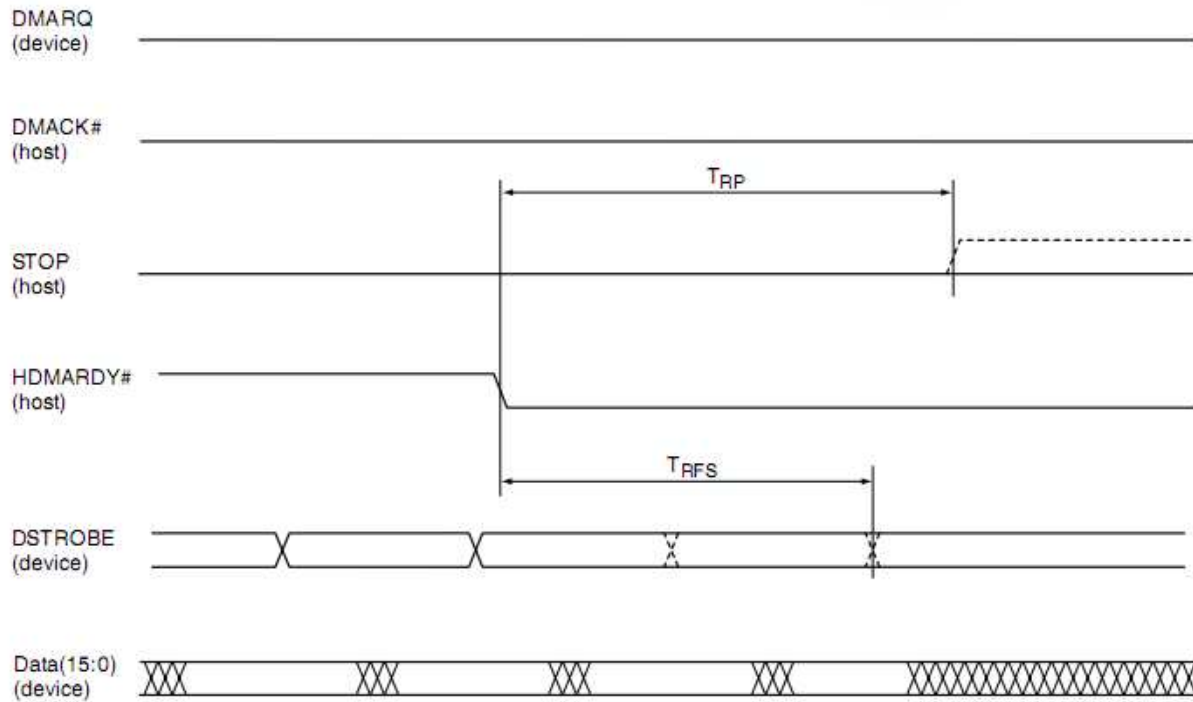


Figure 7-9: Sustained Ultra DMA Data-In Burst

Notes:

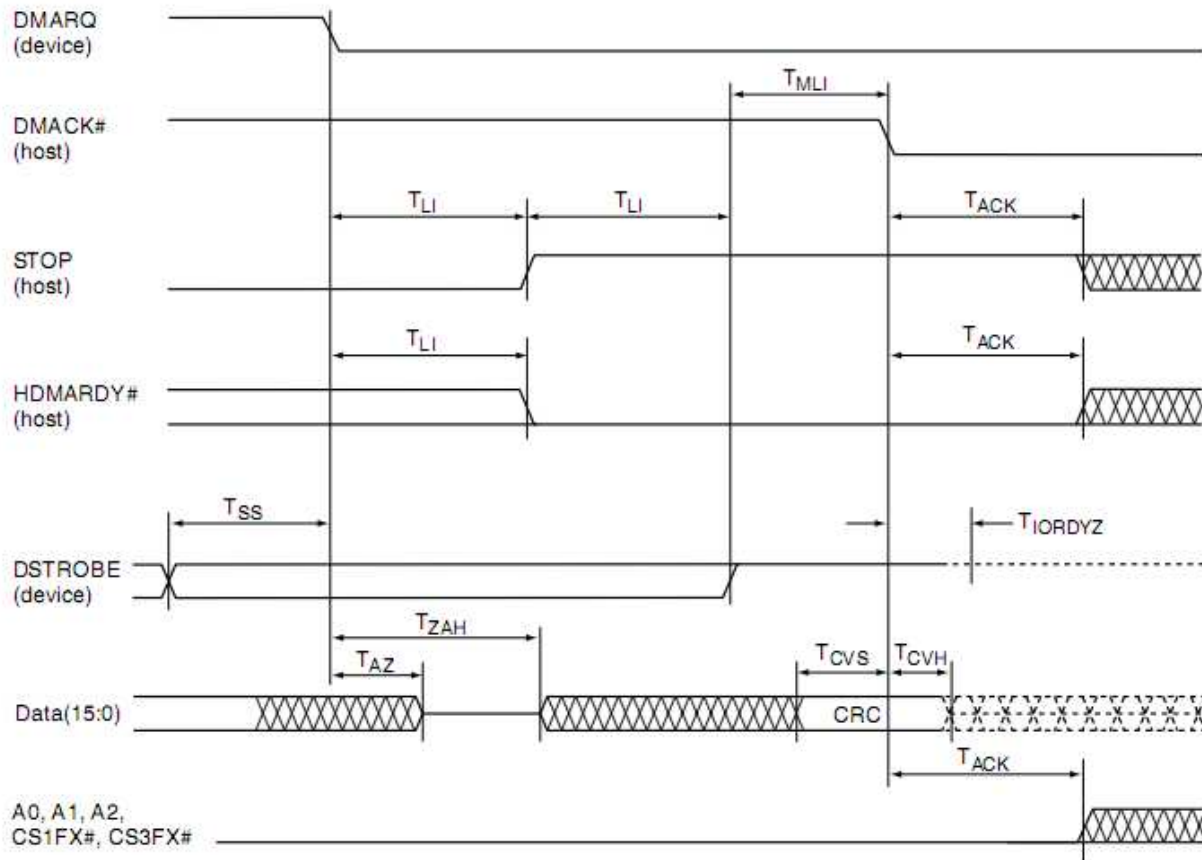
1. DD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay will not allow the data signals to be considered stable at the host until some time after they are driven by the device.



**Figure 7-10: Sustained Ultra DMA Data-In Burst**

Notes:

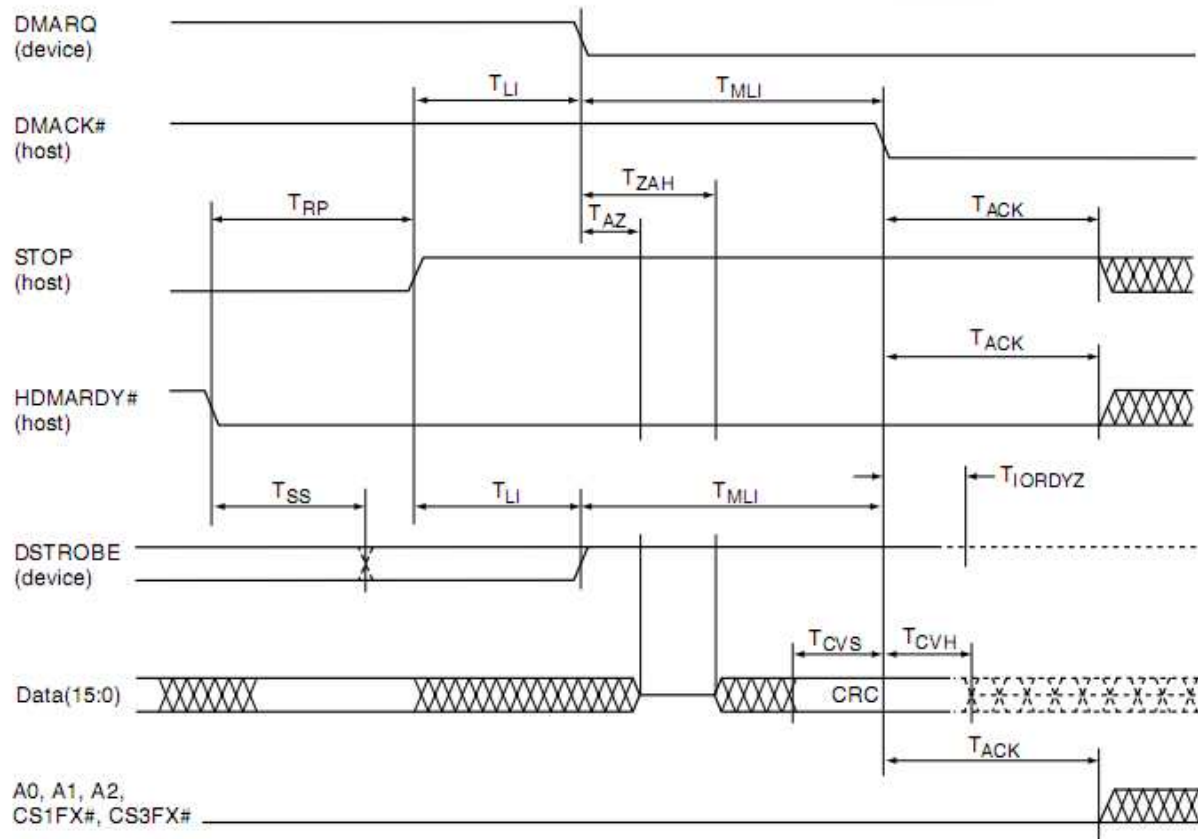
1. The host may assert STOP to request termination of the Ultra DMA burst no sooner than  $T_{RP}$  after HDMARDY# is negated.
2. After negating HDMARDY#, the host may receive zero, one, two, or three more data words from the device.



**Figure 7-11:** Device Terminating and Ultra DMA Data-In Burst

Notes:

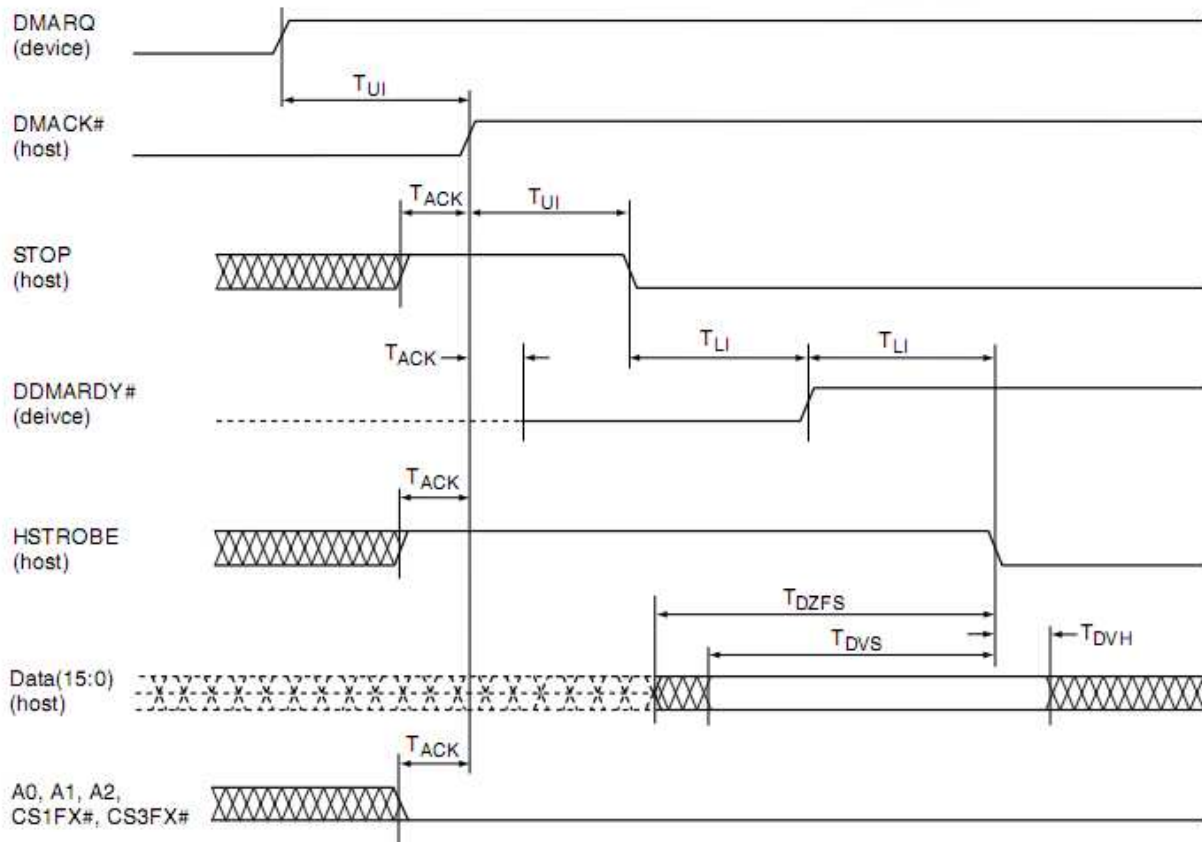
1. The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.



**Figure 7-12: Host Terminating and Ultra DMA Data-In Burst**

Notes:

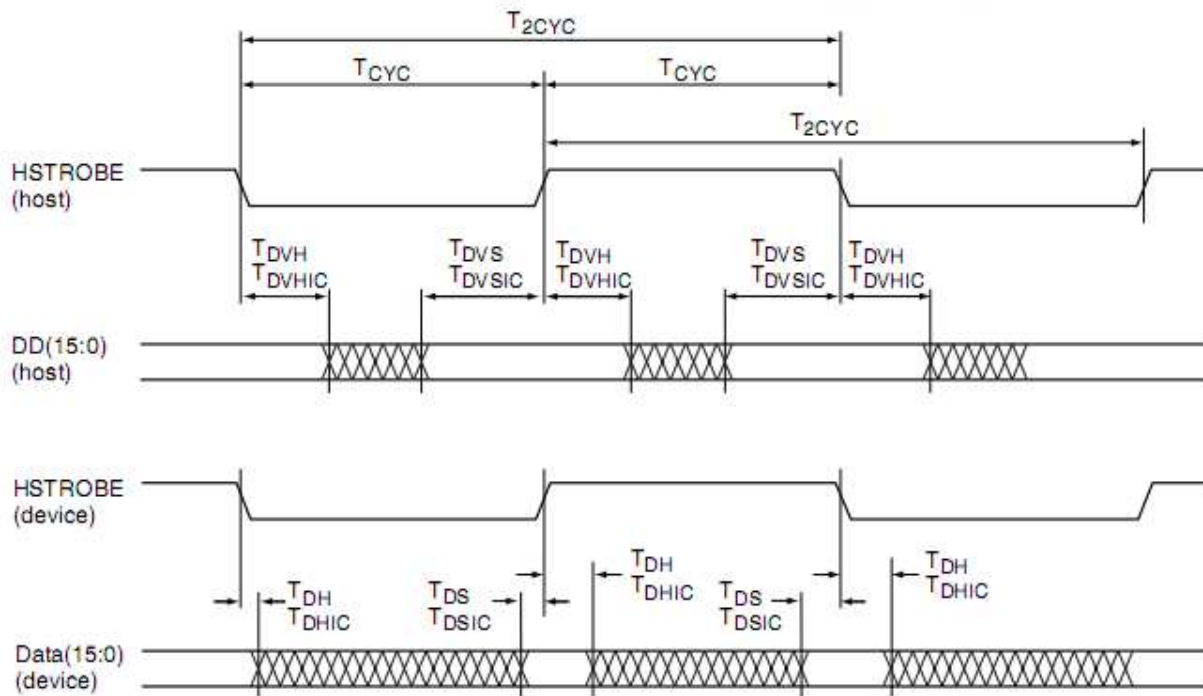
1. The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.



**Figure 7-13: Initiating an Ultra DMA Data-Out Burst**

Notes:

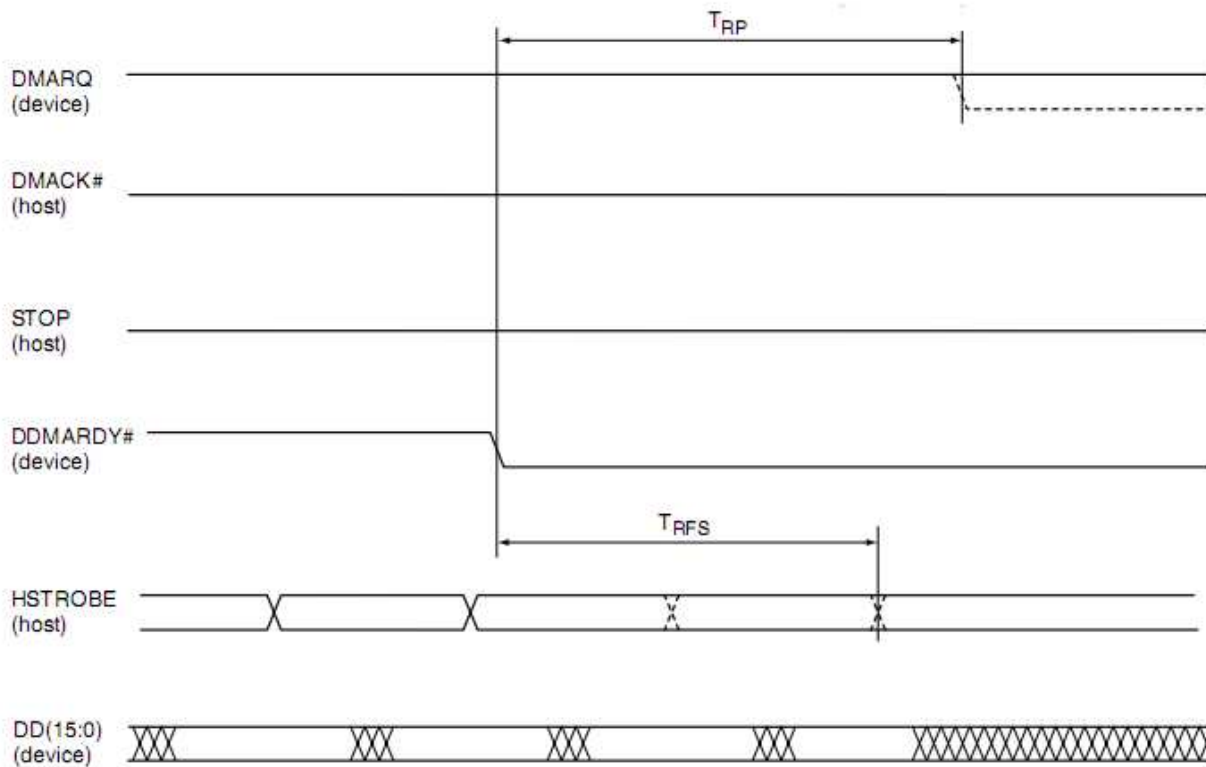
1. The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.



**Figure 7-14:** Sustained Ultra DMA Data-Out Burst

Notes:

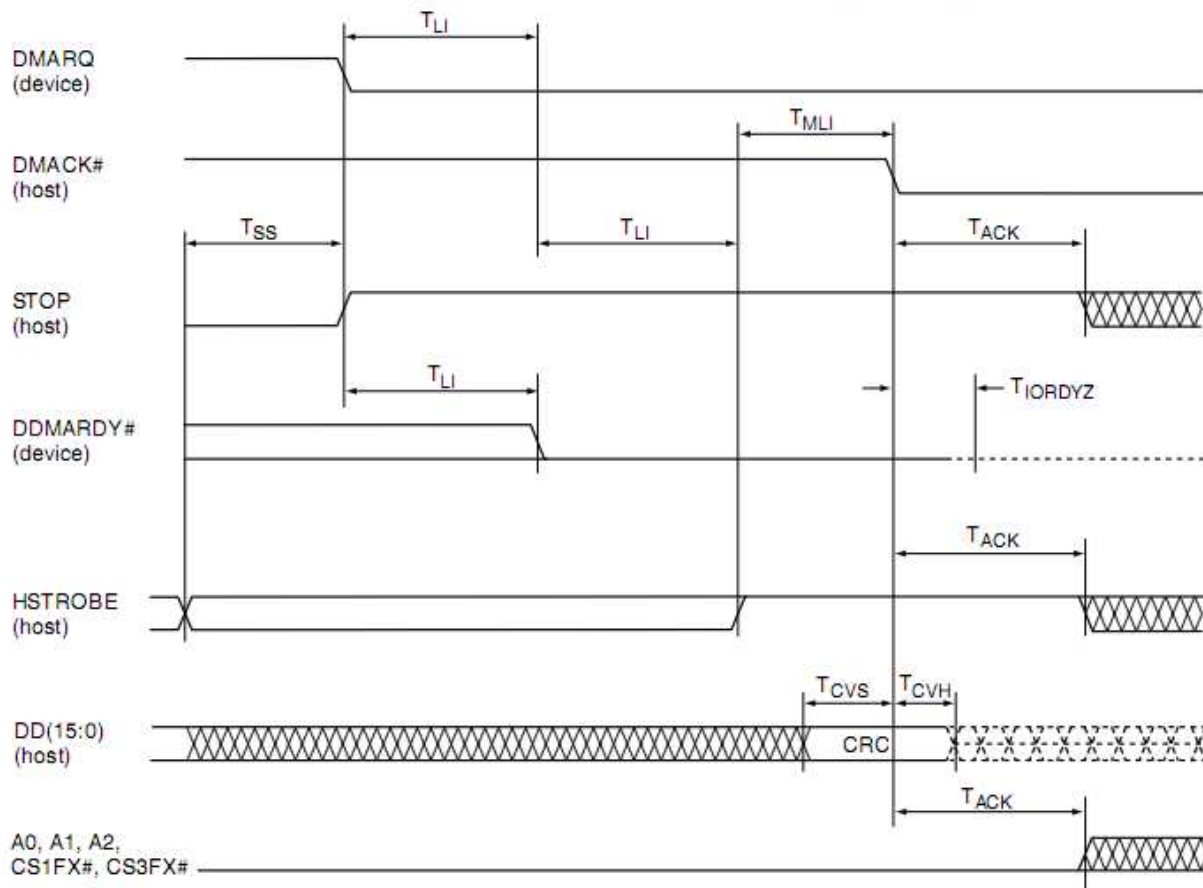
1. DD(15:0) and HSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay will not allow the data signals to be considered stable at the host until some time after they are driven by the host.



**Figure 7-15:** Device Pausing and Ultra DMA Data-Out Burst

Notes:

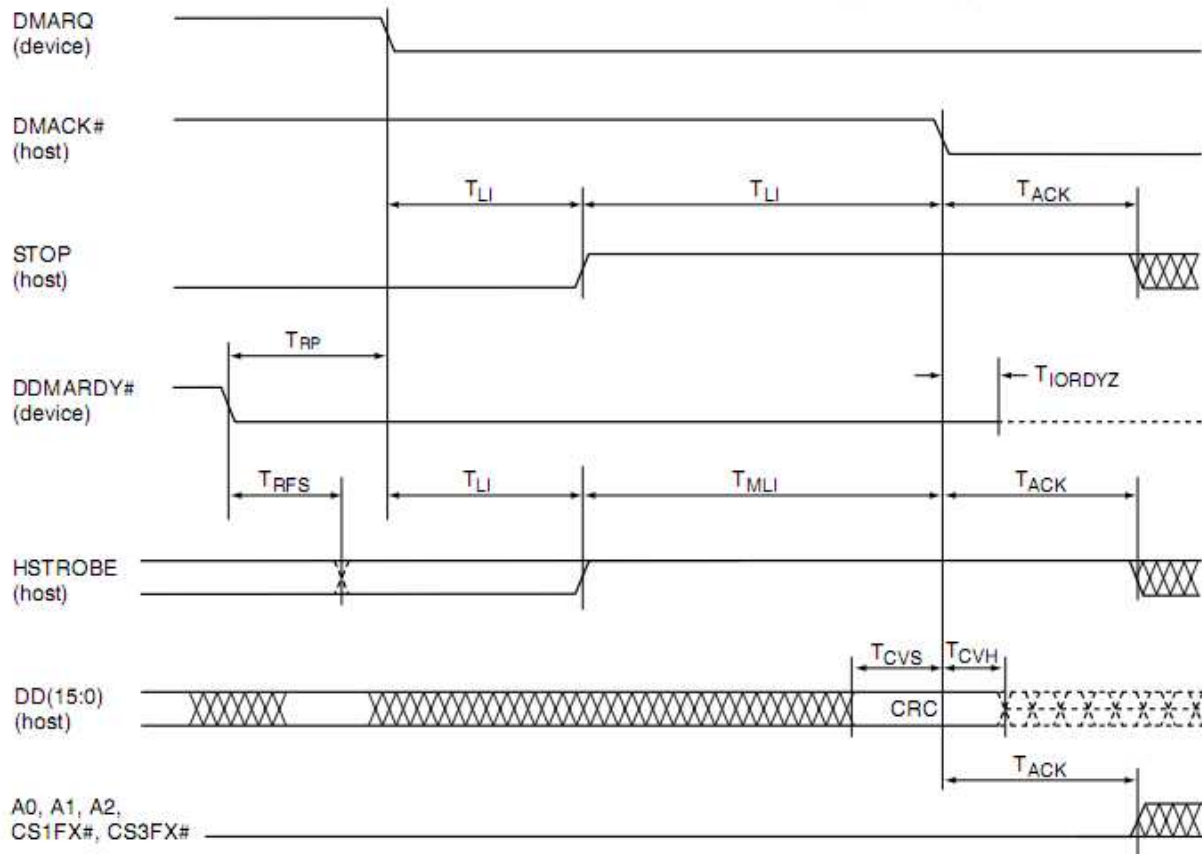
1. The host may negate DMARQ to request termination of the Ultra DMA burst no sooner than  $T_{RP}$  after DDMARDY# is negated.
2. After negating DDMARDY#, the host may receive zero, one, two, or three more data words from the host.



**Figure 7-16:** Host Terminating and Ultra DMA Data-Out Burst

Notes:

1. The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.



**Figure 7-17: Device Terminating and Ultra DMA Data-Out Burst**

Notes:

1. The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

## 7.2.8 Media Side Interface I/O Timing Specifications

**Table 7-13:** Timing Parameter

| Symbol           | Parameter                                     | Min | Max | Units |
|------------------|-----------------------------------------------|-----|-----|-------|
| T <sub>CLS</sub> | FCLE Setup Time                               | 20  | -   | ns    |
| T <sub>CLH</sub> | FCLE Hold Time                                | 40  | -   | ns    |
| T <sub>CS</sub>  | FCE# Setup Time                               | 40  | -   | ns    |
| T <sub>CH</sub>  | FCE# Hold Time for Command/Data Write Cycle   | 40  | -   | ns    |
| T <sub>CHR</sub> | FCE# Hold Time for Sequential Read Last Cycle | -   | 40  | ns    |
| T <sub>WP</sub>  | FWE# Pulse Width                              | 20  | -   | ns    |
| T <sub>WH</sub>  | FWE# High Hold Time                           | 20  | -   | ns    |
| T <sub>WC</sub>  | Write Cycle Time                              | 40  | -   | ns    |
| T <sub>ALS</sub> | FALE Setup Time                               | 20  | -   | ns    |
| T <sub>ALH</sub> | FALE Hold Time                                | 40  | -   | ns    |
| T <sub>DS</sub>  | FAD[15:0] Setup Time                          | 20  | -   | ns    |
| T <sub>DH</sub>  | FAD[15:0] Hold Time                           | 20  | -   | ns    |
| T <sub>RP</sub>  | FRE# Pulse Width                              | 20  | -   | ns    |
| T <sub>RR</sub>  | Ready to FRE# Low                             | 40  | -   | ns    |
| T <sub>RES</sub> | FRE# Data Setup Access Time                   | 20  | -   | ns    |
| T <sub>RC</sub>  | Read Cycle Time                               | 40  | -   | ns    |
| T <sub>REH</sub> | FRE# High Hold Time                           | 20  | -   | ns    |
| T <sub>RHZ</sub> | FRE# High to Data Hi-Z                        | 5   | -   | ns    |

**Note:** All AC specifications are guaranteed by design.

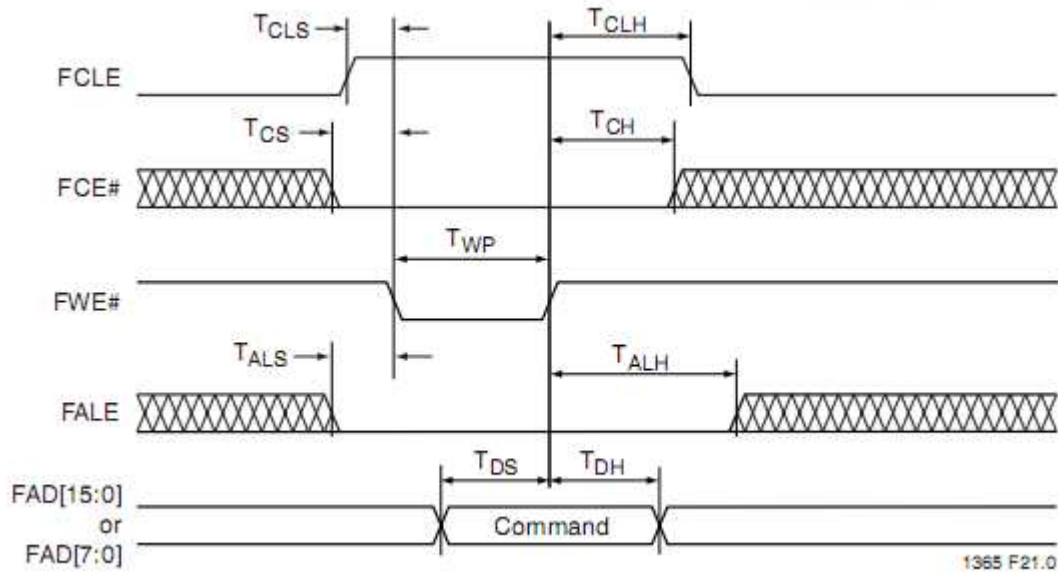


Figure 7-18: Media Command Latch Cycle

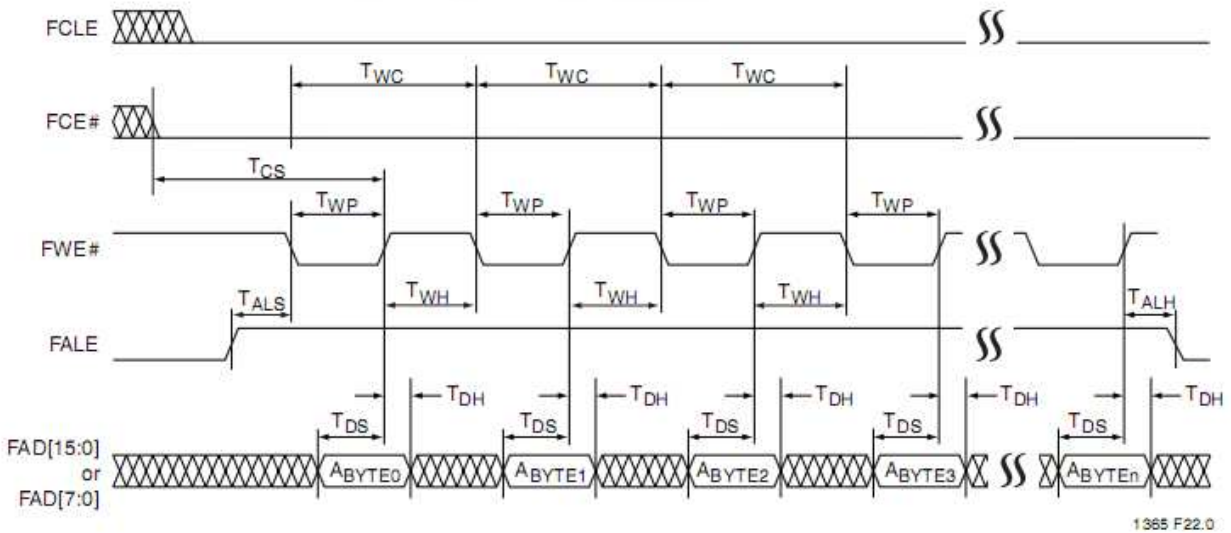


Figure 7-19: Media Access Latch Cycle

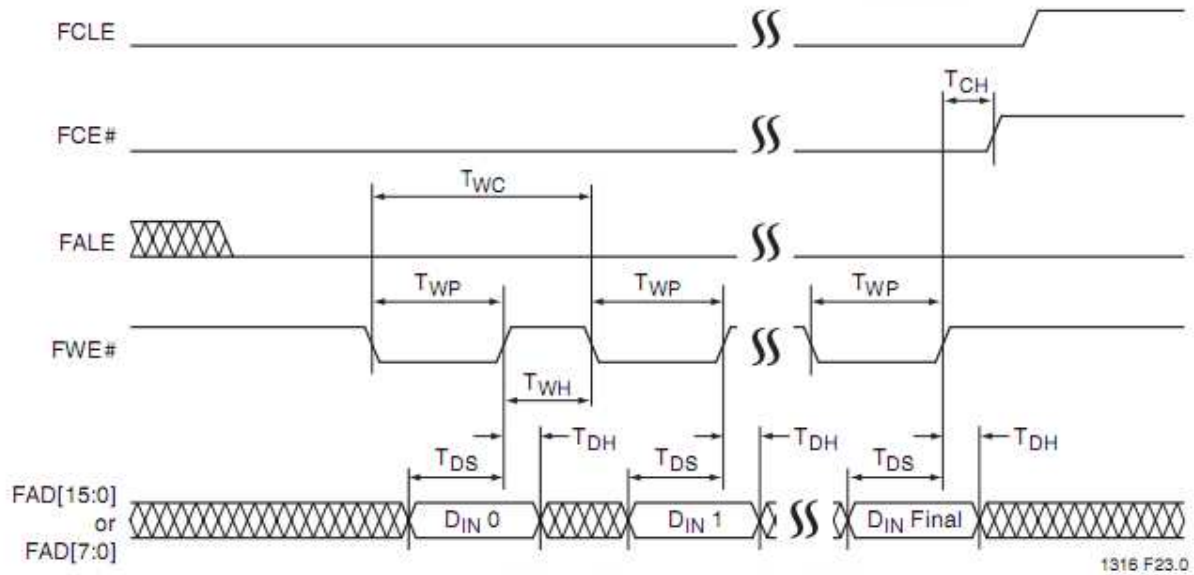


Figure 7-20: Media Data Loading Latch Cycle

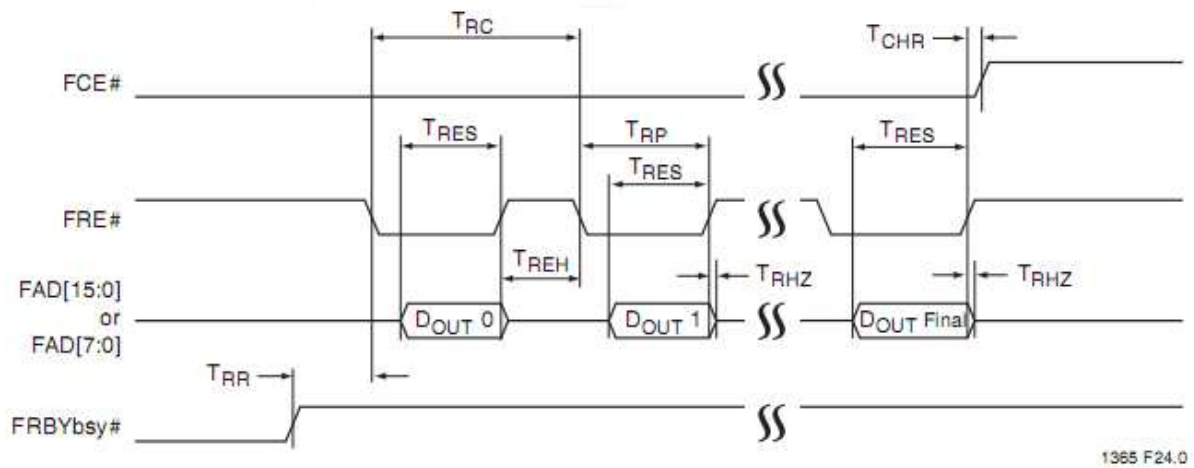


Figure 7-21: Media Data Read Cycle

## 8. Physical Characteristics

### 8.1 Dimension

TABLE 8-1: Type I CFC physical specification

|                                   |                                      |
|-----------------------------------|--------------------------------------|
| Length:                           | 36.40 +/- 0.15mm (1.433+/- 0.06 in.) |
| Width:                            | 42.80 +/- 0.10mm (1.685+/- 0.04 in.) |
| Thickness (Including Label Area): | 3.3mm+/-0.10mm (0.130+/-0.04in.)     |

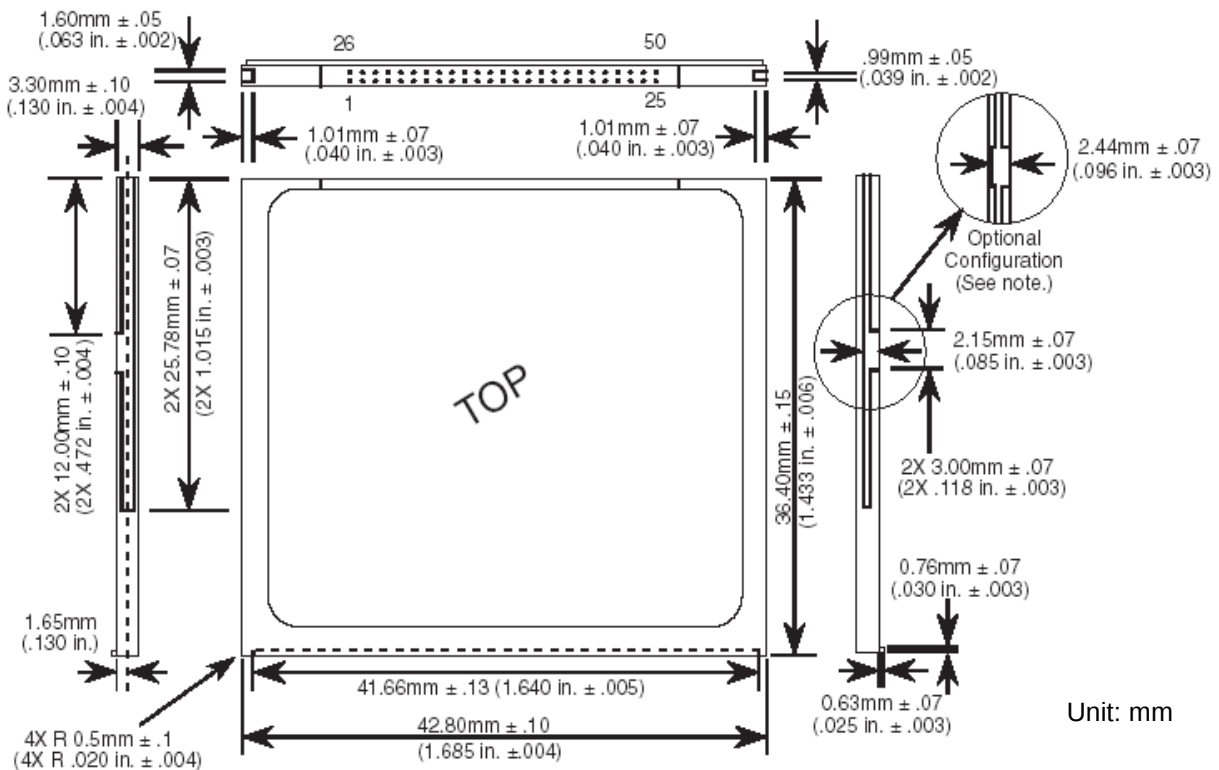


FIGURE 8-1: Physical dimension

## 9. Product Ordering Information

### 9.1 Product Code Designations

A P – C F x x x x E 3 X R – X X X X X X K

#### Specification

NR: Non-Removable Setting  
NDNR: Non-DMA + Non-Removable  
ETNR: Ext. Temp. + Non-Removable  
ETNDNR: Ext. Temp + Non-DMA + Non-Removable  
K: Value Added III

RoHS Compliant

#### Configuration

E: Standard  
F: High Speed

Controller Type

CFC Type

#### Capacity:

128M: 128MB  
256M: 256MB  
512M: 512MB  
001G: 1GB  
002G: 2GB  
004G: 4GB  
008G: 8GB  
016G: 16GB

Model Name

Apacer Product Code

---

## 9.2 Valid Combinations

---

### Standard Temperature

#### Non-Removable

##### Standard

##### High Speed

| Capacity | Model Number      | Capacity | Model Number      |
|----------|-------------------|----------|-------------------|
| 128MB    | AP-CF128ME3ER-NRK | 256MB    | AP-CF256ME3FR-NRK |
| 256MB    | AP-CF256ME3ER-NRK | 512MB    | AP-CF512ME3FR-NRK |
| 512MB    | AP-CF512ME3ER-NRK | 1GB      | AP-CF001GE3FR-NRK |
| 1GB      | AP-CF001GE3ER-NRK | 2GB      | AP-CF002GE3FR-NRK |
| 2GB      | AP-CF002GE3ER-NRK | 4GB      | AP-CF004GE3FR-NRK |
| 16GB     | AP-CF016GE3ER-NRK | 8GB      | AP-CF008GE3FR-NRK |

#### Non-DMA & Non-Removable

##### Standard

##### High Speed

| Capacity | Model Number        | Capacity | Model Number        |
|----------|---------------------|----------|---------------------|
| 128MB    | AP-CF128ME3ER-NDNRK | 256MB    | AP-CF256ME3FR-NDNRK |
| 256MB    | AP-CF256ME3ER-NDNRK | 512MB    | AP-CF512ME3FR-NDNRK |
| 512MB    | AP-CF512ME3ER-NDNRK | 1GB      | AP-CF001GE3FR-NDNRK |
| 1GB      | AP-CF001GE3ER-NDNRK | 2GB      | AP-CF002GE3FR-NDNRK |
| 2GB      | AP-CF002GE3ER-NDNRK | 4GB      | AP-CF004GE3FR-NDNRK |
| 16GB     | AP-CF016GE3ER-NDNRK | 8GB      | AP-CF008GE3FR-NDNRK |

**Value Added Compact Flash III series**  
**AP-CFxxxxE3XR-XXXXXXK**



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**Extended Temperature**

**Non-Removable**

**Standard**

**High Speed**

| Capacity | Model Number        | Capacity | Model Number        |
|----------|---------------------|----------|---------------------|
| 128MB    | AP-CF128ME3ER-ETNRK | 256MB    | AP-CF256ME3FR-ETNRK |
| 256MB    | AP-CF256ME3ER-ETNRK | 512MB    | AP-CF512ME3FR-ETNRK |
| 512MB    | AP-CF512ME3ER-ETNRK | 1GB      | AP-CF001GE3FR-ETNRK |
| 1GB      | AP-CF001GE3ER-ETNRK | 2GB      | AP-CF002GE3FR-ETNRK |
| 2GB      | AP-CF002GE3ER-ETNRK | 4GB      | AP-CF004GE3FR-ETNRK |
| 16GB     | AP-CF016GE3ER-ETNRK | 8GB      | AP-CF008GE3FR-ETNRK |

**Non-DMA & Non-Removable**

**Standard**

**High Speed**

| Capacity | Model Number          | Capacity | Model Number          |
|----------|-----------------------|----------|-----------------------|
| 128MB    | AP-CF128ME3ER-ETNDNRK | 256MB    | AP-CF256ME3FR-ETNDNRK |
| 256MB    | AP-CF256ME3ER-ETNDNRK | 512MB    | AP-CF512ME3FR-ETNDNRK |
| 512MB    | AP-CF512ME3ER-ETNDNRK | 1GB      | AP-CF001GE3FR-ETNDNRK |
| 1GB      | AP-CF001GE3ER-ETNDNRK | 2GB      | AP-CF002GE3FR-ETNDNRK |
| 2GB      | AP-CF002GE3ER-ETNDNRK | 4GB      | AP-CF004GE3FR-ETNDNRK |
| 16GB     | AP-CF016GE3ER-ETNDNRK | 8GB      | AP-CF008GE3FR-ETNDNRK |

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## Revision History

| Revision | Description      | Date        |
|----------|------------------|-------------|
| 1.0      | Official release | Mar 8, 2011 |

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