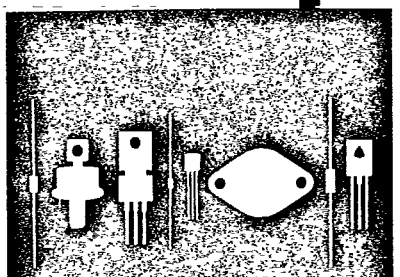
Central Semiconductor Corp.
Central Semiconductor Corp.
Central Semiconductor Corp.
Central™ Semiconductor Corp.
145 Adams Avenue
Hauppauge, New York 11788



CQ39AS
CQ39BS
CQ39DS
CQ39MS

D

TRIAC
4.0 AMPS
100 THRU 600 VOLTS

JEDEC TO-39 CASE

DESCRIPTION

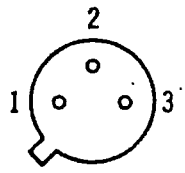
The CENTRAL SEMICONDUCTOR CQ39AS Series is a Hermetically Sealed Silicon Triac designed for full wave AC Control applications featuring gate triggering in all four (4) quadrants.

MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

	SYMBOL	CQ39AS	CQ39BS	CQ39DS	CQ39MS	UNIT
Peak Repetitive Off-Stage Voltage	V_{DRM}	100	200	400	600	V
RMS On-State Current (T_C=80°C)	$I_{T(RMS)}$		4.0			A
Peak One Cycle Surge(10ms.)	I_{TSM}		35			A
Peak Gate Current	I_{GM}		1.0			A
Average Gate Power Dissipation	$P_{G(AV)}$		0.2			W
Operating and Storage Junction Temperature	T_J,Tstg		-65 TO +200			°C

ELECTRICAL CHARACTERISTICS(T_C=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRM}	V_D=Rated V_{DRM}, T_C=100°C			1.5	mA
V_{TM}	I_T=5.0A			1.7	V
I_{GT}	V_D=12V, QUAD I (MT2+, G+)			5.0	mA
I_{GT}	V_D=12V, QUAD II (MT2+, G-)			5.0	mA
I_{GT}	V_D=12V, QUAD III(MT2-, G-)			5.0	mA
I_{GT}	V_D=12V, QUAD IV (MT2-, G+)			5.0	mA
V_{GT}*	V_D=12V			1.8	V
I_H	V_D=12V			10	mA
dv/dt	Exponential Rise to VD=V_{DRM}, T_C=100°C		10		v/µs



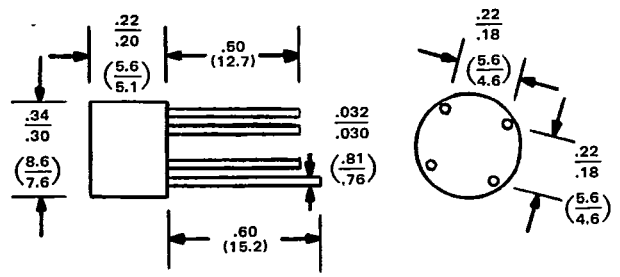
LEAD CODE:

PIN 1. MT1
2. GATE
3. MT2

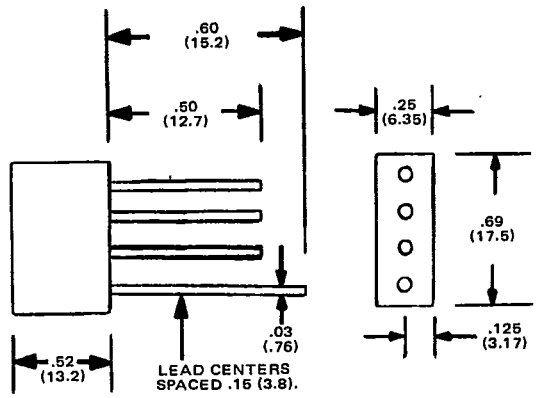
*IN ALL FOUR QUADRANTS

CASE OUTLINE DRAWINGS

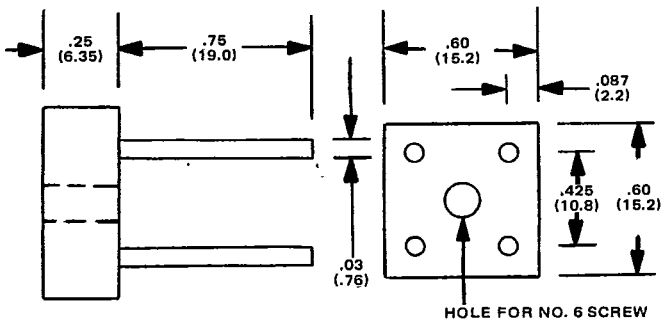
D



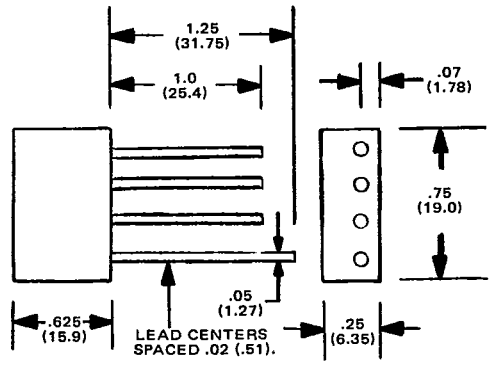
CASE A CBR1 *Series*
CBR2 *Series*



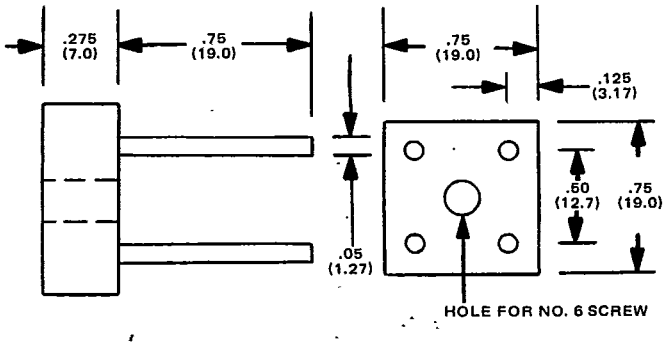
CASE B CBR1-L *Series*
CBR2-L *Series*



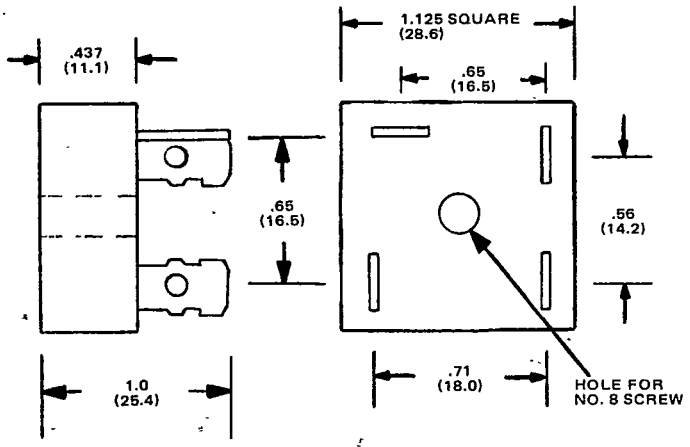
CASE C CBR3-P *Series*



CASE D CBR4-L *Series*



CASE E CBR8 *Series*



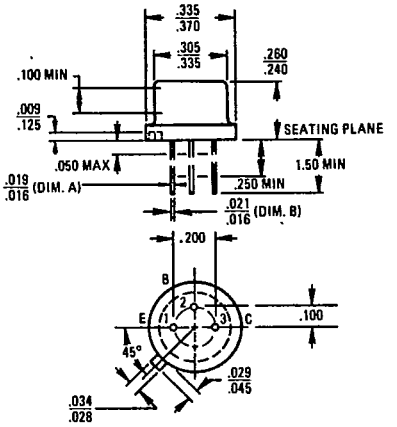
CASE F CBR10 *Series*, CBR25 *Series*
CBR12 *Series*, CBR30 *Series*

All Dimensions in Inches *(Millimeters)*
Drawings Not To Scale

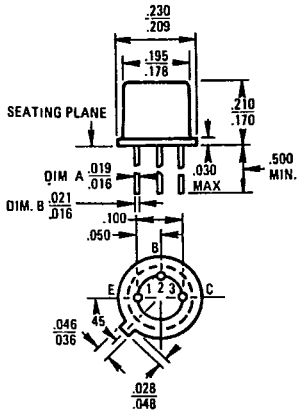
MECHANICAL OUTLINE DRAWINGS

D

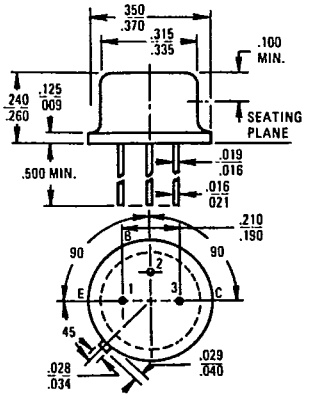
TO-5



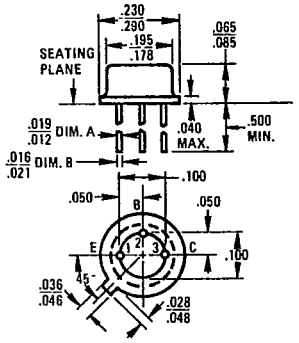
TO-18



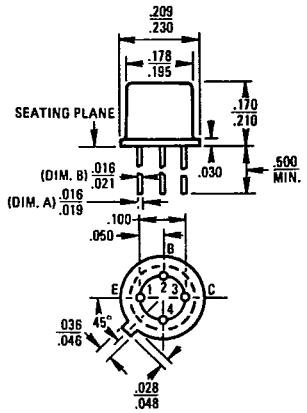
TO-39



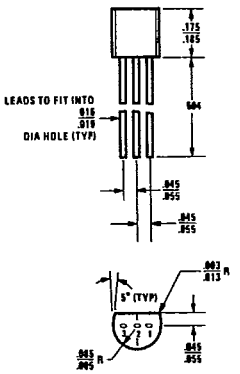
TO-46



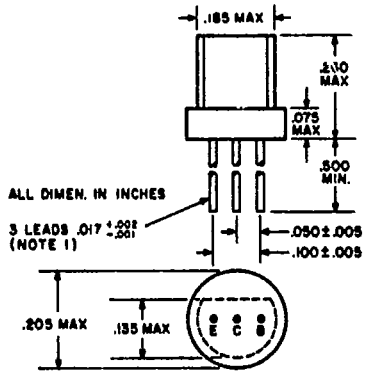
TO-72



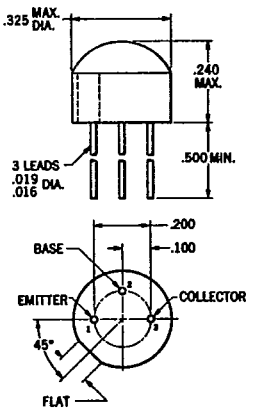
TO-92



TO-98



TO-105



TO-106