

Automotive-grade N-channel 40 V, 1.46 mΩ typ., 120 A STripFET™ F6 Power MOSFETs in I²PAK and TO-220 packages

Datasheet - production data

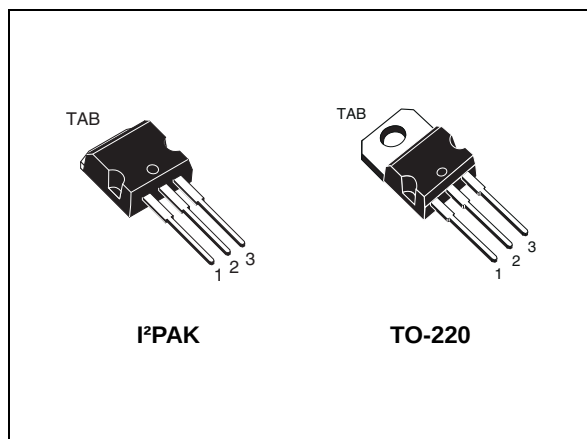
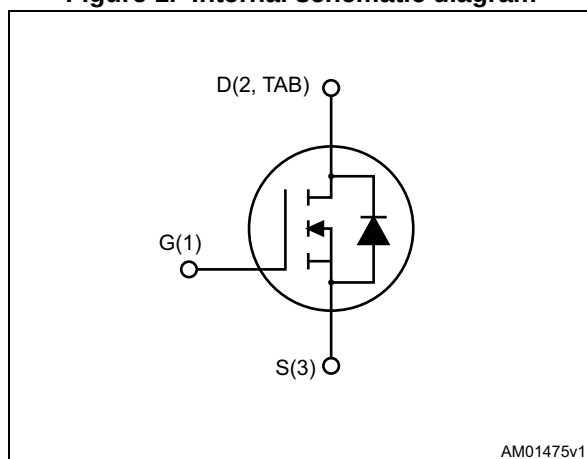


Figure 1. Internal schematic diagram



Features

Order codes	V _{DS}	R _{DS(on)} max.	I _D
STI360N4F6	40 V	1.8 mΩ	120 A
STP360N4F6			

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFETs exhibit very low R_{DS(on)} in all packages.

Table 1. Device summary

Order codes	Marking	Packages	Packing
STI360N4F6	360N4F6	I ² PAK	Tube
STP360N4F6		TO-220	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)(2)}$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	120	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	120	
$I_{DM}^{(1)}$	Drain current (pulsed)	480	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	300	W
T_{stg}	Storage temperature	- 55 to 175	$^{\circ}\text{C}$
T_j	Operating junction temperature		

1. Current limited by package.

2. Pulse width is limited by safe operating area.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.5	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	40			V
I_{DSS}	Zero gate voltage Drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 40\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 40\text{ V}$, $T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 0\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 60\text{ A}$		1.46	1.8	m Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	17800	-	pF
C_{oss}	Output capacitance		-	1750	-	
C_{rss}	Reverse transfer capacitance		-	1305	-	
Q_g	Total gate charge	$V_{DD} = 20\text{ V}$, $I_D = 120\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 14: Gate charge test circuit)	-	304	-	nC
Q_{gs}	Gate-source charge		-	96	-	
Q_{gd}	Gate-drain charge		-	87	-	

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$, $I_D = 60\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13: Switching times test circuit for resistive load and Figure 18: Switching time waveform)	-	64	-	ns
t_r	Rise time		-	182	-	
$t_{d(off)}$	Turn-off-delay time		-	240	-	
t_f	Fall time		-	130	-	

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		120	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		480	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 120\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 120\text{ A}$, $V_{DD} = 32\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_j = 25\text{ }^\circ\text{C}$ (see Figure 15: Test circuit for inductive load switching and diode recovery times)	-	44		ns
Q_{rr}	Reverse recovery charge		-	47		nC
I_{RRM}	Reverse recovery current		-	2.1		A

1. Current limited by package
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

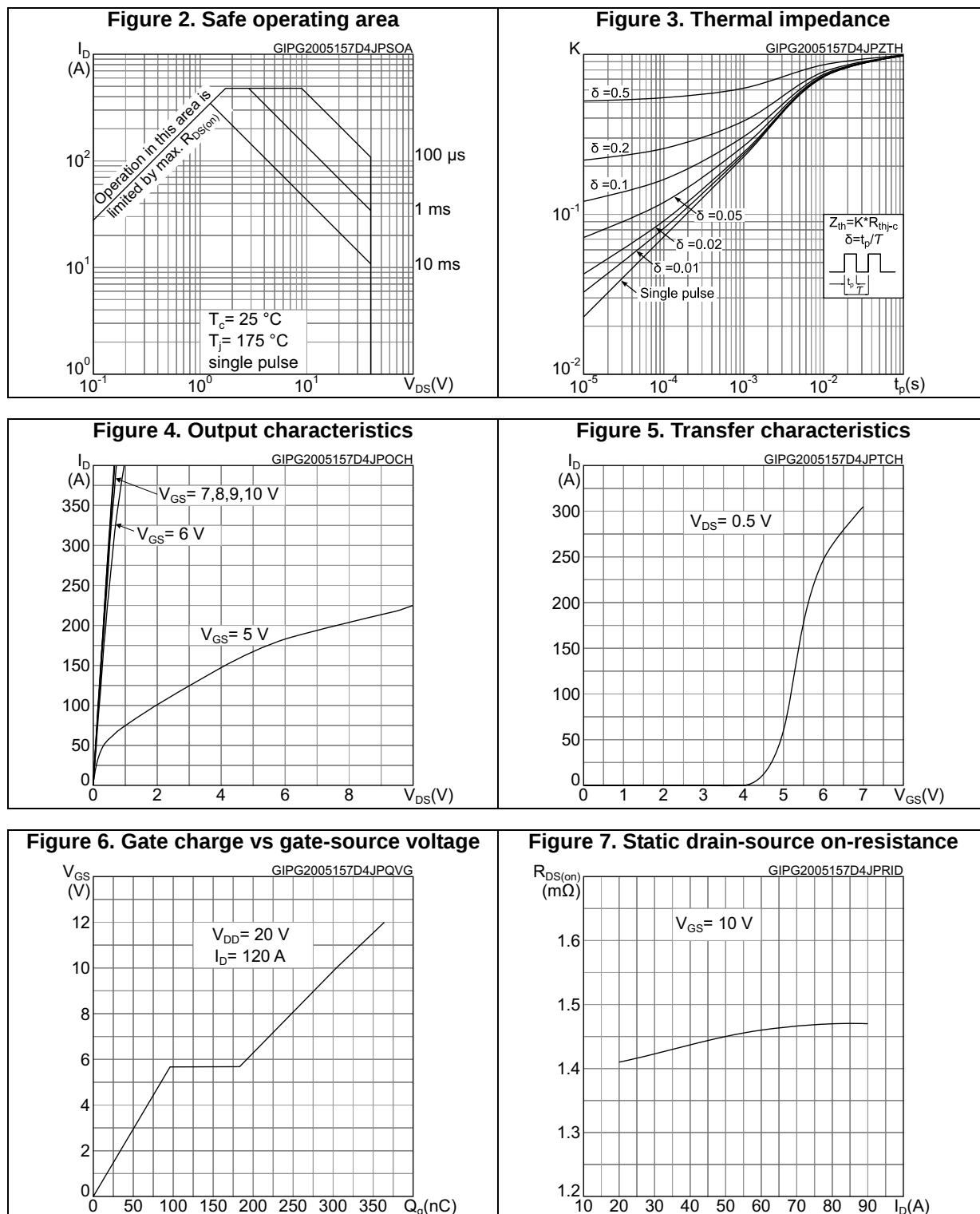


Figure 8. Capacitance variations

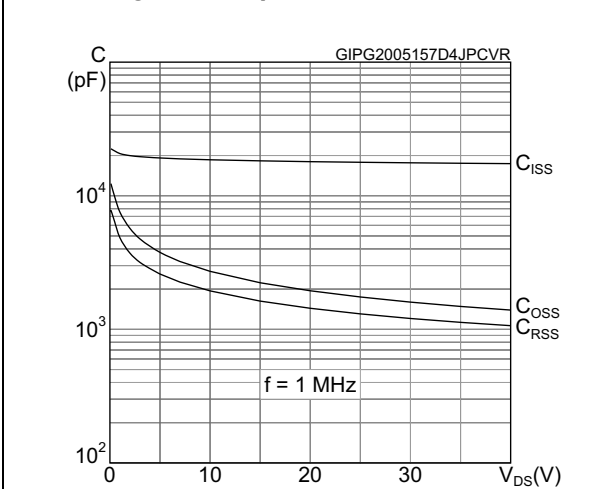


Figure 9. Normalized gate threshold voltage vs temperature

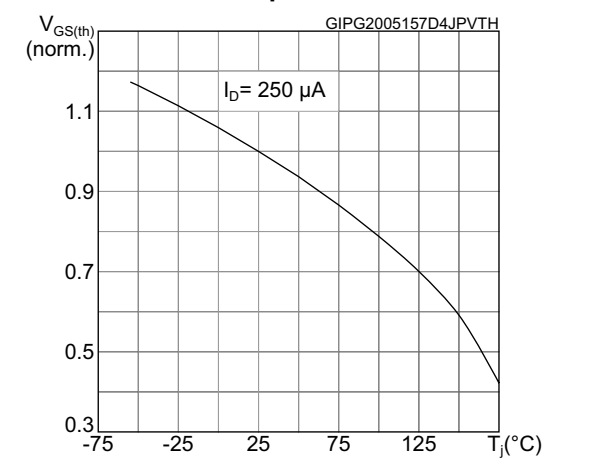


Figure 10. Normalized on-resistance vs temperature

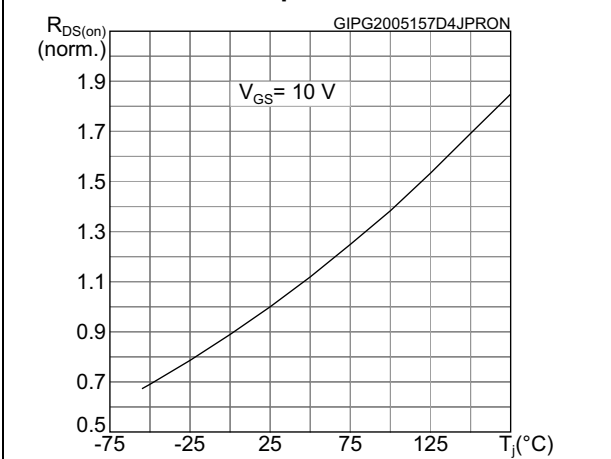


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

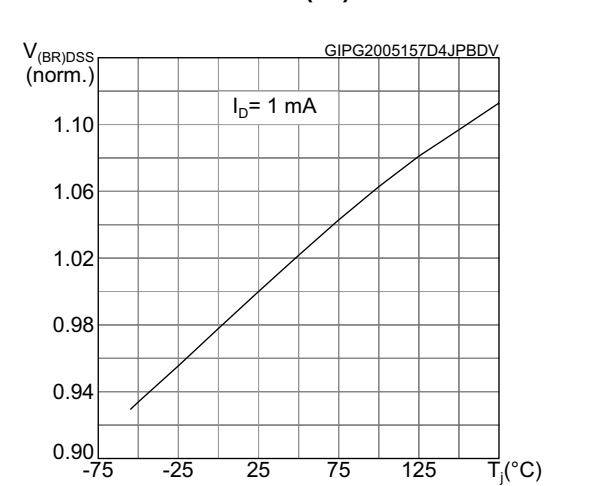
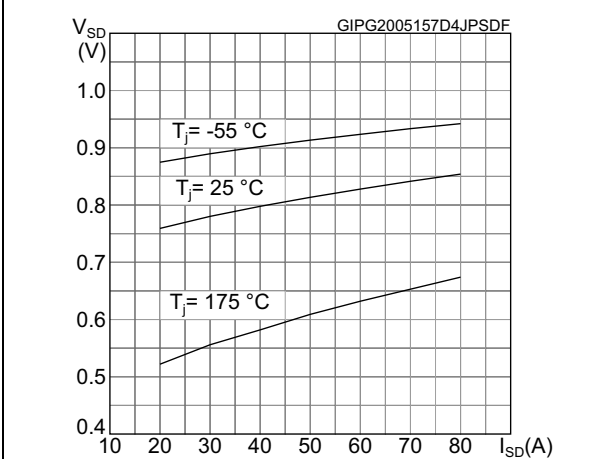
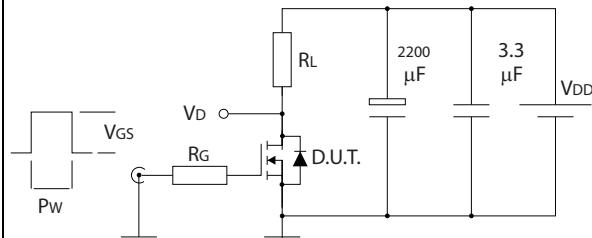


Figure 12. Source-drain diode forward characteristics



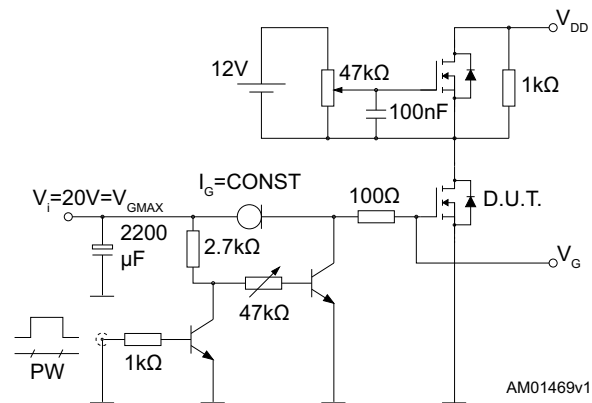
3 Test circuits

Figure 13. Switching times test circuit for resistive load



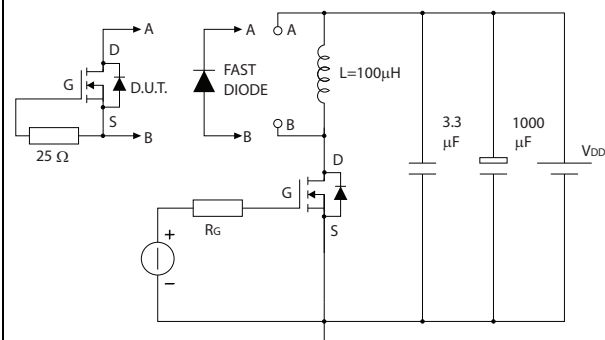
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Figure 14. Gate charge test circuit



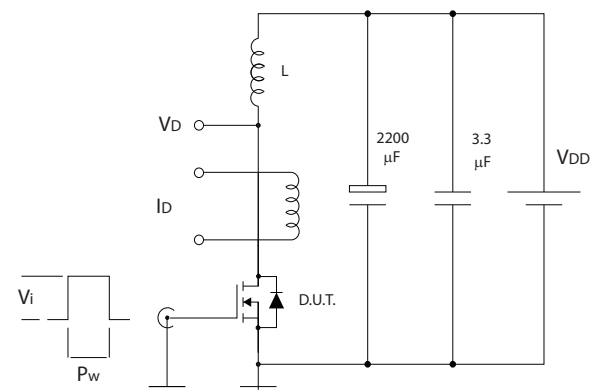
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Figure 15. Test circuit for inductive load switching and diode recovery times



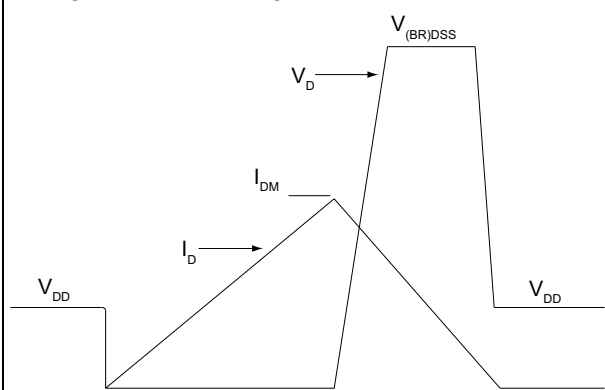
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Figure 16. Unclamped inductive load test circuit



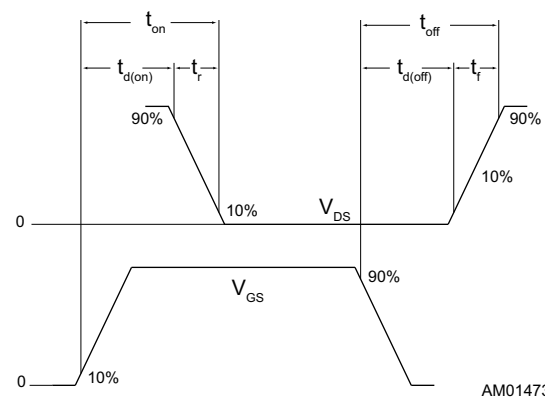
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Figure 17. Unclamped inductive waveform



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Figure 18. Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 I²PAK package information

Figure 19. I²PAK (TO-262) package outline

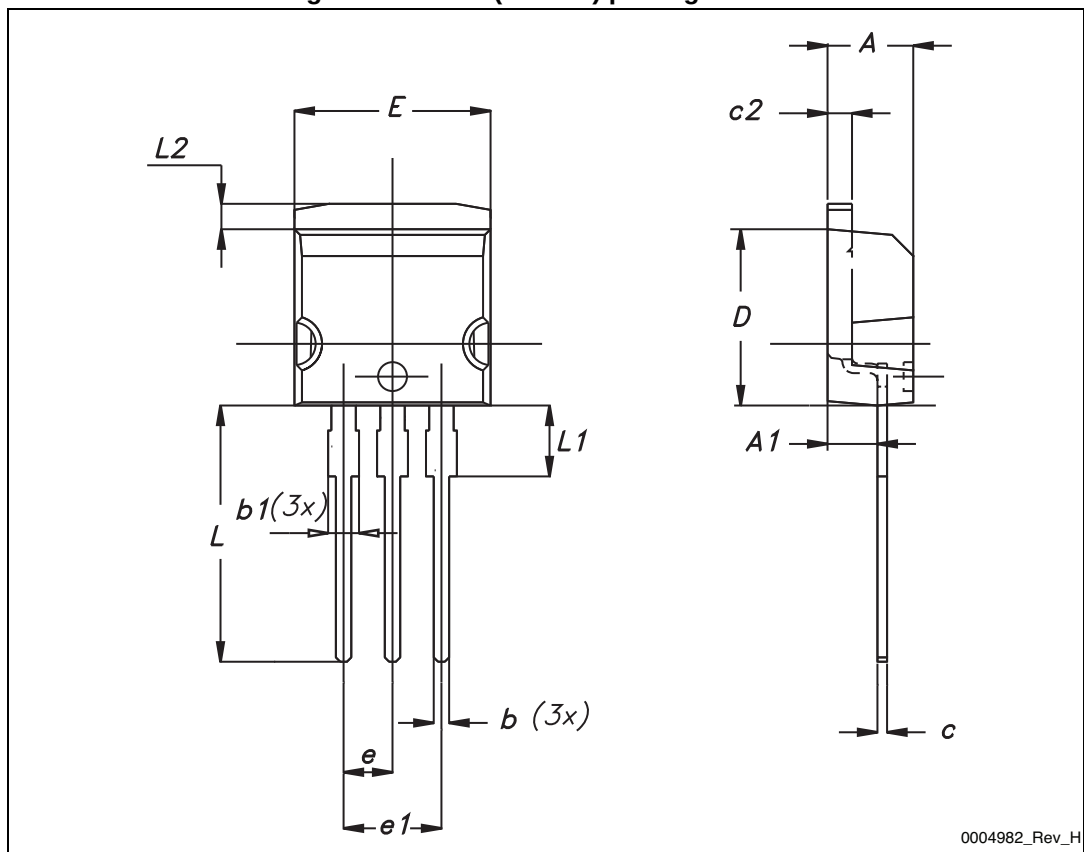


Table 8. I²PAK (TO-262) package mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

4.2 TO-220 package information

Figure 20. TO-220 type A package outline

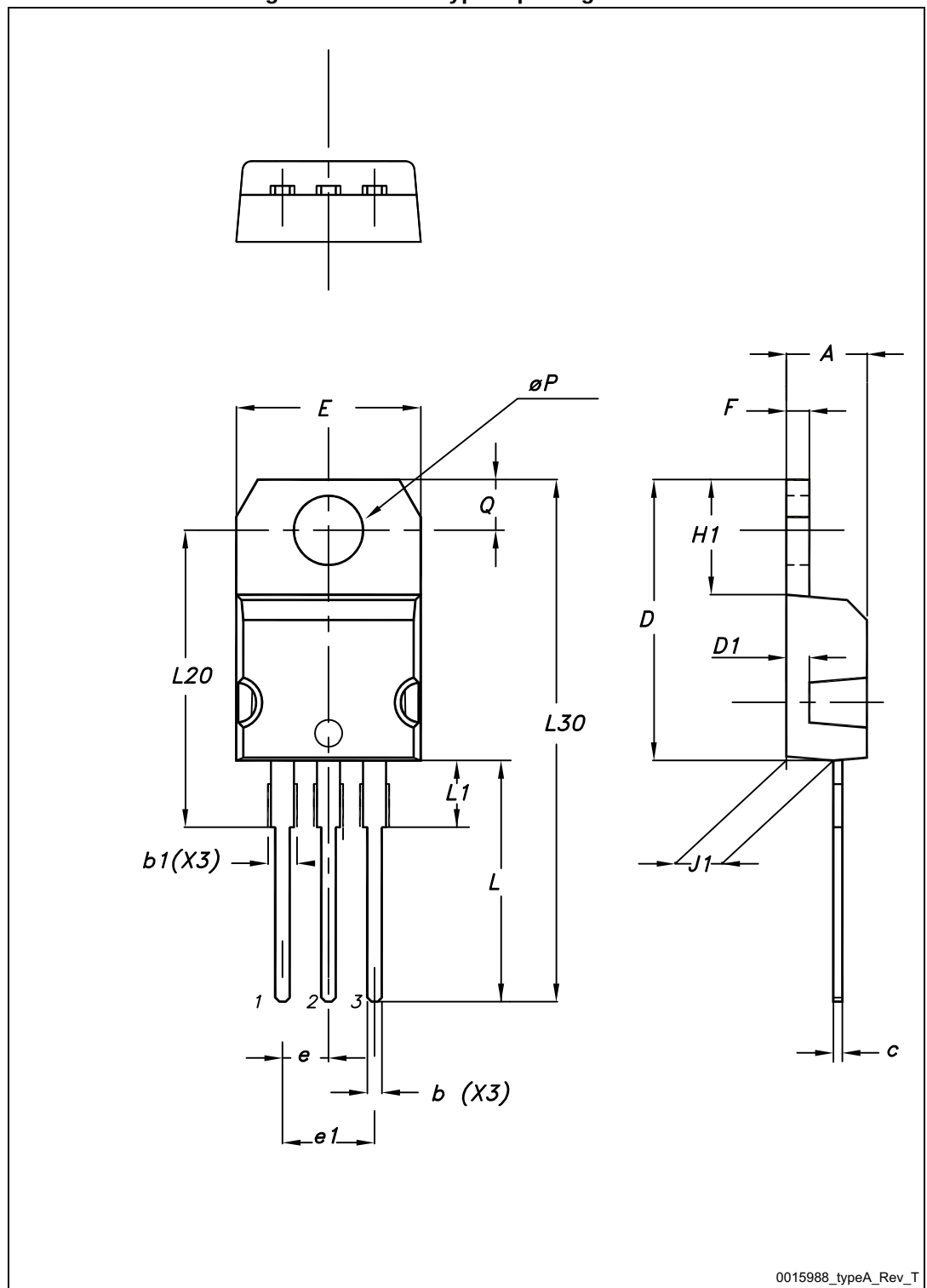


Table 9. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
08-Aug-2012	1	First release.
03-Dec-2015	2	Text and formatting changes throughout document Updated Section 1: Electrical ratings Updated Section 2: Electrical characteristics Added: Section 2.1: Electrical characteristics (curves) Added: Section 3: Test circuits

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