

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	-3.0*	—	0.8	V

* Pulse Width: 50ns, DC: $V_{IL} \text{ min} = -0.3\text{V}$ ■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, GND = 0V, $T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Conditions	HM6116LP-2			HM6116LP-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$ I_{LI} $	$V_{CC} = 5.5\text{V}$, $V_{IN} = \text{GND to } V_{CC}$	—	—	2	—	—	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}} = V_{IH}$ or $\overline{\text{OE}} = V_{IH}$, $V_{IO} = \text{GND to } V_{CC}$	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}} = V_{IL}$, $I_{IO} = 0\text{mA}$	—	35	70	—	30	60	mA
	I_{CC1}^{**}	$V_{IH} = 3.5\text{V}$, $V_{IL} = 0.6\text{V}$, $I_{IO} = 0\text{mA}$	—	30	—	—	25	—	mA
Average Operating Current	I_{CC1}	min. cycle, duty = 100%	—	35	70	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}} = V_{IH}$	—	4	12	—	4	12	mA
	I_{SB1}	$\overline{\text{CS}} \geq V_{CC} - 0.2\text{V}$, $V_{IO} \geq V_{CC} - 0.2\text{V}$ or $V_{IO} \leq 0.2\text{V}$	—	2	50	—	2	50	μA
Output Voltage	V_{OL}	$I_{OL} = 4\text{mA}$	—	—	0.4	—	—	—	V
		$I_{OL} = 2.1\text{mA}$	—	—	—	—	—	0.4	V
	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	—	—	2.4	—	—	V

* : $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

** : Reference Only

■ AC CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$)

● AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

● READ CYCLE

Item	Symbol	HM6116LP-2		HM6116LP-3		HM6116LP-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116LP-2		HM6116LP-3		HM6116LP-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{wc}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{cw}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{aw}	105	—	120	—	140	—	ns
Address Set Up Time	t_{as}	20	—	20	—	20	—	ns
Write Pulse Width	t_{wp}	70	—	90	—	120	—	ns
Write Recovery Time	t_{wr}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{onz}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{wnz}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{dw}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{dh}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{ow}	5	—	10	—	10	—	ns

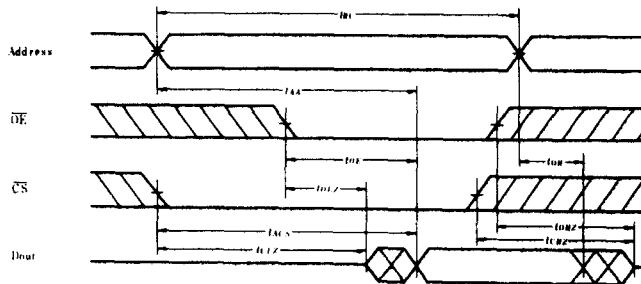
■ CAPACITANCE ($f=1\text{MHz}$, $T_a=25^\circ\text{C}$)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	$V_{in}=0\text{V}$	3	5	pF
Input/Output Capacitance	$C_{i/o}$	$V_{i/o}=0\text{V}$	5	7	pF

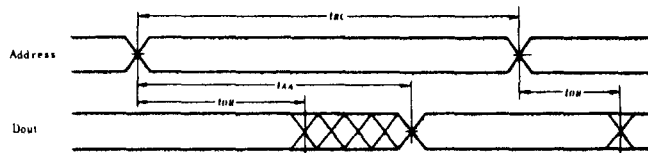
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

● Read Cycle (1) (1)



● Read Cycle (2) (1), (2), (4)

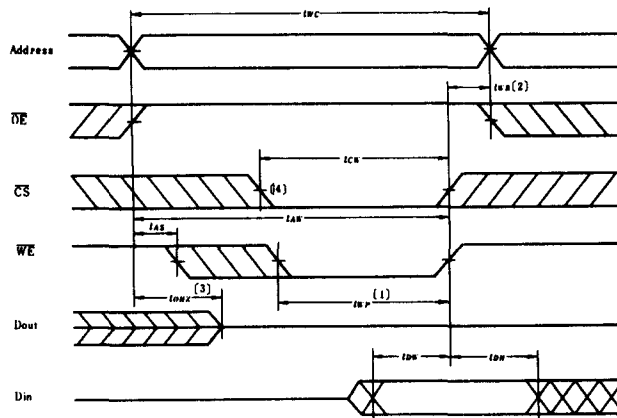


● Read Cycle (3) (1), (3), (4)

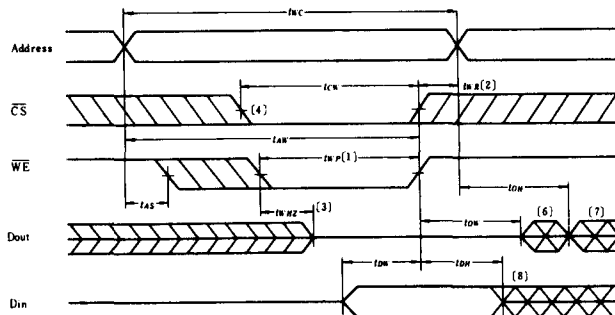


- NOTES: 1. $\overline{WE}$ is High for Read Cycle.
 2. Device is continuously selected, $\overline{CS} = V_{IL}$.
 3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
 4. $\overline{OE} = V_{IL}$.

● Write Cycle (1)



● Write Cycle (2) (5)



- NOTES: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$

transition, output remain in a high impedance state.

5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

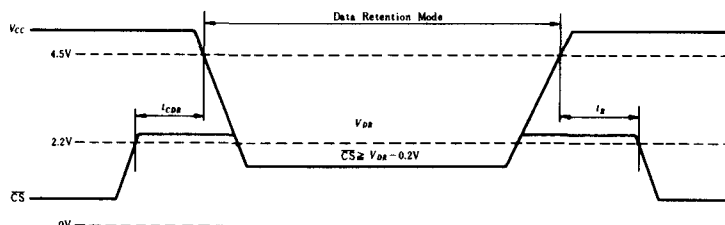
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$, $V_{IL} \geq V_{CC} - 0.2\text{V}$ or $V_{IL} \leq 0.2\text{V}$	2.0	—	—	V
Data Retention Current	I_{CCDR}^*	$V_{CC} = 3.0\text{V}$, $\overline{CS} \geq 2.8\text{V}$, $V_{IL} \geq 2.8\text{V}$ or $V_{IL} \leq 0.2\text{V}$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}^{**}	—	—	ns

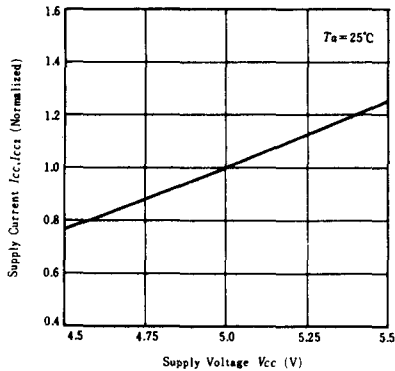
* 10 μA max at $T_a = 0^\circ\text{C}$ to $+40^\circ\text{C}$, V_{IL} min = -0.3V

** t_{RC} = Read Cycle Time.

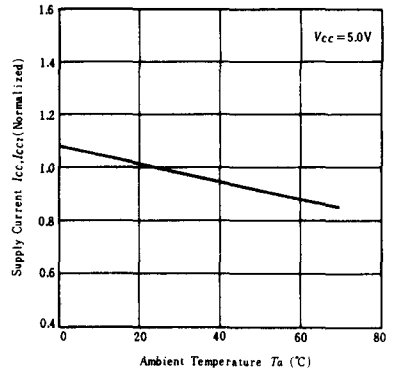
● Low V_{CC} Data Retention Waveform



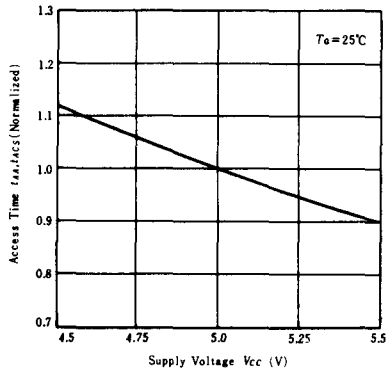
**SUPPLY CURRENT vs.
SUPPLY VOLTAGE**



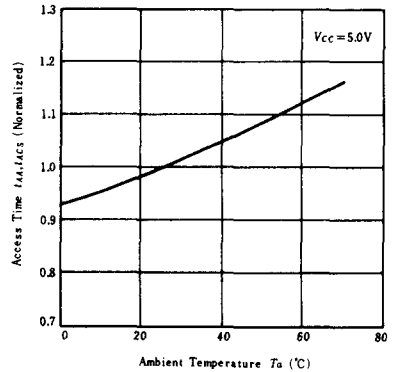
**SUPPLY CURRENT vs.
AMBIENT TEMPERATURE**



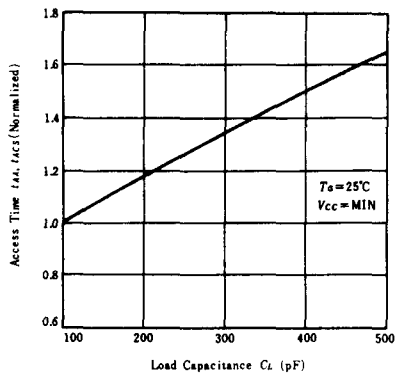
**ACCESS TIME vs.
SUPPLY VOLTAGE**



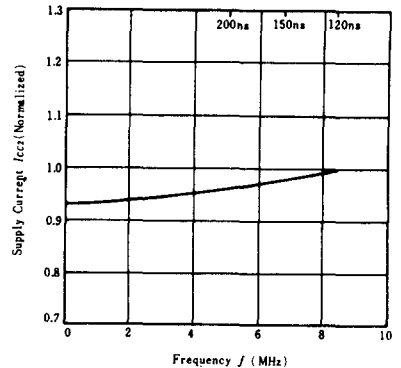
**ACCESS TIME vs.
AMBIENT TEMPERATURE**



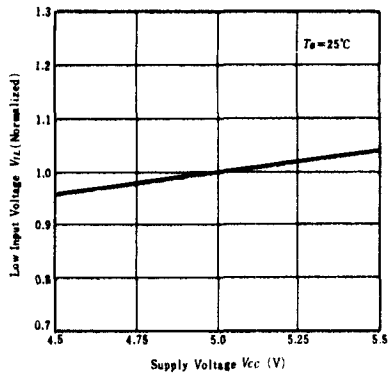
**ACCESS TIME vs.
LOAD CAPACITANCE**



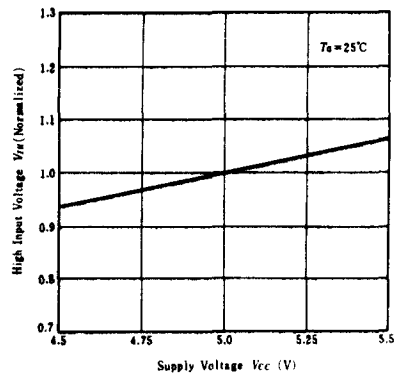
**SUPPLY CURRENT vs.
FREQUENCY**



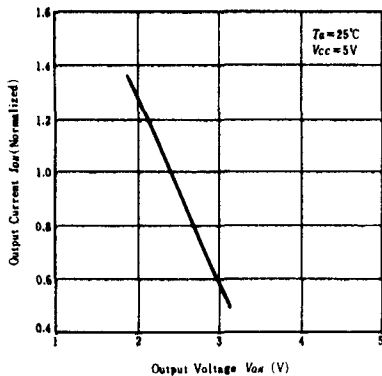
**LOW INPUT VOLTAGE vs.
SUPPLY VOLTAGE**



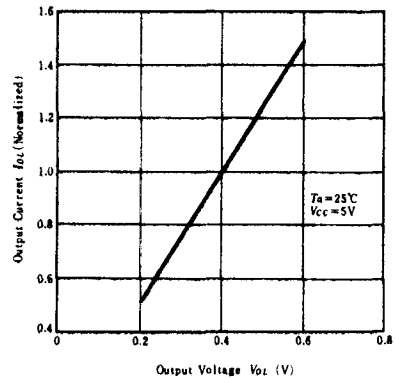
**HIGH INPUT VOLTAGE vs.
SUPPLY VOLTAGE**



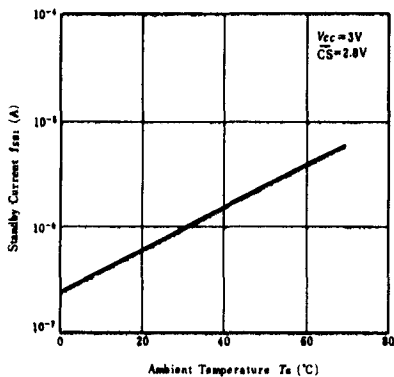
**OUTPUT CURRENT vs.
OUTPUT VOLTAGE**



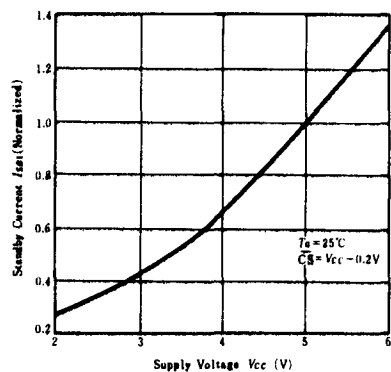
**OUTPUT CURRENT vs.
OUTPUT VOLTAGE**



**STANDBY CURRENT vs.
AMBIENT TEMPERATURE**



**STANDBY CURRENT vs.
SUPPLY VOLTAGE**



**STANDBY CURRENT vs.
INPUT VOLTAGE**