

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74VHCT125AF, TC74VHCT125AFN, TC74VHCT125AFT, TC74VHCT125AFK TC74VHCT126AF, TC74VHCT126AFN, TC74VHCT126AFT, TC74VHCT126AFK

TC74VHCT125AF/AFN/AFT/AFK Quad Bus Buffer

TC74VHCT126AF/AFN/AFT/AFK Quad Bus Buffer

Note: xxxFN (JEDEC SOP) is not available in Japan.

The TC74VHCT125A/126A are high speed CMOS QUAD BUS BUFFERS fabricated with silicon gate CMOS technology.

They achieve the high speed operation similar to equivalent Bipolar Shottky TTL while maintaining the CMOS low power dissipation.

The TC74VHCT125A requires the 3-state control input  $\bar{G}$  to be set high to place the output into the high impedance state, whereas the TC74VHCT126A requires the control input G to be set low to place the output into high impedance.

The input voltage are compatible with TTL output voltage.

This device may be used as a level converter for interfacing 3.3 V to 5 V system.

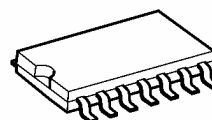
Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output <sup>(Note)</sup> pins without regard to the supply voltage. There structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

Note:  $V_{CC} = 0\text{ V}$

### Features

- High speed:  $t_{pd} = 3.8\text{ ns (typ.)}$  at  $V_{CC} = 5\text{ V}$
- Low power dissipation:  $I_{CC} = 4\text{ }\mu\text{A (max)}$  at  $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs:  $V_{IL} = 0.8\text{ V (max)}$   
 $V_{IH} = 2.0\text{ V (min)}$
- Power down protection is provided on all inputs and outputs.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Low noise:  $V_{OLP} = 0.8\text{ V (max)}$
- Pin and function compatible with the 74 series (74AC/HC/F/ALS/LS etc.) 125/126 types.

TC74VHCT125AF, TC74VHCT126AF



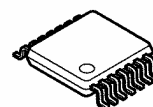
SOP14-P-300-1.27A

TC74VHCT125AFN, TC74VHCT126AFN



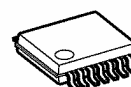
SOL14-P-150-1.27

TC74VHCT125AFT, TC74VHCT126AFT



TSSOP14-P-0044-0.65A

TC74VHCT125AFK, TC74VHCT126AFK

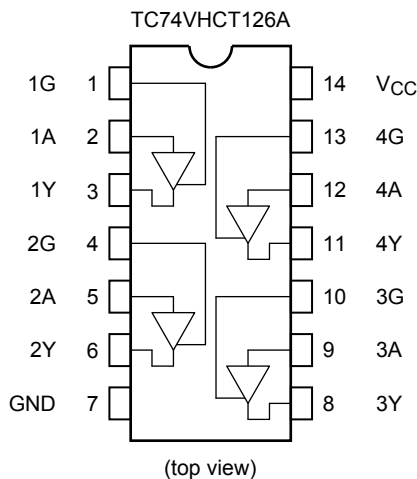
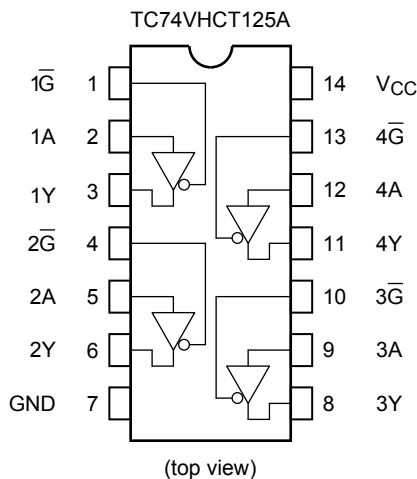


VSSOP14-P-0030-0.50

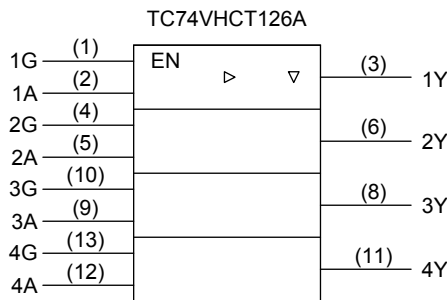
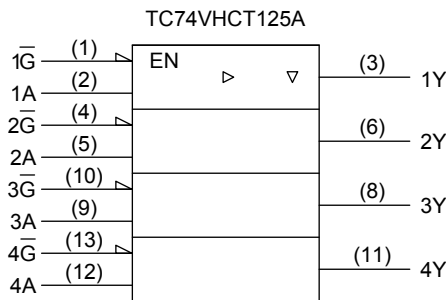
### Weight

SOP14-P-300-1.27A	: 0.18 g (typ.)
SOL14-P-150-1.27	: 0.12 g (typ.)
TSSOP14-P-0044-0.65A	: 0.06 g (typ.)
VSSOP14-P-0030-0.50	: 0.02 g (typ.)

Pin Assignment



IEC Logic Symbol



Truth Table

TC74VHCT125A

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

X: Don't care

Z: High impedance

TC74VHCT126A

Inputs		Output
G	A	Y
L	X	Z
H	L	L
H	H	H

X: Don't care

Z: High impedance

**Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to 7.0	V
DC output voltage	$V_{OUT}$	-0.5 to 7.0 (Note 2)	V
		-0.5 to $V_{CC} + 0.5$ (Note 3)	
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	$\pm 20$ (Note 4)	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in off-state

Note 3: High or low state.  $I_{OUT}$  absolute maximum rating must be observed.

Note 4:  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$

**Operating Ranges (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	4.5 to 5.5	V
Input voltage	$V_{IN}$	0 to 5.5	V
Output voltage	$V_{OUT}$	0 to 5.5 (Note 2)	V
		0 to $V_{CC}$ (Note 3)	
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	$dt/dv$	0 to 20	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or  $GND$ .

Note 2: Output in off-state

Note 3: High or low state

## Electrical Characteristics

## DC Characteristics

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to 85°C		Unit
				Min	Typ.	Max	Min	Max	
High-level input voltage	V <sub>IH</sub>	—	4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V <sub>IL</sub>	—	4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 µA	4.5	4.40	4.50	—	4.40	V
			I <sub>OH</sub> = -8 mA	4.5	3.94	—	—	3.80	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 µA	4.5	—	0.0	0.1	—	V
			I <sub>OL</sub> = 8 mA	4.5	—	—	0.36	—	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5	—	—	±0.1	—	±1.0	µA
3-state output off-state current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	5.5	—	—	±0.25	—	±2.50	µA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	4.0	—	40.0	µA
	I <sub>CC(T)</sub>	Per input: V <sub>IN</sub> = 3.4 V Other input: V <sub>CC</sub> or GND	5.5	—	—	1.35	—	1.50	mA
Output leakage current	I <sub>OPD</sub>	V <sub>OUT</sub> = 5.5 V	0	—	—	0.5	—	5.0	µA

AC Characteristics (input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Ta = 25°C			Ta = -40 to 85°C		Unit
					Min	Typ.	Max	Min	Max	
Propagation delay time	t <sub>pLH</sub>	—	5.0 ± 0.5	15	—	3.8	5.5	1.0	6.5	ns
	t <sub>pHL</sub>			50	—	5.3	7.5	1.0	8.5	
Output enable time	t <sub>pZL</sub>	R <sub>L</sub> = 1 kΩ	5.0 ± 0.5	15	—	3.6	5.1	1.0	6.0	ns
	t <sub>pZH</sub>			50	—	5.1	7.1	1.0	8.0	
Output disable time	t <sub>pLZ</sub>	R <sub>L</sub> = 1 kΩ	5.0 ± 0.5	50	—	6.1	8.8	1.0	10.0	ns
	t <sub>pHZ</sub>									
Output to output skew	t <sub>osLH</sub>	(Note 1)	5.0 ± 0.5	50	—	—	1.0	—	1.0	ns
	t <sub>osHL</sub>									
Input capacitance	C <sub>IN</sub>	—	—	—	—	4	10	—	10	pF
Output capacitance	C <sub>OUT</sub>	—	—	—	—	6	—	—	—	pF
Power dissipation capacitance	C <sub>PD</sub> (Note 2)	TC74VHCT125A	—	—	—	14	—	—	—	pF
		TC74VHCT126A	—	—	—	15	—	—	—	

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$$

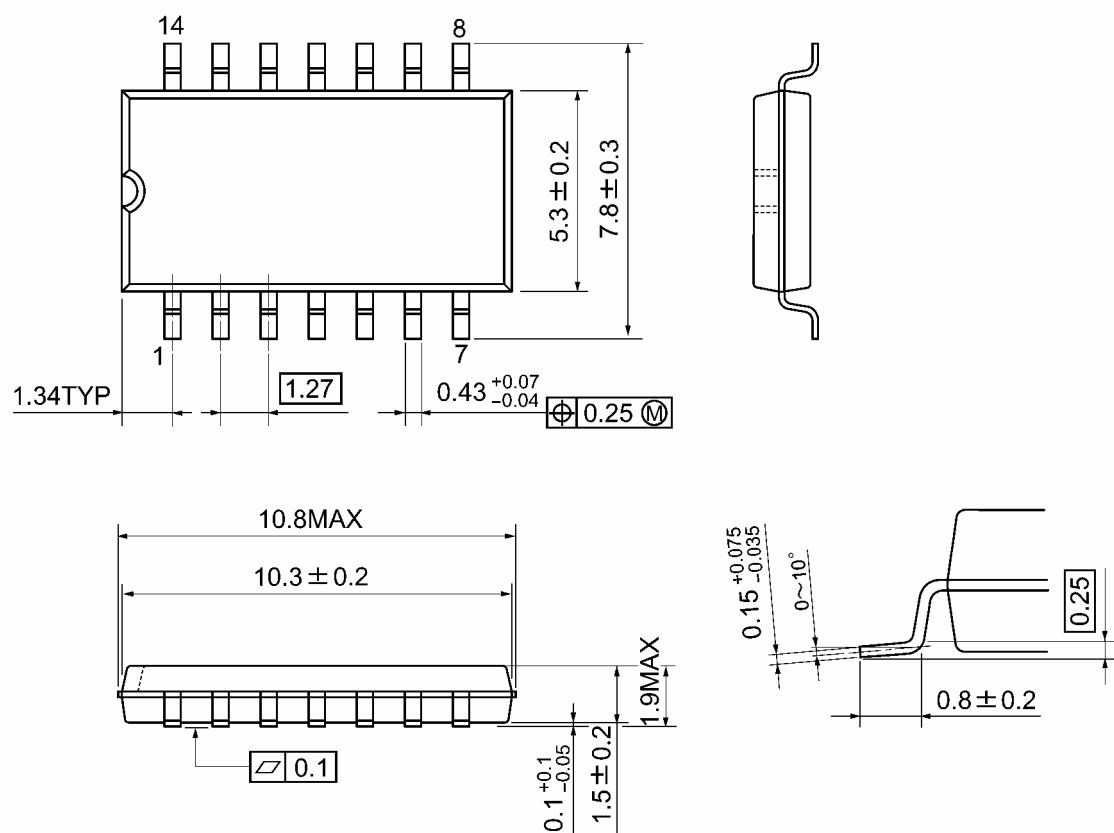
Noise Characteristics (input:  $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V <sub>CC</sub> (V)	Typ.	Limit	
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	0.5	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	−0.5	−0.8	V
Minimum high level dynamic input voltage	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0	—	2.0	V
Maximum low level dynamic input voltage	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	—	0.8	V

## Package Dimensions

SOP14-P-300-1.27A

Unit: mm

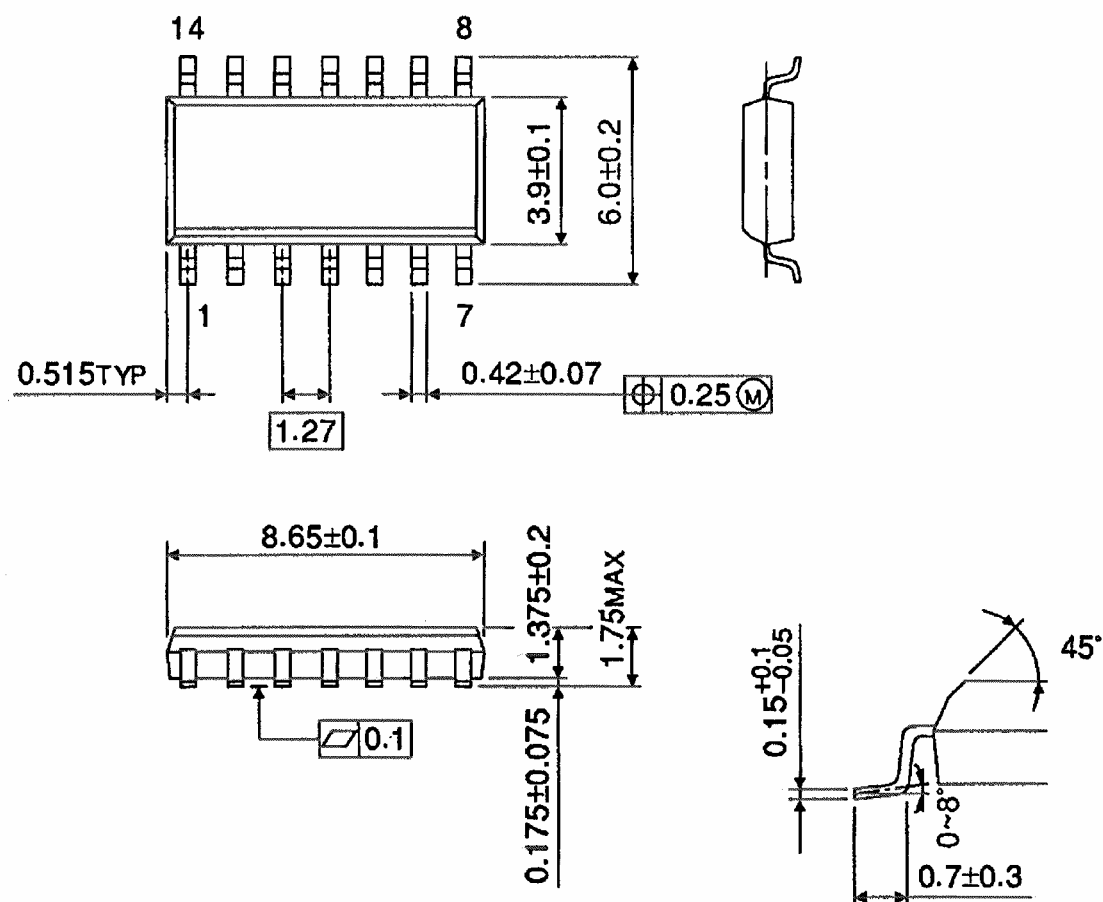


Weight: 0.18 g (typ.)

## Package Dimensions (Note)

SOL14-P-150-1.27

Unit : mm

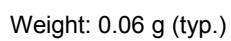


Note: This package is not available in Japan.

Weight: 0.12 g (typ.)

## TSSOP14-P-0044-0.65A

Unit: mm

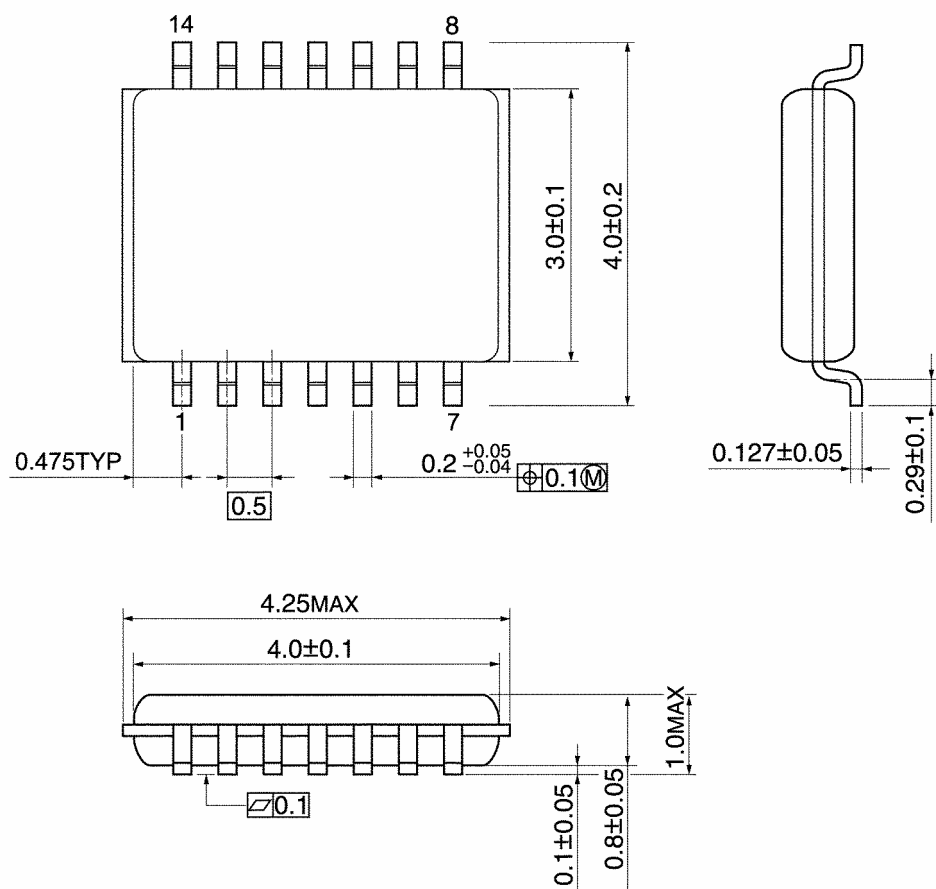




## Package Dimensions

VSSOP14-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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20070701-EN GENERAL

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