

# S30ML-P ORNAND™ Flash Family

**S30ML512P, S30ML256P, S30ML128P**

**512 Megabit, 256 Megabit, 128 Megabit  
3.0-Volt NAND Interface Flash Memory  
featuring MirrorBit® Technology**

***Data Sheet*** (Advance Information)

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3.0-Volt NAND Interface Flash Memory

featuring MirrorBit® Technology



*Data Sheet (Advance Information)*

## Distinctive Characteristics

- **Single power supply operation**
  - Full voltage range: 2.7 to 3.6 volt read, erase, and program operations
- **Manufactured on 90 nm MirrorBit process technology**
- **x8 and x16 Bus width**
- **Page and block sizes**
  - Page Size of 528 bytes (512 bytes for user area and 16 bytes for spare area)
  - Number of Blocks
    - 512Mb: 128 blocks
    - 256Mb: 64 blocks
    - 128Mb: 32 blocks
  - Block Size
    - x8 device block size = (512K + 16K) bytes
    - x16 device block size = (256K + 8K) words
- **Compatibility with NAND Flash I/O**
  - Provides pinout and command set compatibility with single-power supply NAND flash
- **100,000 program/erase cycles per sector typical**
- **10-Year data retention typical**
- **Industrial operating temperature range (–40°C to +85°C)**
- **48-pin standard pinout TSOP**
- **Devices with < 2% invalid blocks (requires ECC capable of correcting 1 bit per 512 Bytes)**

### Optional

- **100% valid blocks**
- **Enhanced Versatile I/O™ Control**
  - All input and output levels (address, control and I/O levels) are determined by voltage on V<sub>IO</sub> input. V<sub>IO</sub> range is 1.7 to V<sub>CC</sub>

## Performance Characteristics

| Read Access Times (Maximum) |             |       |
|-----------------------------|-------------|-------|
| Full Page Random Access     |             | 9 µs  |
| Serial Read                 | x8 devices  | 30 ns |
|                             | x16 devices | 50 ns |

| Current Consumption (Typical) |       |
|-------------------------------|-------|
| Read Current                  | 35 mA |
| Erase Current                 | 31 mA |
| Program Current               | 31 mA |
| Standby Current               | 10 µA |

| Program and Erase Performance (Typical) |        |
|-----------------------------------------|--------|
| Page Program Time                       | 180 µs |
| Block Erase Time                        | 150 ms |

### Legend

*b = bit, B = Byte, K = 1024, M = 1048576*

## General Description

The S30ML-P ORNAND™ Flash Family family consists of 3.0-volt, single-power-supply Flash memory devices that have memory arrays organized as shown in the following tables.

| S30ML-P Device Organization |         |         |         |        |
|-----------------------------|---------|---------|---------|--------|
| Device Name                 | Density | Rows    | Columns | Blocks |
| S30ML512P                   | 512 Mb  | 131,072 | 528     | 128    |
| S30ML256P                   | 256 Mb  | 65,536  | 528     | 64     |
| S30ML128P                   | 128 Mb  | 32,768  | 528     | 32     |

| S30ML-P Block & Page Divisions |                                                     |                                                    |
|--------------------------------|-----------------------------------------------------|----------------------------------------------------|
| Division                       | x8 Devices                                          | x16 Devices                                        |
| Page                           | 528 bytes (512-byte main area + 16-byte spare area) | 264 words (256-word main area + 8-word spare area) |
| Block                          | 1024 pages                                          |                                                    |

S30ML-P ORNAND™ Flash Family devices have a Static Page Register that allows program and read data to be transferred between the static page register and the memory cell array in whole-page increments (528 bytes for x8 devices and 264 words for x16 devices). The erase operation is implemented in block increments.

S30ML-P ORNAND™ Flash Family devices use I/O pins to serially shift command, address, or data into the device, and data or status out of the device. These serial-type memory devices are well suited for shadowing applications where the contents of the Flash memory is copy straight into a random access memory with the code executed out of random access memory. S30ML-P devices are not recommended for applications where code is executed directly out of the flash memory, as jump and branch microcode instructions require the fast read access characteristics provided by NOR Flash devices. Contact a Spansion representative for more information on the complete line of Spansion products.

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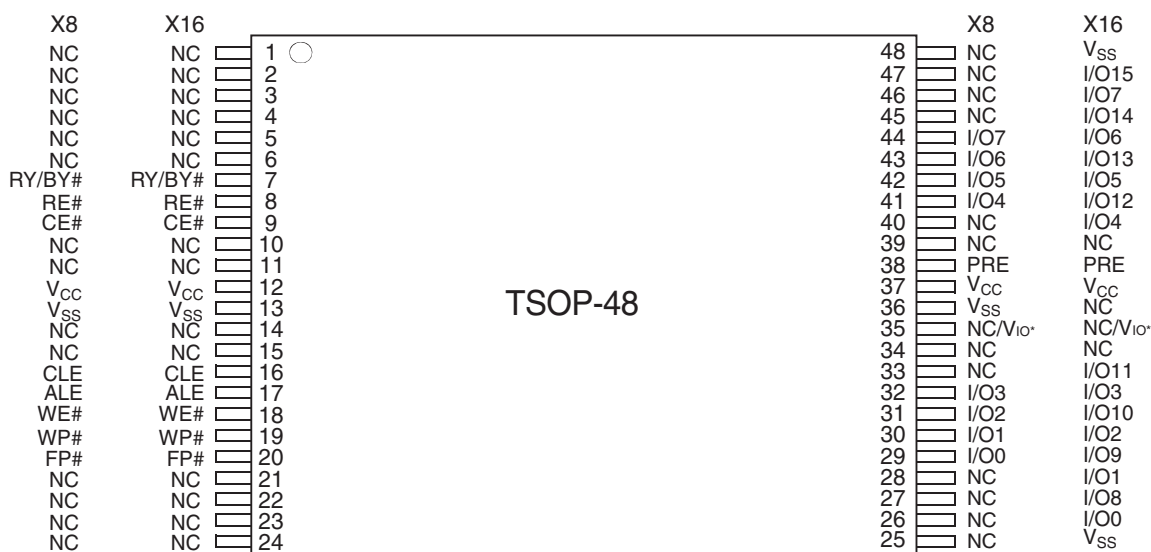
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## 1. Connection Diagrams

### 1.1 48-pin TSOP Connections

Figure 1.1 48-pin TSOP

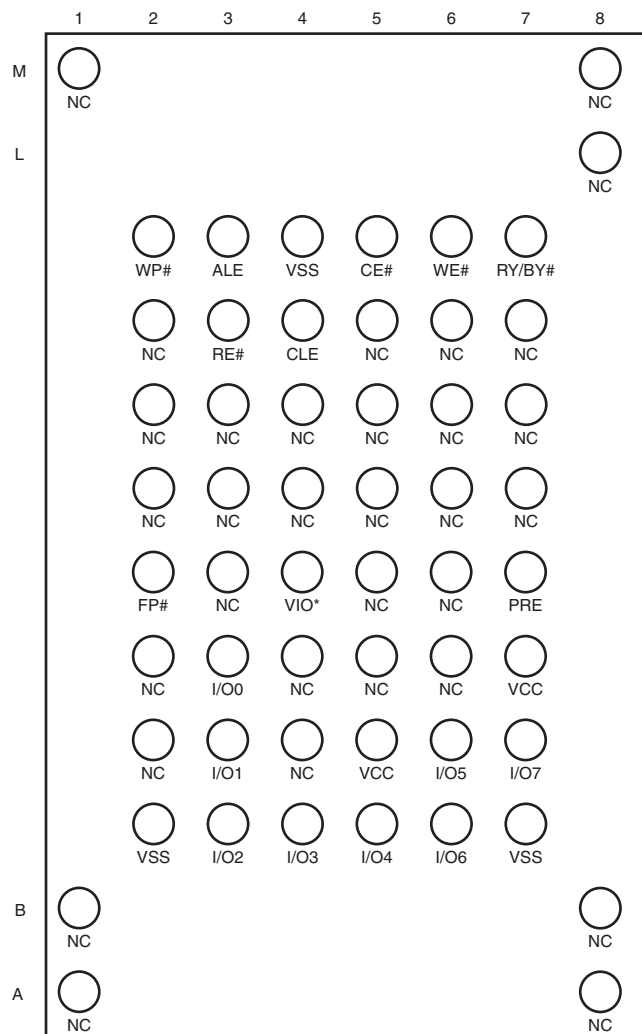


**Note**

Pin 35 is No Connect. If Enhanced Versatile I/O™ Control is needed, pin 35 is used as the V<sub>IO</sub> pin for both x 8 and x 16 modes through different OPN offering.

## 1.2 55-Ball FBGA Connections

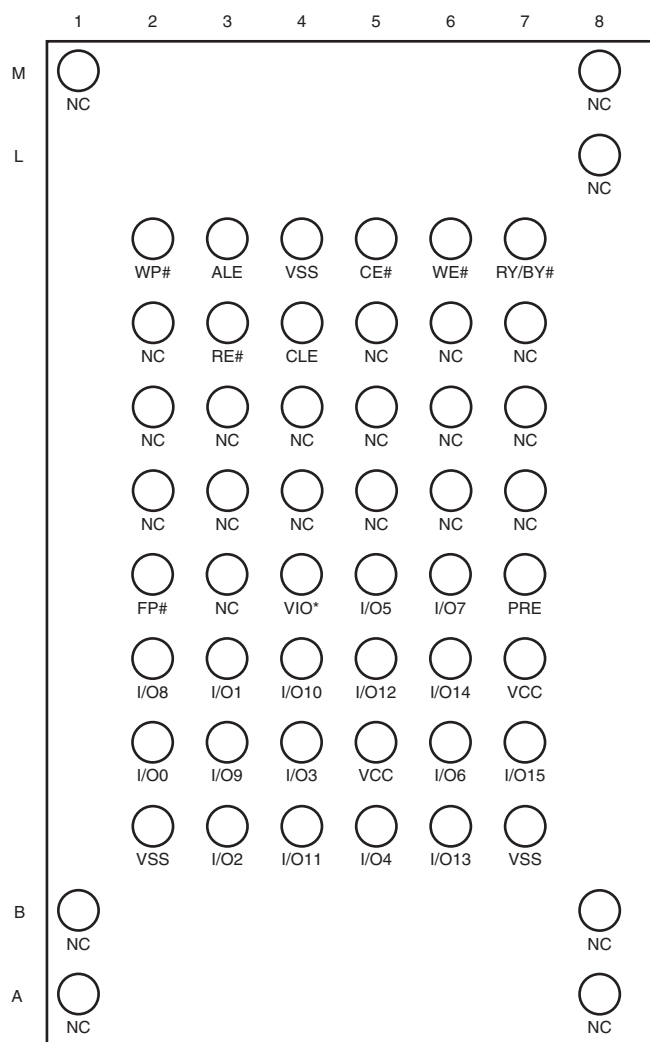
**Figure 1.2** 55-Ball FBGA Connections - x8



**Note**

Ball F4 is No Connect. If Enhanced Versatile I/O™ Control is needed, ball F4 is used as the VIO pin for both x8 and x16 modes through different OPN offerings.

**Figure 1.3** 55-Ball FBGA Connections - x16



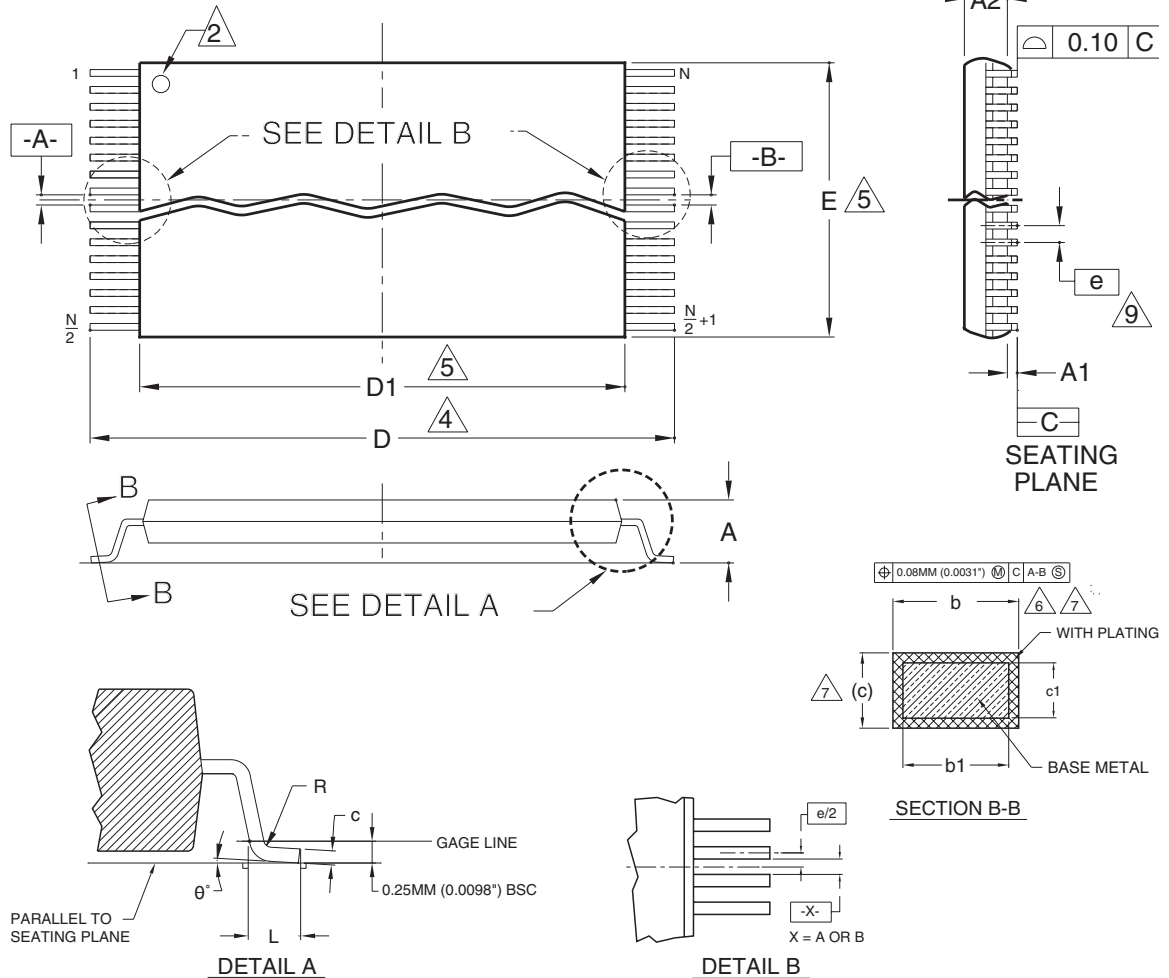
**Note**

Ball F4 is No Connect. If Enhanced Versatile I/O™ Control is needed, ball F4 is used as the VIO pin for both x8 and x16 modes through different OPN offerings.

## 2. Physical Dimensions

### 2.1 48-pin TSOP Dimensions

STANDARD PIN OUT (TOP VIEW)



| Package | TS 048        |       |       |
|---------|---------------|-------|-------|
| Jedec   | MO-142 (B) EC |       |       |
| Symbol  | MIN           | NOM   | MAX   |
| A       | —             | —     | 1.20  |
| A1      | 0.05          | —     | 0.15  |
| A2      | 0.95          | 1.00  | 1.05  |
| b1      | 0.17          | 0.20  | 0.23  |
| b       | 0.17          | 0.22  | 0.27  |
| c1      | 0.10          | —     | 0.16  |
| c       | 0.10          | —     | 0.21  |
| D       | 19.80         | 20.00 | 20.20 |
| D1      | 18.30         | 18.40 | 18.50 |
| E       | 11.90         | 12.00 | 12.10 |
| e       | 0.50 BASIC    |       |       |
| L       | 0.50          | 0.60  | 0.70  |
| 0       | 0°            | 3°    | 5°    |
| R       | 0.08          | —     | 0.20  |
| N       | 48            |       |       |

## NOTES:

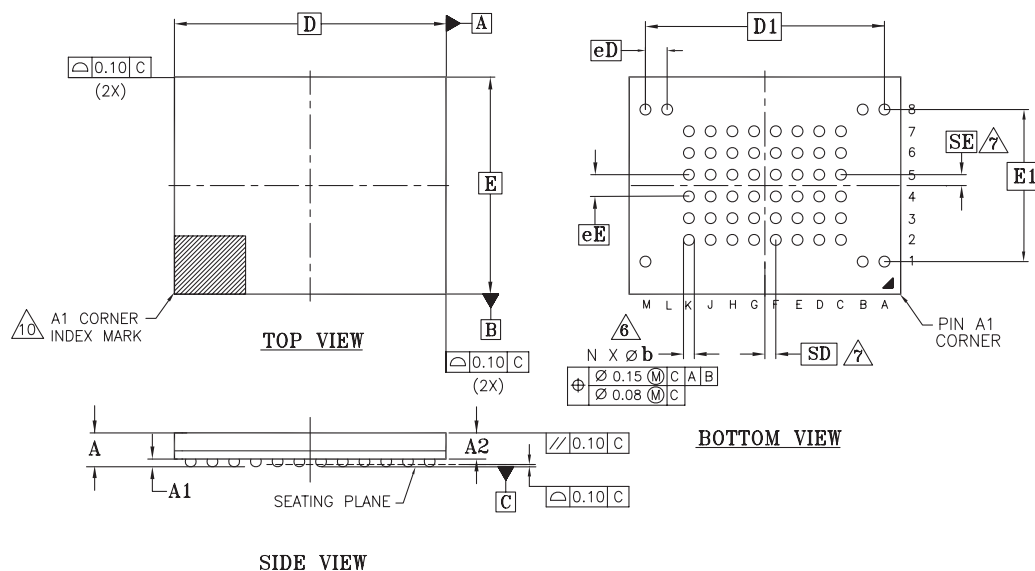
- 1 CONTROLLING DIMENSIONS ARE IN MILLIMETERS (MM). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
- 2 PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
- 3 NOT APPLICABLE.
- 4 TO BE DETERMINED AT THE SEATING PLANE [C]. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
- 5 DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15MM (.0059") PER SIDE.
- 6 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 (0.0028").
- 7 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10MM (.0039") AND 0.25MM (0.0098") FROM THE LEAD TIP.
- 8 LEAD COPLANARITY SHALL BE WITHIN 0.10MM (0.004") AS MEASURED FROM THE SEATING PLANE.
- 9 DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

**Note**

For other available package options, please contact your Spansion representative.

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## 2.2 VBW055 - 55-Ball Fine-Pitch Ball Grid Array Dimensions



|                                                                                             |                                |      |      |                          |
|---------------------------------------------------------------------------------------------|--------------------------------|------|------|--------------------------|
| PACKAGE                                                                                     | VBW 055                        |      |      |                          |
| JEDEC                                                                                       | N/A                            |      |      |                          |
|                                                                                             | 10.00 mm x 8.00 mm NOM PACKAGE |      |      |                          |
| SYMBOL                                                                                      | MIN                            | NOM  | MAX  | NOTE                     |
| A                                                                                           | ---                            | ---  | 1.00 | PROFILE                  |
| A1                                                                                          | 0.17                           | ---  | ---  | BALL HEIGHT              |
| A2                                                                                          | 0.60                           | ---  | 0.72 | BODY THICKNESS           |
| D                                                                                           | 10.00 BSC.                     |      |      | BODY SIZE                |
| E                                                                                           | 8.00 BSC.                      |      |      | BODY SIZE                |
| D1                                                                                          | 8.80 BSC.                      |      |      | MATRIX FOOTPRINT         |
| E1                                                                                          | 5.60 BSC.                      |      |      | MATRIX FOOTPRINT         |
| MD                                                                                          | 12                             |      |      | MATRIX SIZE D DIRECTION  |
| ME                                                                                          | 8                              |      |      | MATRIX SIZE E DIRECTION  |
| N                                                                                           | 55                             |      |      | BALL COUNT               |
| Ø b                                                                                         | 0.35                           | 0.40 | 0.45 | BALL DIAMETER            |
| eE                                                                                          | 0.80 BSC.                      |      |      | BALL PITCH               |
| eD                                                                                          | 0.80 BSC.                      |      |      | BALL PITCH               |
| SD SE                                                                                       | 0.40 BSC.                      |      |      | SOLDER BALL PLACEMENT    |
| A2-A7, B2-B7, L1-L7, M2-M7, K1, J1, H1, G1, F1, E1, D1, C1, K8, J8, H8, G8, F8, E8, D8, C8, |                                |      |      | DEPOPULATED SOLDER BALLS |

### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.  
N IS THE TOTAL NUMBER OF SOLDER BALLS.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
- WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.
- WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
- NOT USED.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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### 3. Pin Names and Descriptions

#### 3.1 Pin Names and Functions

**Table 3.1** S30ML-P ORNAND™ Flash Family Pin Configurations

| Pin Name        | Pin Function              |
|-----------------|---------------------------|
| I/O15 to I/O0   | Data Input/Output         |
| CLE             | Command Latch Enable      |
| ALE             | Address Latch Enable      |
| CE#             | Chip Enable               |
| RE#             | Read Enable               |
| WE#             | Write Enable              |
| WP#             | Write Protect             |
| PRE             | Power On Read Enable      |
| RY/BY#          | Ready/Busy Output         |
| V <sub>CC</sub> | Power                     |
| V <sub>SS</sub> | Ground                    |
| V <sub>IO</sub> | Input/Output Buffer Power |
| NC              | No Connect                |
| FP#             | Fast Program/Erase Mode   |

#### 3.2 Pin Descriptions

This device is a word/byte serial access memory which uses time-sharing input of address information.

**Table 3.2** S30ML-P ORNAND™ Flash Family Pin Descriptions (Sheet 1 of 2)

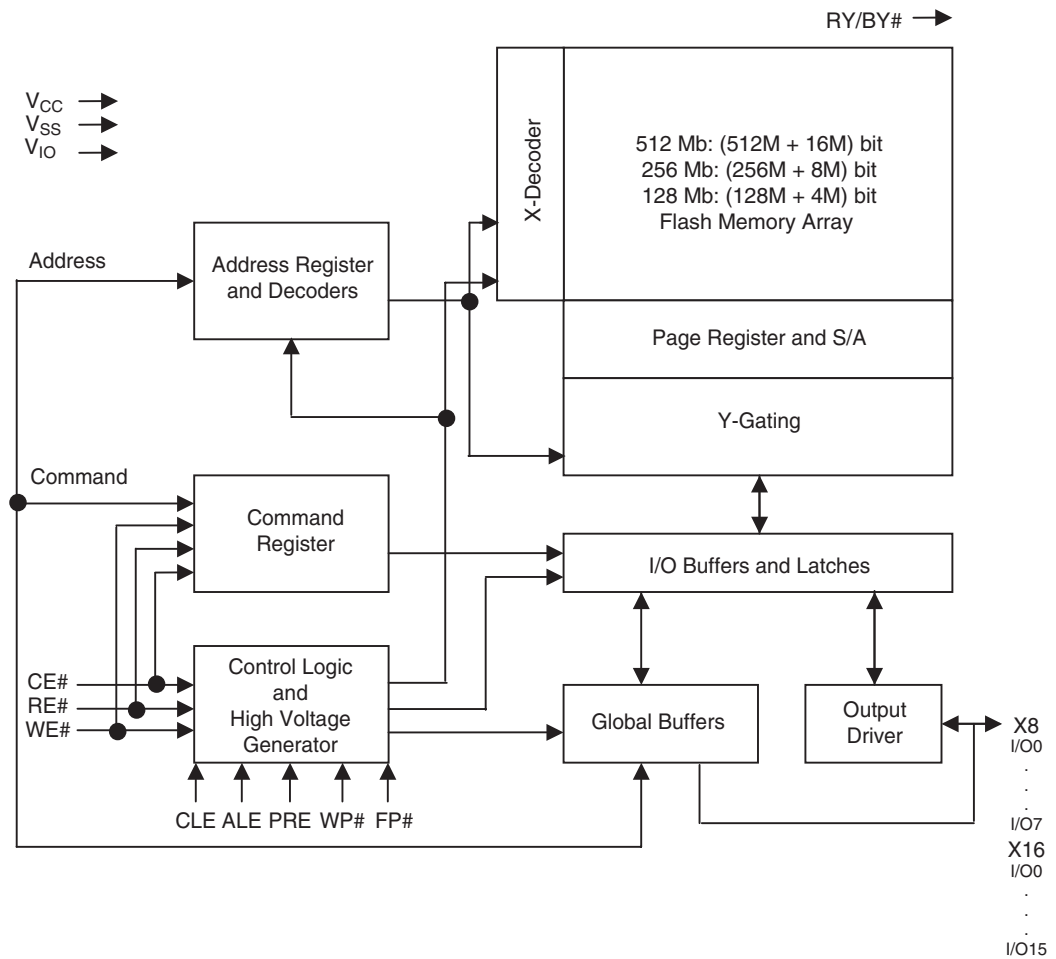
| Pin          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I/O7 – I/O0  | <b>Data Inputs/Outputs.</b> The I/O0 to I/O7 pins are used for transferring address, command, and input data to the device and output data from the device. Active for x8 and x16 ORNAND device configurations.                                                                                                                                                                                                                                               |
| I/O15 – I/O8 | <b>Data Inputs/Data Outputs.</b> The I/O8 to I/O15 pins are used for transferring address, command, and input data to the device and output data from the device. Active only for x16 ORNAND device configuration. I/O8 to I/O15 must be low level during address and command input.                                                                                                                                                                          |
| CLE          | <b>Command Latch Enable.</b> The CLE input signal is used to control the loading of any command into the internal command register. The command is always latched into the internal command register from the data inputs on the rising edge of WE# signal while the CLE signal is active high.                                                                                                                                                               |
| ALE          | <b>Address Latch Enable.</b> The ALE input signal is used to control the loading of any address into the internal address register. The address is always latched into the internal address register from the data inputs on the rising edge of WE# signal while the ALE signal is active high.                                                                                                                                                               |
| CE#          | <b>Chip Enable.</b> The CE# input signal controls if the device is selected. When the device is in the Busy State (RY/BY# = L) while a read, program, or erase operation is in progress, the CE# signal going high is ignored. While in Busy State, the device will not enter Standby Mode even with the CE# signal going high.                                                                                                                               |
| RE#          | <b>Read Enable.</b> The RE# input signal controls reads from the device. Output data is driven and becomes available t <sub>REA</sub> time after the falling edge of RE# signal. The internal address column counter increments up one address every RE# rising edge.                                                                                                                                                                                         |
| WE#          | <b>Write Enable.</b> The WE# input signal controls writes to the device. Commands, addresses, and input data are latched on the rising edge of WE# signal.                                                                                                                                                                                                                                                                                                    |
| WP#          | <b>Write Protect.</b> The WP# input signal is used to protect the device from accidental programming or erasing. When WP# signal is asserted low, the entire memory is protected from writes and no program and erase operation can execute.                                                                                                                                                                                                                  |
| PRE          | <b>Power-On Read Enable.</b> The PRE input signal controls the automatic read operation execution during power-on. The power-on automatic read feature is enabled when PRE signal is asserted high during power-on and allows page 0 to be automatically read out of the device so any system can automatically shadow boot code into DRAM without having to issue a read command. It is recommended that the user tie the PRE input pin to V <sub>CC</sub> . |

**Table 3.2** S30ML-P ORNAND™ Flash Family Pin Descriptions (Sheet 2 of 2)

| Pin             | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RY/BY#          | <b>Ready/Busy.</b> The RY/BY# output signal is used to indicate the operating condition of the device. The RY/BY# signal is always in the Busy State and asserts low when the device is executing read, program, and erase operations. When a read, program, or erase operation has completed, the RY/BY# signal stops asserting low to indicate completion and that the device is ready for a new operation. Since the RY/BY# output is open-drain, an external pull-up resistor is required. |
| V <sub>CC</sub> | <b>Power Supply.</b> The V <sub>CC</sub> input is the main power supply for this device.                                                                                                                                                                                                                                                                                                                                                                                                       |
| V <sub>SS</sub> | <b>Ground.</b> The V <sub>SS</sub> input is the main supply ground for this device.                                                                                                                                                                                                                                                                                                                                                                                                            |
| NC              | <b>No Connect.</b> Lead is not internally connected.                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| V <sub>IO</sub> | <b>V<sub>IO</sub></b> is the I/O power supply for device. The V <sub>IO</sub> pin exists only if the Enhanced Versatile I/O control feature is needed through a different product ordering part number.                                                                                                                                                                                                                                                                                        |
| FP#             | <b>Fast Program/Erase Mode.</b> FP# is used to set the device in standard mode or Fast Program/Erase Mode. When FP# is held at V <sub>IL</sub> , the device operates in Fast Program/Erase Mode. When FP# is held at V <sub>IH</sub> , the device operates in standard mode. Note: FP# contains an internal pull-up. When unconnected, FP# is at V <sub>IH</sub> .                                                                                                                             |

## 4. Block Diagram

**Figure 4.1** S30ML-P ORNAND™ Flash Family Block Diagram



## 5. Ordering Information

The ordering part number is formed by a valid combination of the following:

| S30ML | 512 | P | 30 | T | F | I | 00 | 0 |                                               |
|-------|-----|---|----|---|---|---|----|---|-----------------------------------------------|
|       |     |   |    |   |   |   |    |   | <b>PACKING TYPE</b> (Note 1)                  |
|       |     |   |    |   |   |   |    |   | 0 = Tray                                      |
|       |     |   |    |   |   |   |    |   | 3 = 13-inch Tape and Reel                     |
|       |     |   |    |   |   |   |    |   | <b>MODEL NUMBER</b>                           |
|       |     |   |    |   |   |   |    |   | 00 = x8, no V <sub>IO</sub> , ECC-free        |
|       |     |   |    |   |   |   |    |   | 01 = x16, no V <sub>IO</sub> , ECC-free       |
|       |     |   |    |   |   |   |    |   | 02 = x8, with V <sub>IO</sub> , ECC-free      |
|       |     |   |    |   |   |   |    |   | 03 = x16, with V <sub>IO</sub> , ECC-free     |
|       |     |   |    |   |   |   |    |   | 50 = x8, no V <sub>IO</sub> , ECC required    |
|       |     |   |    |   |   |   |    |   | 51 = x16, no V <sub>IO</sub> , ECC required   |
|       |     |   |    |   |   |   |    |   | 52 = x8, with V <sub>IO</sub> , ECC required  |
|       |     |   |    |   |   |   |    |   | 53 = x16, with V <sub>IO</sub> , ECC required |
|       |     |   |    |   |   |   |    |   | <b>TEMPERATURE RANGE</b>                      |
|       |     |   |    |   |   |   |    |   | I = Industrial (−40°C to +85°C)               |
|       |     |   |    |   |   |   |    |   | <b>PACKAGE MATERIAL SET</b>                   |
|       |     |   |    |   |   |   |    |   | F = Pb-free                                   |
|       |     |   |    |   |   |   |    |   | <b>PACKAGE TYPE</b>                           |
|       |     |   |    |   |   |   |    |   | T = Thin Small Outline Package (TSOP)         |
|       |     |   |    |   |   |   |    |   | B = Fine-Pitch Ball Grid Array (FBGA)         |
|       |     |   |    |   |   |   |    |   | <b>SPEED OPTION</b>                           |
|       |     |   |    |   |   |   |    |   | 30 = 30 ns                                    |
|       |     |   |    |   |   |   |    |   | 50 = 50 ns                                    |
|       |     |   |    |   |   |   |    |   | <b>PROCESS TECHNOLOGY</b>                     |
|       |     |   |    |   |   |   |    |   | P = 90 nm MirrorBit Technology                |
|       |     |   |    |   |   |   |    |   | <b>FLASH DENSITY</b>                          |
|       |     |   |    |   |   |   |    |   | 512 = 512 Mb                                  |
|       |     |   |    |   |   |   |    |   | 256 = 256 Mb                                  |
|       |     |   |    |   |   |   |    |   | 128 = 128 Mb                                  |
|       |     |   |    |   |   |   |    |   | <b>DEVICE FAMILY</b>                          |
|       |     |   |    |   |   |   |    |   | S30ML = 3.0 V. NAND Interface Flash Memory    |

### 5.1 Valid Combinations

Valid Combination list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

| Base Part Number                   | Speed Option | Package, Material, and Temperature Range | Model Number<br>(Note 4) | Packing Type  | Package Description                |
|------------------------------------|--------------|------------------------------------------|--------------------------|---------------|------------------------------------|
| S30ML512,<br>S30ML256,<br>S30ML128 | 30           | TFI, BFI (Note 3)                        | 00, 50                   | 0, 3 (Note 1) | TS048 TSOP (Note 2)<br>VBW055 FBGA |
|                                    | 50           |                                          | 01, 51                   |               |                                    |

## Notes

1. Type 0 is standard.
2. TSOP package marking omits packing type designator from ordering part number.
3. Use "TFE" and "BFE" to request engineering samples prior to volume production release.
4. Consult your local sales representative for availability of model numbers 02, 03, 52, 53.

## 6. Electrical Specifications

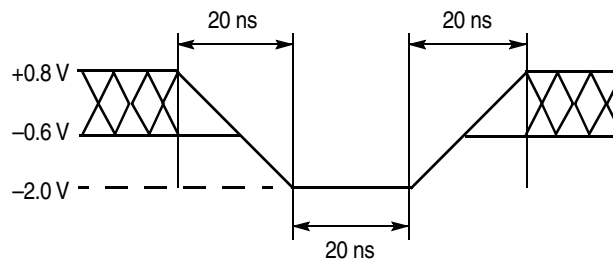
### 6.1 Absolute Maximum Ratings

| Parameter                               | Symbol     | Rating                   | Unit |
|-----------------------------------------|------------|--------------------------|------|
| Voltage on any pin relative to $V_{SS}$ | $V_{CC}$   | -0.6 to +4.6             | V    |
| Storage Temperature                     | $T_{STG}$  | -65 to +150              | °C   |
| Operating Temperature                   | $T_{OPR}$  | -40 to +85 (Industrial)  | °C   |
| Temperature under bias                  | $T_{BIAS}$ | -10 to +125 (Industrial) | °C   |
| Short circuit current                   | $I_{OS}$   | 5                        | mA   |

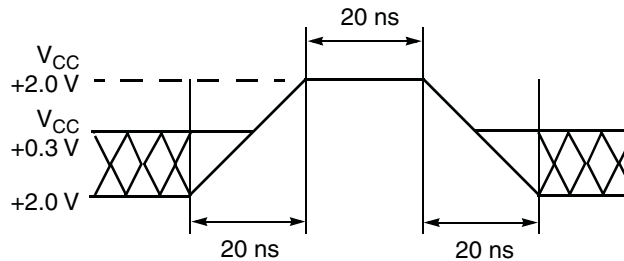
#### Notes

1. Minimum DC voltage is -0.6V on Input/ Output pins. During transitions the I/O pins may undershoot  $V_{SS}$  to -2.0 V for periods of less than 20 ns
2. Maximum DC voltage is  $V_{CC} + 0.3$  V on I/O pins which, during transitions, can overshoot to  $V_{CC} + 2.0$  V for periods of less than 20ns.
3. Permanent device damage can occur if [Absolute Maximum Ratings](#) are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

**Figure 6.1** Maximum Negative Overshoot Waveform



**Figure 6.2** Maximum Positive Overshoot Waveform



### 6.2 Capacitance

| Symbol    | Description                                         | Test Condition | Typ. | Max. | Unit |
|-----------|-----------------------------------------------------|----------------|------|------|------|
| $C_{IN}$  | Input Capacitance<br>(All pins, except PRE and WP#) | $V_{IN} = 0$   | —    | 10   | pF   |
|           | Input Capacitance - PRE and WP#                     | $V_{IN} = 0$   | —    | 25   | pF   |
| $C_{OUT}$ | Output Capacitance                                  | $V_{OUT} = 0$  | —    | 10   | pF   |

#### Notes

1. Test conditions  $T_A = 25^\circ\text{C}$ ,  $f = 1.0$  MHz
2. Sampled, not 100% tested.

## 6.3 Valid Blocks

**Table 6.1** Devices with up to 2% Invalid Blocks (ECC-Required)

| Parameter              | Symbol   | Density | Minimum | Typical | Max | Unit   |
|------------------------|----------|---------|---------|---------|-----|--------|
| Number of Valid Blocks | $N_{VB}$ | 512 Mb  | 126     | -       | 128 | Blocks |
|                        |          | 256 Mb  | 63      | -       | 64  |        |
|                        |          | 128 Mb  | 31      | -       | 32  |        |

**Note**

- For Model Numbers 50, 51, 52, and 53, Block 0 is valid upon shipment and error-free through 1000 cycles.
- Model Numbers 00, 01, 02, 03 are offered with 100% valid blocks.

## 6.4 Recommended DC Operating Conditions

| Parameter                                   | Symbol   | Minimum | Typical | Max. | Unit |
|---------------------------------------------|----------|---------|---------|------|------|
| Power Supply Voltage                        | $V_{CC}$ | 2.7     | 3.3     | 3.6  | V    |
| Power Supply Ground                         | $V_{SS}$ | 0       | 0       | 0    |      |
| I/O Power Supply Voltage                    | $V_{IO}$ | 1.7     | –       | 3.6  | V    |
| Ambient Temperature, Industrial (I) Devices | $T_A$    | –40     | –       | +85  | °C   |

## 6.5 DC Characteristics—CMOS Compatible

| Parameter      | Description                                              | Test Conditions                                         | Min. | Typ. | Max.     | Unit    |
|----------------|----------------------------------------------------------|---------------------------------------------------------|------|------|----------|---------|
| $I_{LI}$       | Input Load Current                                       | $V_{IN} = V_{SS}$ to $V_{CC}$ , $V_{CC} = V_{CC\ max}$  |      |      | $\pm 10$ | $\mu A$ |
| $I_{LO}$       | Output Leakage Current                                   | $V_{OUT} = V_{SS}$ to $V_{CC}$ , $V_{CC} = V_{CC\ max}$ |      |      | $\pm 10$ | $\mu A$ |
| $I_{CC1}$      | $V_{CC}$ Active Read Current (average during read cycle) | $t_{CYCLE} = 30\ ns$ , $I_{OUT} = 0\ mA$                |      | 35   | 50       | mA      |
| $I_{CC2}$      | $V_{CC}$ Program Current (Standard Mode)                 |                                                         |      | 31   | 47       | mA      |
| $I_{CC3\ (1)}$ | $V_{CC}$ Program Current (Fast Program/Erase Mode)       |                                                         |      | 48   | 73       | mA      |
| $I_{CC4}$      | $V_{CC}$ Erase Current (Standard Mode)                   |                                                         |      | 31   | 47       | mA      |
| $I_{CC5\ (1)}$ | $V_{CC}$ Erase Current (Fast Program/Erase Mode)         |                                                         |      | 48   | 73       | mA      |

**Note**

- For Fast Mode Operation,  $V_{CC} = 3.3V$  to  $3.6V$

**Table 6.2** No  $V_{IO}$  Pin

| Parameter         | Description                     | Test Conditions                                                                     | Min. | Typ. | Max.           | Unit    |
|-------------------|---------------------------------|-------------------------------------------------------------------------------------|------|------|----------------|---------|
| $V_{IH}$ (Note 1) | Input High Voltage              |                                                                                     | 2.0  |      | $V_{CC} + 0.3$ | V       |
| $V_{IL}$ (Note 2) | Input Low Voltage               |                                                                                     | –0.3 |      | 0.8            | V       |
| $V_{OH}$          | Output High Voltage             | $I_{OH} = -400\ \mu A$                                                              | 2.4  |      |                | V       |
| $V_{OL}$          | Output Low Voltage              | $I_{OL} = 2.1\ mA$                                                                  |      |      | 0.4            | V       |
| $I_{OL}$          | Output Low Current (RY/BY#)     | $V_{OL} = 0.4\ V$                                                                   | 8    | 12   |                | mA      |
| $I_{SB1}$         | $V_{CC}$ Standby Current (TTL)  | $CE\# = V_{IH}$ , $WP\# = V_{IH}$ or $V_{IL}$ , $PRE = V_{CC}$ or $V_{SS}$          |      |      | 1              | mA      |
| $I_{SB2}$         | $V_{CC}$ Standby Current (CMOS) | $CE\# = V_{CC} - 0.2\ V$ , $WP\# = V_{IH}$ or $V_{IL}$ , $PRE = V_{CC}$ or $V_{SS}$ |      | 10   | 50             | $\mu A$ |

**Notes**

- $V_{IH}$  can overshoot to  $V_{CC} + 2.0\ V$  for durations of 20 ns or less.
- $V_{IL}$  can undershoot to  $-2.0\ V$  for durations of 20 ns or less.

Table 6.3 With  $V_{IO}$  Pin,  $V_{IO} = 1.8V$ 

| Parameter         | Description                     | Test Conditions                                                                   | Min.         | Typ | Max          | Unit    |
|-------------------|---------------------------------|-----------------------------------------------------------------------------------|--------------|-----|--------------|---------|
| $V_{IH}$ (Note 1) | Input High Voltage              |                                                                                   | $V_{IO}-0.4$ |     | $V_{IO}+0.3$ | V       |
| $V_{IL}$ (Note 2) | Input Low Voltage               |                                                                                   | -0.3         |     | 0.4          | V       |
| $V_{OH}$          | Output High Voltage             | $I_{OH} = -100 \mu A$                                                             | $V_{IO}-0.1$ |     |              | V       |
| $V_{OL}$          | Output Low Voltage              | $I_{OL} = 100 \mu A$                                                              |              |     | 0.1          | V       |
| $I_{OL}$          | Output Low Current (RY/BY#)     | $V_{OL} = 0.1 V$                                                                  | 2            | 3   |              | mA      |
| $I_{SB1}$         | $V_{CC}$ Standby Current (TTL)  | CE# = $V_{IH}$ , WP# = $V_{IH}$ or $V_{IL}$ , PRE = $V_{CC}$ or $V_{SS}$          |              |     | 1            | mA      |
| $I_{SB2}$         | $V_{CC}$ Standby Current (CMOS) | CE# = $V_{IO}-0.2 V$ , WP# = $V_{IH}$ or $V_{IL}$ ,<br>PRE = $V_{CC}$ or $V_{SS}$ |              | 10  | 50           | $\mu A$ |

**Notes**

1.  $V_{IH}$  can overshoot to  $V_{CC} + 2.0 V$  for durations of 20 ns or less.
2.  $V_{IL}$  can undershoot to  $-2.0 V$  for durations of 20 ns or less.

## 6.6 AC Characteristics—CMOS Compatible

| Parameter         | Description                               | Min.<br>(x8, no V <sub>IO</sub> ) | Max<br>(x8, no V <sub>IO</sub> ) | Min.<br>(x8 with V <sub>IO</sub> ,<br>x16 no V <sub>IO</sub> ,<br>x16 with V <sub>IO</sub> ) | Max<br>(x8 with V <sub>IO</sub> ,<br>x16 no V <sub>IO</sub> ,<br>x16 with V <sub>IO</sub> ) | Unit |
|-------------------|-------------------------------------------|-----------------------------------|----------------------------------|----------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|------|
| t <sub>CLS</sub>  | CLE Setup Time                            | 0                                 | -                                | 0                                                                                            | -                                                                                           | ns   |
| t <sub>CLH</sub>  | CLE Hold Time                             | 10                                | -                                | 10                                                                                           | -                                                                                           |      |
| t <sub>CS</sub>   | CE Setup Time                             | 0                                 | -                                | 0                                                                                            | -                                                                                           |      |
| t <sub>CH</sub>   | CE Hold Time                              | 10                                | -                                | 10                                                                                           | -                                                                                           |      |
| t <sub>WP</sub>   | Write Pulse Width (See Note)              | 15                                | -                                | 25                                                                                           | -                                                                                           |      |
| t <sub>ALS</sub>  | ALE Setup Time                            | 0                                 | -                                | 0                                                                                            | -                                                                                           |      |
| t <sub>ALH</sub>  | ALE Hold Time                             | 10                                | -                                | 10                                                                                           | -                                                                                           |      |
| t <sub>DS</sub>   | Data Setup Time                           | 15                                | -                                | 20                                                                                           | -                                                                                           |      |
| t <sub>DH</sub>   | Data Hold Time                            | 5                                 | -                                | 10                                                                                           | -                                                                                           |      |
| t <sub>WC</sub>   | Write Cycle Time                          | 30                                | -                                | 45                                                                                           | -                                                                                           |      |
| t <sub>WH</sub>   | WE# High Hold Time                        | 10                                | -                                | 15                                                                                           | -                                                                                           |      |
| t <sub>WW</sub>   | WP# High to WE# Low                       | 100                               | -                                | 100                                                                                          | -                                                                                           |      |
| t <sub>RR</sub>   | Ready to RE# Falling Edge                 | 20                                | -                                | 20                                                                                           | -                                                                                           |      |
| t <sub>RW</sub>   | Ready to WE# Falling Edge                 | 20                                | -                                | 20                                                                                           | -                                                                                           |      |
| t <sub>RP</sub>   | Read Pulse Width                          | 20                                | -                                | 30                                                                                           | -                                                                                           |      |
| t <sub>RC</sub>   | Read Cycle Time                           | 30                                | -                                | 50                                                                                           | -                                                                                           |      |
| t <sub>REA</sub>  | RE# Access Time                           | -                                 | 18                               | -                                                                                            | 30                                                                                          |      |
| t <sub>CEA</sub>  | CE# Access Time                           | -                                 | 23                               | -                                                                                            | 35                                                                                          |      |
| t <sub>CLR</sub>  | CLE to RE# delay                          | 10                                | -                                | 10                                                                                           | -                                                                                           |      |
| t <sub>ALEA</sub> | ALE Access Time                           | -                                 | 28                               | -                                                                                            | 40                                                                                          |      |
| t <sub>OH</sub>   | Data Output Hold Time                     | 10                                | -                                | 10                                                                                           | -                                                                                           |      |
| t <sub>RHZ</sub>  | RE# High to Output High Impedance         | -                                 | 40                               | -                                                                                            | 40                                                                                          |      |
| t <sub>CHZ</sub>  | CE# High to Output High Impedance         | -                                 | 40                               | -                                                                                            | 40                                                                                          |      |
| t <sub>REH</sub>  | RE# High Hold Time                        | 5                                 | -                                | 15                                                                                           | -                                                                                           |      |
| t <sub>IR</sub>   | Output High Impedance to RE# Falling Edge | 0                                 | -                                | 0                                                                                            | -                                                                                           |      |
| t <sub>RHW</sub>  | RE# High to WE# Low                       | 30                                | -                                | 30                                                                                           | -                                                                                           |      |
| t <sub>WHC</sub>  | WE# High to CE# Low                       | 30                                | -                                | 30                                                                                           | -                                                                                           |      |
| t <sub>WHR</sub>  | WE# High to RE# Low                       | 60                                | -                                | 60                                                                                           | -                                                                                           |      |
| t <sub>R</sub>    | Data Transfer from Memory to Register     | -                                 | 9                                | -                                                                                            | 9                                                                                           | μs   |
| t <sub>WB</sub>   | WE# High to Busy                          | -                                 | 100                              | -                                                                                            | 100                                                                                         | ns   |
| t <sub>RST</sub>  | Device Reset (Read/Program/Erase)         | Read                              | 5                                | -                                                                                            | 5                                                                                           | μs   |
|                   |                                           | Program                           | 10                               | -                                                                                            | 10                                                                                          |      |
|                   |                                           | Erase                             | 500                              | -                                                                                            | 500                                                                                         |      |
| t <sub>REAI</sub> | RE# Access Time (Read ID)                 |                                   | 18                               | -                                                                                            | 18                                                                                          | ns   |

**Note**

If T<sub>CS</sub> is less than 10 ns, T<sub>WP</sub> must be minimum 25 ns; otherwise T<sub>WP</sub> may be minimum 15 ns.

## 6.7 AC Test Conditions

| Test Condition                                                | No V <sub>IO</sub>               | With V <sub>IO</sub>   |
|---------------------------------------------------------------|----------------------------------|------------------------|
| Operating Range                                               | V <sub>CC</sub> = 2.7 V to 3.6 V |                        |
| Input level                                                   | 0.0 to V <sub>CC</sub>           | 0.0 to V <sub>IO</sub> |
| Input comparison                                              | V <sub>CC</sub> /2               | V <sub>IO</sub> /2     |
| Output data comparison level                                  | V <sub>CC</sub> /2               | V <sub>IO</sub> /2     |
| Load capacitance (C <sub>L</sub> )                            | 30 pF                            |                        |
| Transition time (t <sub>r</sub> ) (input rise and fall times) | 5 ns                             |                        |

## 6.8 Programming And Erase Characteristics

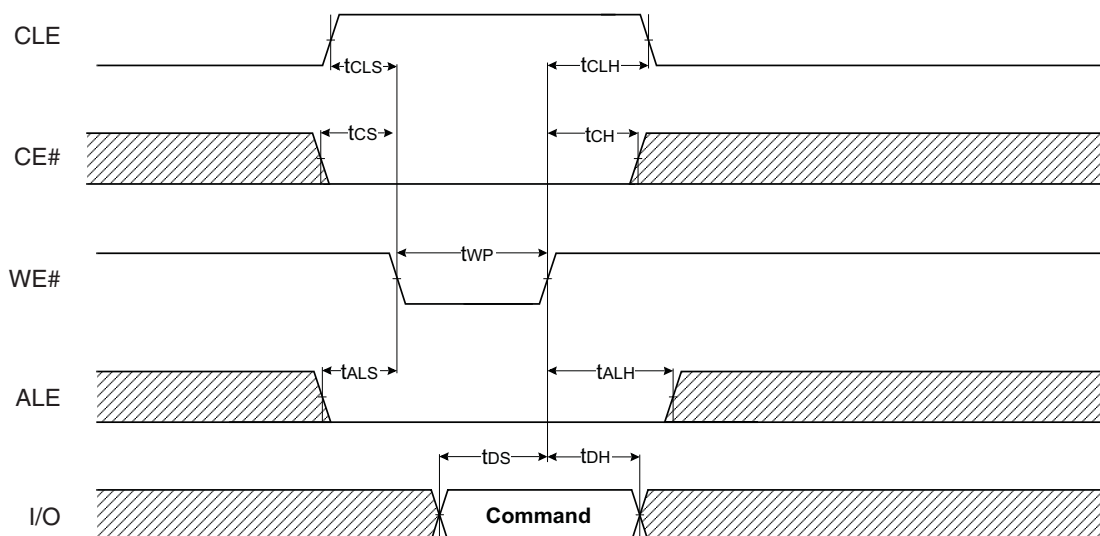
| Symbol              | Parameter                                 | Min. | Typ. (Note 1) | Max. (Note 2) | Unit          |
|---------------------|-------------------------------------------|------|---------------|---------------|---------------|
| $t_{\text{PROG}}$   | Average Programming Time (Standard Mode)  |      | 180           | 1400          | $\mu\text{s}$ |
|                     | Fast Program/Erase Mode Programming Time  |      | 170           | 1300          | $\mu\text{s}$ |
| N                   | Number of Programming Cycles on Same Page |      |               | 1             |               |
| $t_{\text{BERASE}}$ | Block Erase Time (Standard Mode)          |      | 150           | 400           | ms            |
|                     | Fast Program/Erase Mode Block Erase Time  |      | 130           | 360           | ms            |

### Notes

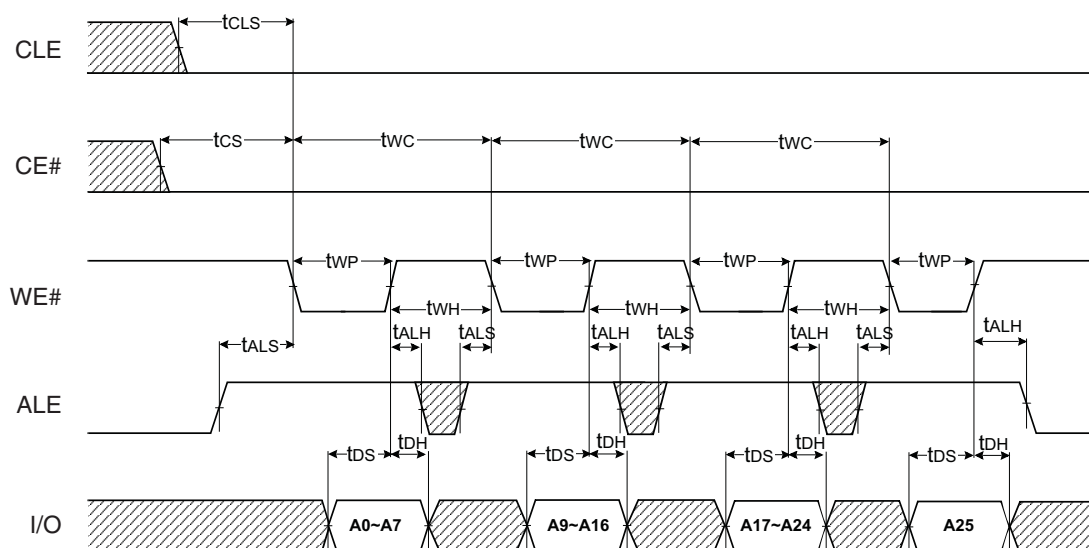
1. Assumes the following conditions: 25°C, 3.3V  $V_{\text{CC}}$ , 10,000 cycles; checkerboard data pattern.
2. Under worst case conditions: 90°C, 2.7V  $V_{\text{CC}}$ , 100,000 cycles.

## 7. Timing Diagrams

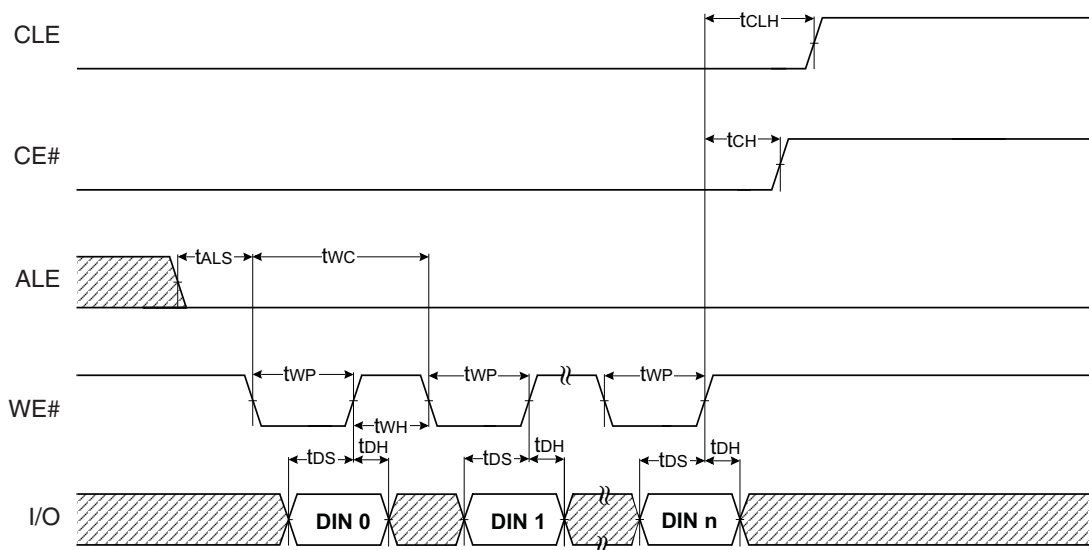
Figure 7.1 Command Latch Cycle Timing Diagram

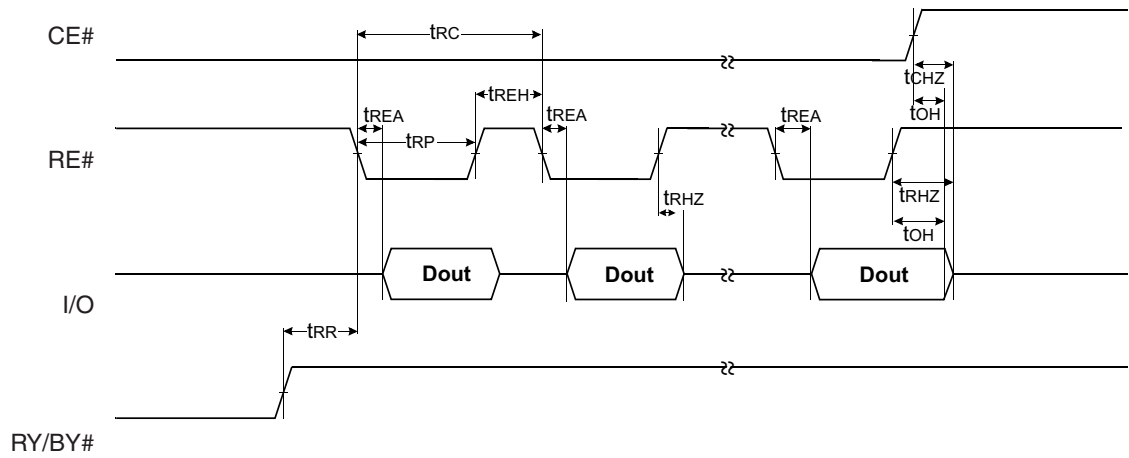
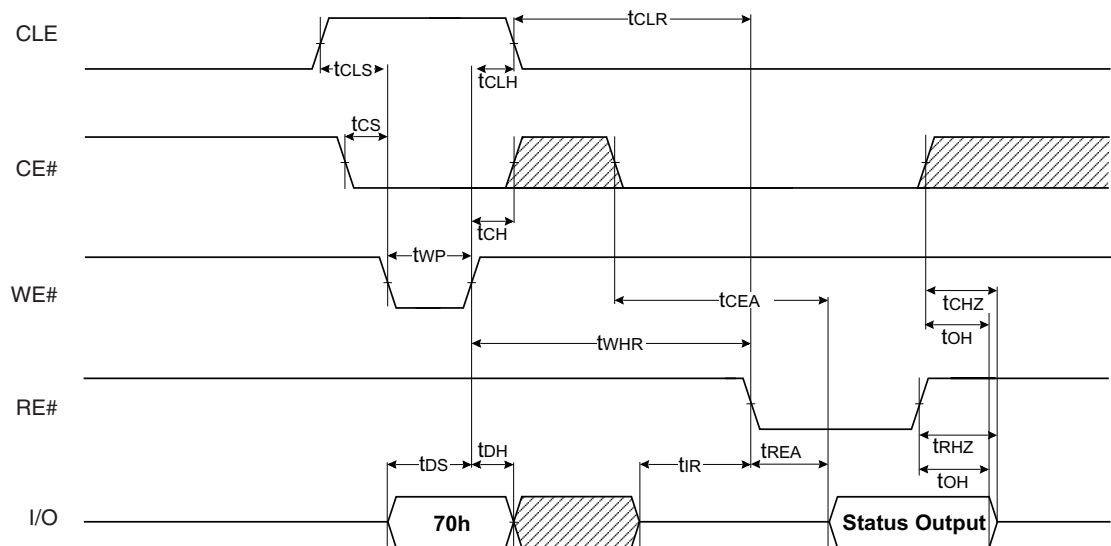


**Figure 7.2** Address Latch Cycle Timing Diagram



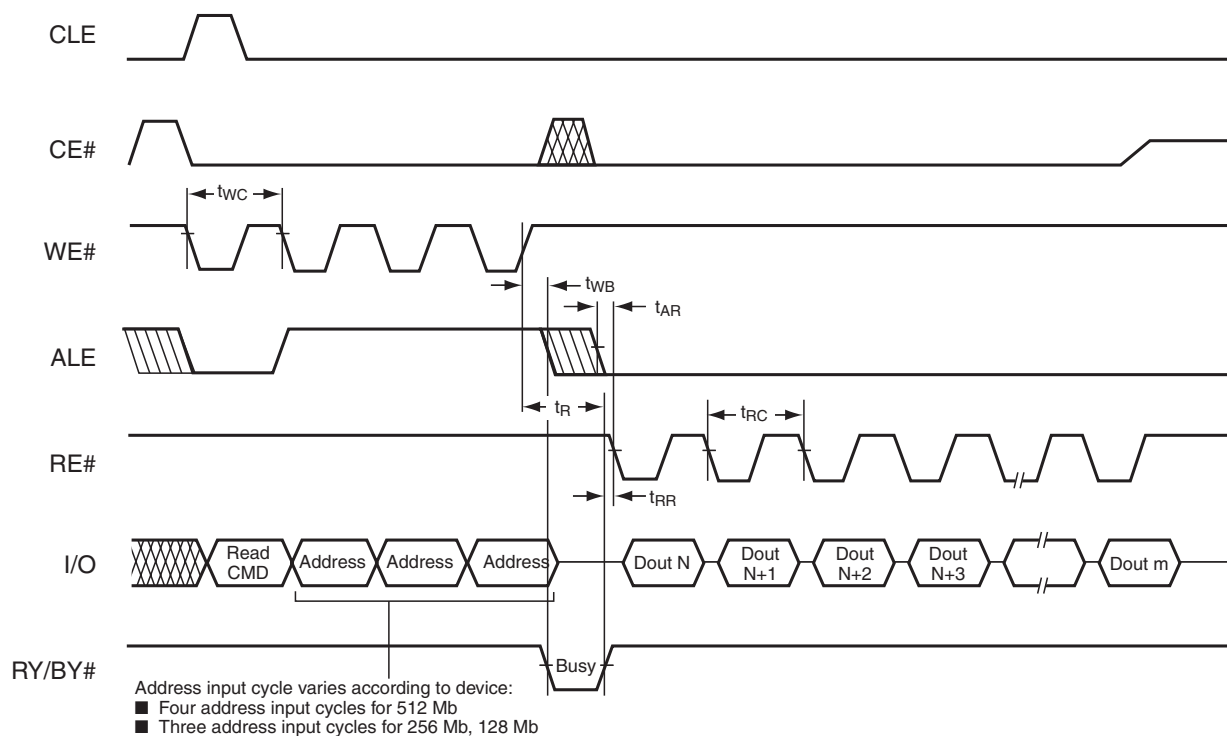
**Figure 7.3** Input Data Latch Cycle Timing Diagram



**Figure 7.4** Sequential Data Out Cycle Timing Diagram (CLE = Low, ALE = Low, WE# = High)**Figure 7.5** Status Read Cycle Timing Diagram

| I/O#  | Status                  | Definition                    |
|-------|-------------------------|-------------------------------|
| I/O 0 | Program/Erase           | 0: Successful Program/Erase   |
|       |                         | 1: Error in Program/Erase     |
| I/O 1 | Reserved for Future Use | 0                             |
| I/O 2 | Block Status            | 0 = Normal                    |
| I/O 3 | Reserved for Future Use | Don't care                    |
| I/O 4 | Reserved for Future Use | Don't care                    |
| I/O 5 | Reserved for Future Use | Don't care                    |
| I/O 6 | Device Operation        | 0: Busy<br>1 Ready            |
| I/O 7 | Write Protect           | 0: Protect<br>1 Not Protected |

**Figure 7.6** Read Operation Timing Diagram (00h or 01h Commands)



**Figure 7.7** Read Spare Area Operation Timing Diagram (50h command)

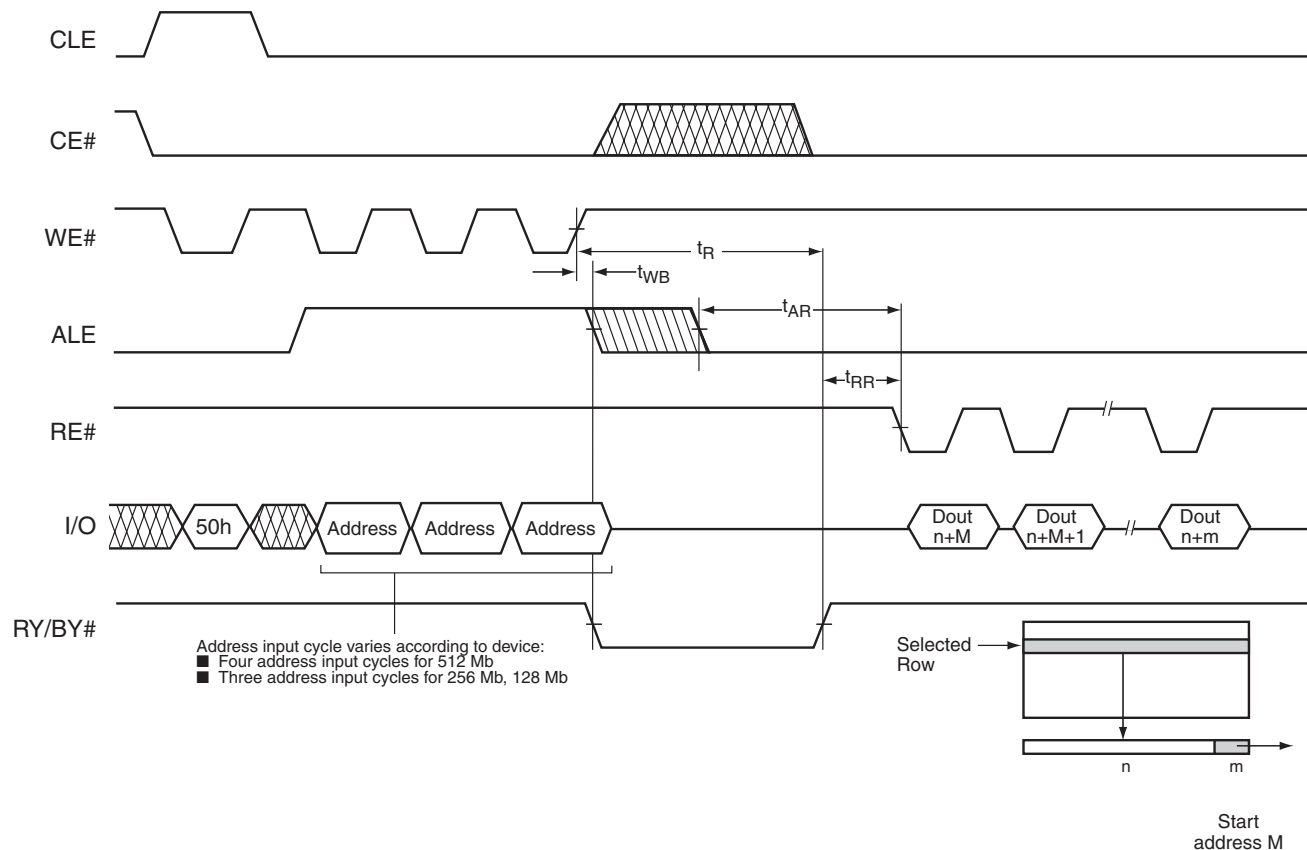
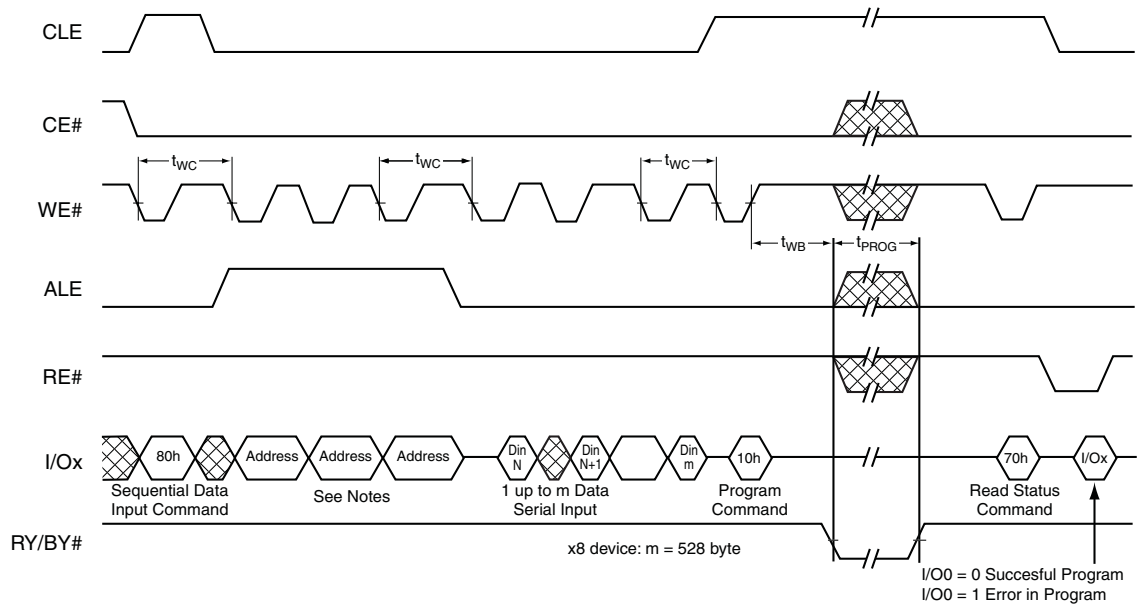
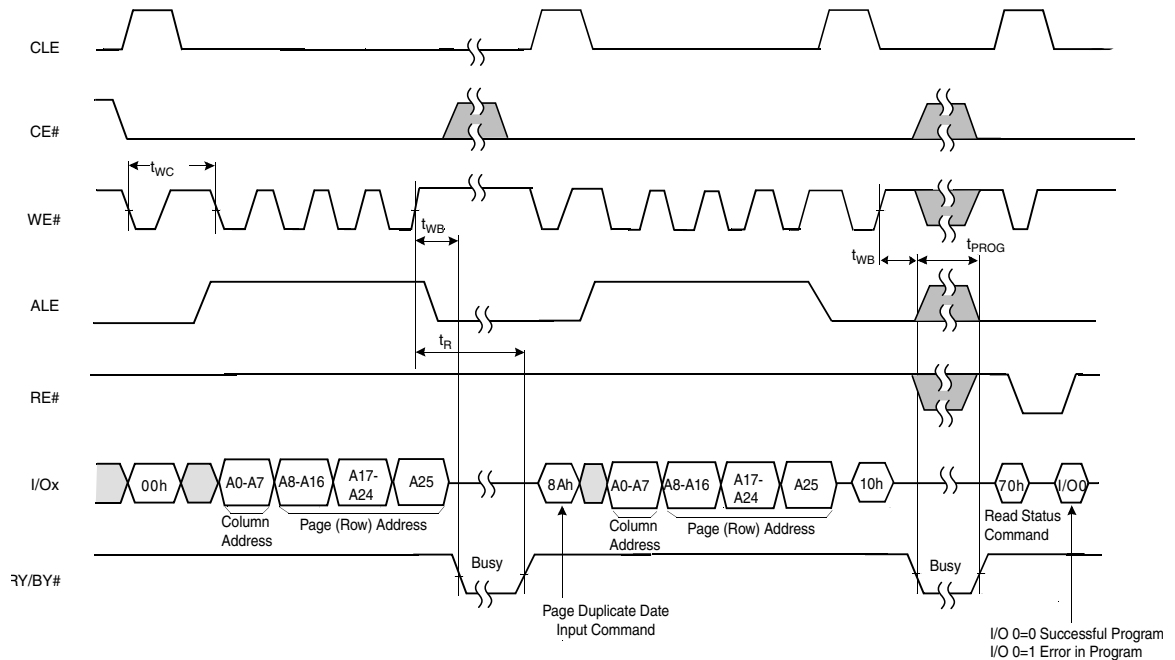


Figure 7.8 Page Program Timing Diagram

**Note**

Address input cycle varies per device: 512 Mb devices require 4 address input cycles; 256 Mb and 128 Mb devices require 3 address input cycles.

Figure 7.9 Page Duplicate Program Timing Diagram

**Note**

1. Address input cycle varies per device: 512 Mb devices require 4 address input cycles; 256 Mb and 128 Mb devices require 3 address input cycles.

Figure 7.10 Block Erase Timing Diagram

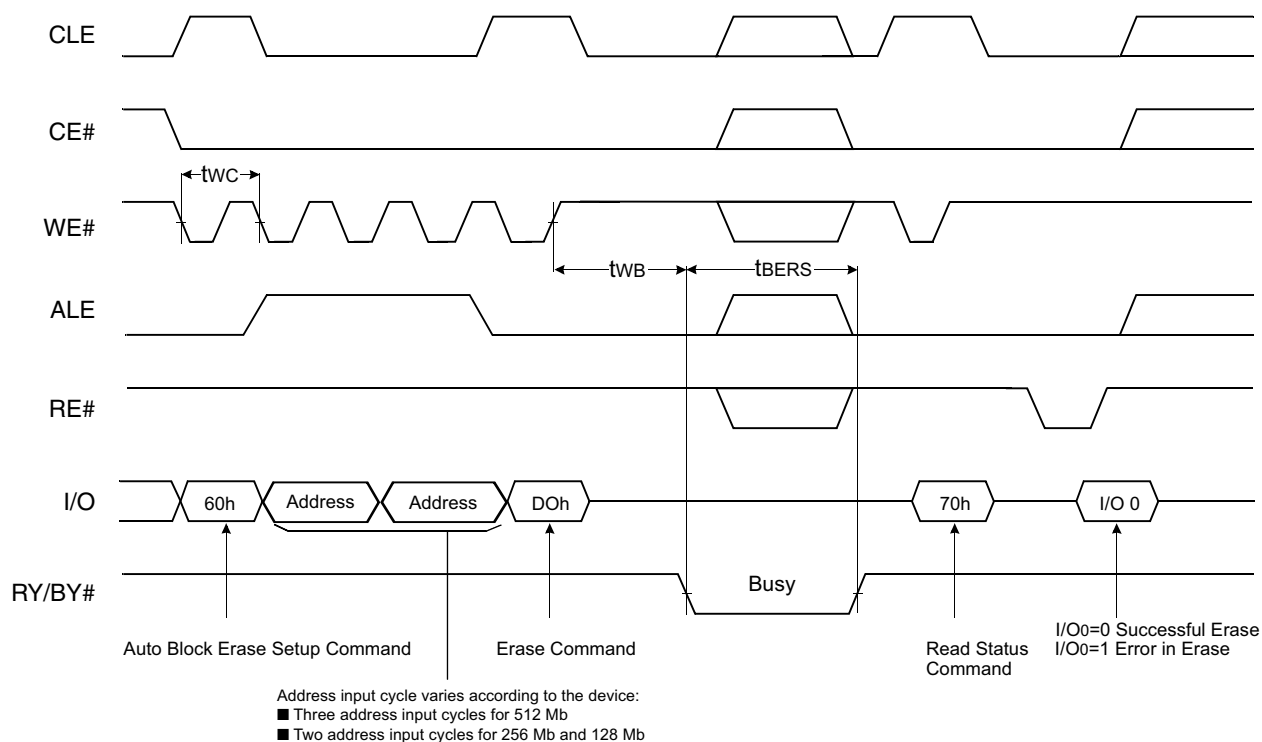
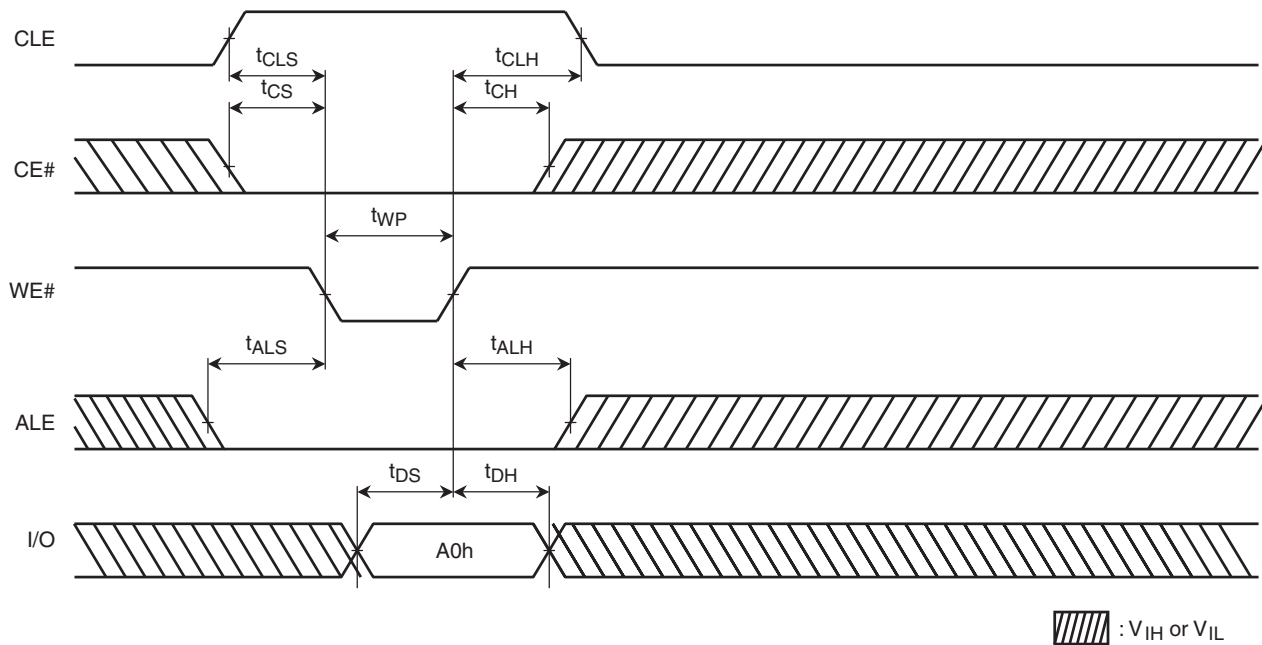


Figure 7.11 Spansion Command Mode Entry Timing Diagram

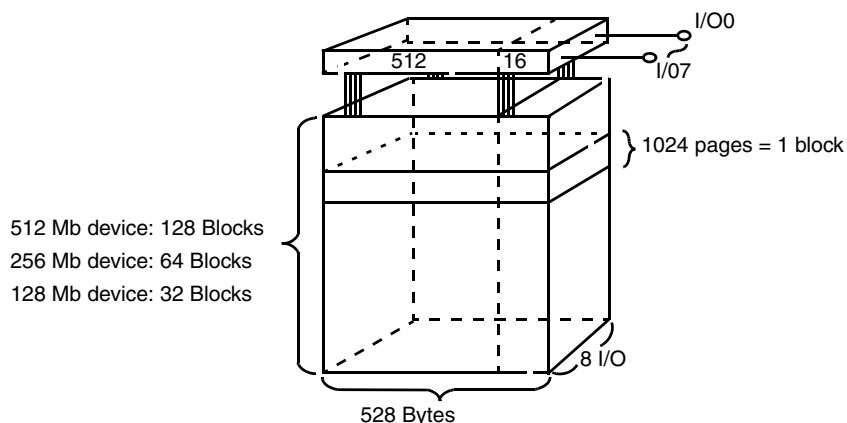


## 8. Schematic Cell Layouts and Address Assignments

The Program operation works on page units while the Erase operation work on block units.

### 8.1 x8 Array Organization

**Figure 8.1** x8 Array Organization



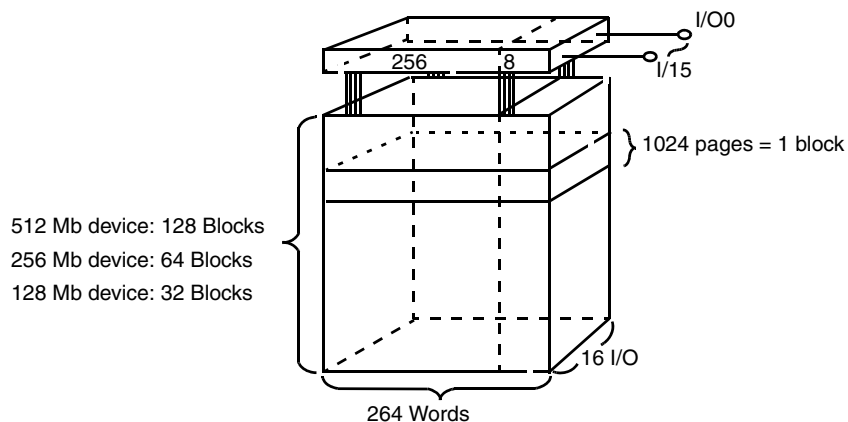
A page consists of 528 Bytes in which 512 Bytes are used for main memory storage and 16 Bytes are reserved for redundancy or other usage.

#### 8.1.1 512 Mb, 256 Mb, and 128 Mb

- 1 Page = 528 Bytes = (512+16) Bytes
- 1 Block = 528 Bytes x 1024 Pages = (512K + 16K) Bytes
- 512 Mb ORNAND Flash = 528 Bytes x 1024 Pages x 128 Blocks
- 256 Mb ORNAND Flash = 528 Bytes x 1024 Pages x 64 Blocks
- 128 Mb ORNAND Flash = 528 Bytes x 1024 Pages x 32 Blocks

## 8.2 x16 Array Organization

Figure 8.2 x16 Array Organization



A page consists of 264 Words in which 256 Words are used for main memory storage and 8 Words are reserved for redundancy or other usage.

### 8.2.1 512 Mb, 256 Mb, and 128 Mb

- 1 Page = 264 Words = (256 + 8) Words
- 1 Block = 264 Words x 1024 Pages = (256K + 8K) Words
- 512 Mb ORNAND Flash = 264 Words x 1024 Pages x 128 Blocks
- 256 Mb ORNAND Flash = 264 Words x 1024 Pages x 64 Blocks
- 128Mb ORNAND Flash = 264 Words x 1024 Pages x 32 Blocks

## 8.3 Address Assignments

The addresses for ORNAND Flash for accessing stored data is always input onto the I/O pins in a little-endian system. In a little-endian system, the least significant value in the sequence is stored first.

### 8.3.1 512 Mb, 256 Mb, and 128 Mb x8 Addressing

**Table 8.1** 512 Mb, 256 Mb, and 128 Mb x8 Addressing

| 512 Mb  | I/O0 | I/O1 | I/O2 | I/O3 | I/O4 | I/O5 | I/O6 | I/O7 |
|---------|------|------|------|------|------|------|------|------|
| Cycle 1 | A0   | A1   | A2   | A3   | A4   | A5   | A6   | A7   |
| Cycle 2 | A9   | A10  | A11  | A12  | A13  | A14  | A15  | A16  |
| Cycle 3 | A17  | A18  | A19  | A20  | A21  | A22  | A23  | A24  |
| Cycle 4 | A25  | L    | L    | L    | L    | L    | L    | L    |
| 256 Mb  | I/O0 | I/O1 | I/O2 | I/O3 | I/O4 | I/O5 | I/O6 | I/O7 |
| Cycle 1 | A0   | A1   | A2   | A3   | A4   | A5   | A6   | A7   |
| Cycle 2 | A9   | A10  | A11  | A12  | A13  | A14  | A15  | A16  |
| Cycle 3 | A17  | A18  | A19  | A20  | A21  | A22  | A23  | A24  |
| 128 Mb  | I/O0 | I/O1 | I/O2 | I/O3 | I/O4 | I/O5 | I/O6 | I/O7 |
| Cycle 1 | A0   | A1   | A2   | A3   | A4   | A5   | A6   | A7   |
| Cycle 2 | A9   | A10  | A11  | A12  | A13  | A14  | A15  | A16  |
| Cycle 3 | A17  | A18  | A19  | A20  | A21  | A22  | A23  | L    |

**Legend**

L = Logic Low

**Notes**

1. 00h Command (Read) defines the starting address of the main page area of the register.
2. 50h Command (Read) defines the starting address of the spare area of the register
3. The device ignores any additional input of address cycles than required

### 8.3.2 512 Mb, 256 Mb, and 128 Mb x16 Addressing

**Table 8.2** 512 Mb, 256 Mb, and 128 Mb x16 Addressing

| 512 Mb  | I/O0 | I/O1 | I/O2 | I/O3 | I/O4 | I/O5 | I/O6 | I/O7 | I/O8-I/O15 |
|---------|------|------|------|------|------|------|------|------|------------|
| Cycle 1 | A0   | A1   | A2   | A3   | A4   | A5   | A6   | A7   | L          |
| Cycle 2 | A9   | A10  | A11  | A12  | A13  | A14  | A15  | A16  | L          |
| Cycle 3 | A17  | A18  | A19  | A20  | A21  | A22  | A23  | A24  | L          |
| Cycle 4 | A25  | L    | L    | L    | L    | L    | L    | L    | L          |
| 256 Mb  | I/O0 | I/O1 | I/O2 | I/O3 | I/O4 | I/O5 | I/O6 | I/O7 | I/O8-I/O15 |
| Cycle 1 | A0   | A1   | A2   | A3   | A4   | A5   | A6   | A7   | L          |
| Cycle 2 | A9   | A10  | A11  | A12  | A13  | A14  | A15  | A16  | L          |
| Cycle 3 | A17  | A18  | A19  | A20  | A21  | A22  | A23  | A24  | L          |
| 128 Mb  | I/O0 | I/O1 | I/O2 | I/O3 | I/O4 | I/O5 | I/O6 | I/O7 | I/O8-I/O15 |
| Cycle 1 | A0   | A1   | A2   | A3   | A4   | A5   | A6   | A7   | L          |
| Cycle 2 | A9   | A10  | A11  | A12  | A13  | A14  | A15  | A16  | L          |
| Cycle 3 | A17  | A18  | A19  | A20  | A21  | A22  | A23  | L    | L          |

**Legend**

L = Logic Low

**Notes**

1. 00h Command (Read) defines the starting address of the 1st half of the register
2. 50h Command (Read) defines the starting address of the spare area of the register
3. The device ignores any additional input of address cycles than required
4. For x16 device, I/O8-I/O15 must be held to logic low when address is input

## 9. Operation Mode: Logic and Command Tables

Read, Reset, Program, and Erase are controlled by fourteen different command operations shown in Table 4. Address input, command input, and data input and output are controlled by the CLE, ALE, CE#, WE#, RE#, and WP# signals, as shown in Table 9.1.

**Table 9.1** Device Bus Operations

| CLE | ALE | CE# | WE#   | RE#   | PRE                 | WP# | FP# | Mode                          |               |
|-----|-----|-----|-------|-------|---------------------|-----|-----|-------------------------------|---------------|
| H   | L   | L   | Pulse | H     | X                   | X   | H   | Read Mode                     | Command Input |
| L   | H   | L   | Pulse | H     | X                   | X   |     |                               | Address Input |
| L   | L   | X   | H     | H     | X                   | X   | H   | During Read (Busy)            |               |
| L   | L   | L   | H     | Pulse | X                   | X   | H   | Sequential Read & Data Output |               |
| H   | L   | L   | Pulse | H     | X                   | H   | H   | Program Mode                  | Command Input |
| L   | H   | L   | Pulse | H     | X                   | H   |     |                               | Address Input |
| H   | L   | L   | Pulse | H     | X                   | H   | L   | Fast Program Mode             | Command Input |
| L   | H   | L   | Pulse | H     | X                   | H   |     |                               | Address Input |
| L   | L   | L   | Pulse | H     | X                   | H   | H   | Data Input                    |               |
| X   | X   | X   | X     | X     | X                   | H   |     | During Program (Busy)         |               |
| X   | X   | X   | X     | X     | X                   | H   |     | During Erase (Busy)           |               |
| X   | X   | X   | X     | X     | X                   | L   |     | Write Protect                 |               |
| X   | X   | H   | X     | X     | 0 V/V <sub>CC</sub> | H/L |     | Standby                       |               |

### Notes

1.  $H = V_{IH}$ ,  $L = V_{IL}$ ,  $X = V_{IH}$  or  $V_{IL}$ .
2.  $H/L = WP\#$  should be biased to CMOS high or CMOS low for standby.

**Table 9.2** Normal Mode Commands

| Function               | 1 <sup>st</sup> Cycle | 2 <sup>nd</sup> Cycle | 3 <sup>rd</sup> Cycle | Command Accepted During Busy State |
|------------------------|-----------------------|-----------------------|-----------------------|------------------------------------|
| Read 1                 | 00h/01h               | -                     | -                     | No                                 |
| Read 2                 | 50h                   | -                     | -                     | No                                 |
| ID Read                | 90h                   | -                     | -                     | No                                 |
| Reset                  | FFh                   | -                     | -                     | Yes                                |
| Page Program           | 80h                   | 10h                   | -                     | No                                 |
| Page Duplicate Program | 00h                   | 8Ah                   | 10h                   | No                                 |
| Block Erase            | 60h                   | D0h                   | -                     | No                                 |
| Status Read            | 70h                   | -                     | -                     | Yes                                |

### Notes

1. It is recommended that the user enter specified commands into the device. Illegal commands may corrupt stored data.
2. During Busy State, only Reset and Status Read commands are accepted. Other commands will be ignored.

Table 9.3 Read Mode States

| Operation       | CLE | ALE | CE# | WE# | RE# | I/O0 to I/O max | Power   |
|-----------------|-----|-----|-----|-----|-----|-----------------|---------|
| Output Select   | L   | L   | L   | H   | L   | Data Output     | Active  |
| Output Deselect | L   | L   | X   | H   | H   | HI-Z            | Active  |
| Standby         | X   | X   | H   | X   | X   | HI-Z            | Standby |

**Notes**

1.  $H = V_{IH}$ ,  $L = V_{IL}$ ,  $X = V_{IH}$  or  $V_{IL}$ , HI-Z = High Impedance
2. Standby is only available when the device is not executing program and erase operations.

## 10. Device Operation

### 10.1 Pointer Operation

The device contains three different areas for x8 devices and two different areas for x16 devices (See [Figure 10.1 on page 31](#)).

The Read commands 00h/01h/50h, along with four address cycles for 512 Mb devices, or three address cycles for 256 Mb and 128 Mb devices, set the address pointer to different areas of the memory array, and they select the most significant column address.

- In x8 devices, the 00h Read 1 command sets the address pointer to the beginning of the first 256 bytes of the main page area, consisting of columns 0 to 255.
- The 01 Read 1 command sets the address pointer to the beginning of the second 256 byte main page area, consisting of columns 256 to 511.
- In x16 devices, the 00h Read 1 command sets the address pointer to the beginning of the 256 words of the main page area, consisting of columns 0 to 255.

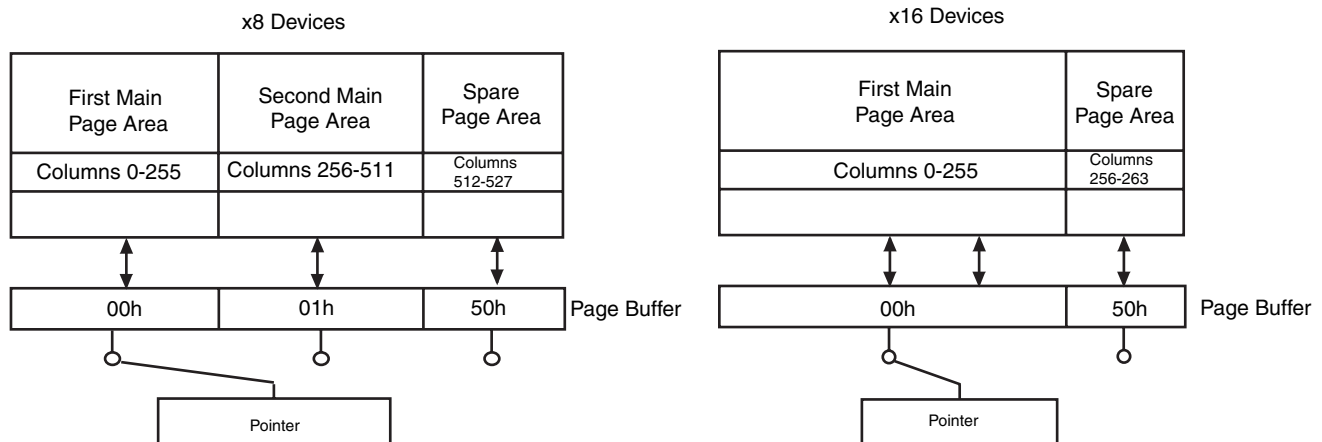
In both the x8 and x16 devices, the 50h Read 2 command sets the address pointer to the beginning of the spare page area, that is, columns 512 to 527 for x8 devices, or columns 256 to 263 for x16 devices.

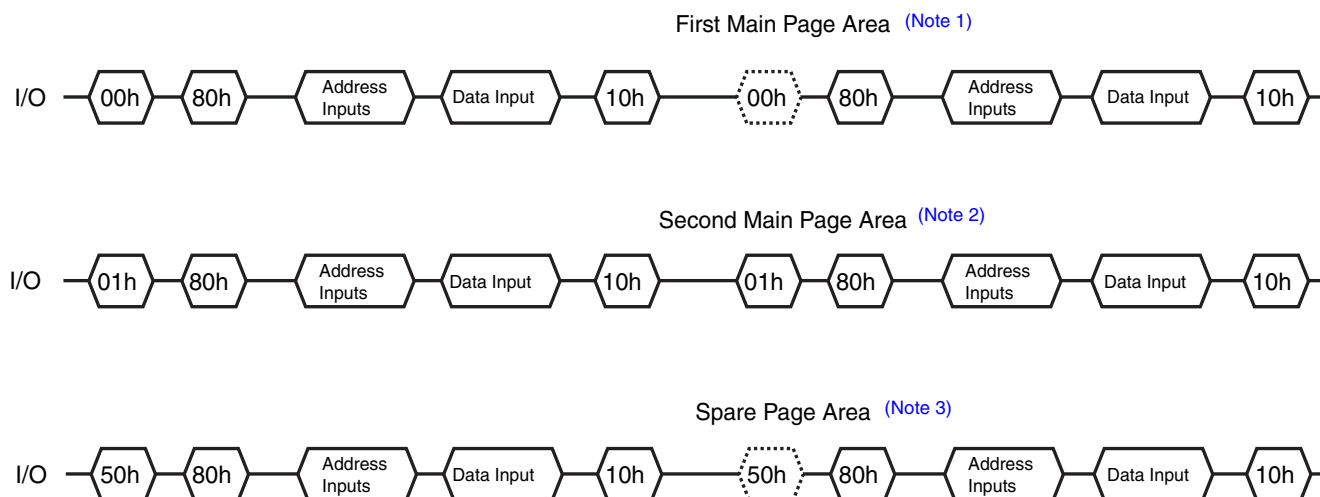
Once the 00h Read 1 or 50h Read 2 commands are issued, the address pointer remains in the respective areas until a new pointer command is issued.

In x8 devices, the 01h Read 1 command moves the address pointer only for the current operation. Once the operation is executed, the address pointer is set to an area consisting of the columns 0 to 255 of the main page area.

The address pointer operations (00h/01h/50h) can also be used before a program operation: the appropriate code can be issued before the program command 80h is issued (see [Figure 10.2 on page 32](#)).

Figure 10.1 Pointer Operations



**Figure 10.2** Pointer Operations for Programming

**Notes**

1. The First Main Page Area, Second Main Page Area or Spare Area can be programmed based on the quantity of input data. Subsequent 00h commands can be omitted.
2. The Second Main Page Area or Spare Area can be programmed based on the quantity of input data. The 01h command must be re-issued before each program.
3. Only the Spare Area can be programmed. Subsequent 50h commands can be omitted.

## 10.2 Read Mode

The device defaults to read mode, pointing at column 0 after power-up or a reset operation. This operation can also be initiated by writing 00h to the command register along with four address input cycles for 512 Mb devices or three address input cycles for 256 Mb and 128 Mb devices.

In x8 devices, there are three types of operations: reading starting at the beginning of the first 256 byte main page area, reading starting at the beginning of the second 256 byte main page area, or reading only the 16 byte spare page area. Upon the final rising edge of the WE# pulse where all address have been latched into the device, there is an initial access delay of loading a 528 byte page content from the flash memory into the page buffer before data can be clocked out of the device. The data is clocked out through consecutive RE# pulses, or the high to low transition of the RE# signal starting from the selected column address up to the last column address. The CE# signal must stay low during the entire read operation or else the operation will automatically be terminated.

The 00h Read command, along with four address cycles for 512 Mb devices, or three address cycles for 256 Mb and 128 Mb devices, sets the address pointer to the beginning of the first 256 byte main page area, consisting of columns 0 to 255. The 01h Read command, along with four address cycles for 512 Mb devices, or three address cycles for 256 Mb and 128 Mb devices, sets the address pointer to the beginning of the second 256 byte main page area, consisting of columns 256 to 511. It may be logical to assume that the 00h Read command automatically set A8 = 0 and the 01h Read command automatically set A8 = 1. The 00h and 01h Read commands define only where the address pointer starts to clock out data from the page buffer. When the first 528 byte page buffer contents has been clocked out, the RY/BY# signal will go into the busy state (logic low) while the next sequential page content is transferred from the flash memory into the page buffer. Once the transfer process has completed, the RY/BY# signal will go into the ready state (high impedance) with the address pointer defaulted to column 0 to enable clocking out of data through consecutive RE# pulses.

In order to read the spare page area, consisting of columns 512 to 527, the 50h Read command along with four address cycles for 512 Mb devices, or three address cycles for 256 Mb and 128 Mb devices, are issued. Enabling the 50h Read command keeps the address pointer positioned to start clocking out data at column 512. Issuing the 00h or 01h Read command alone moves the address pointer out of the spare page area and into the main page area.

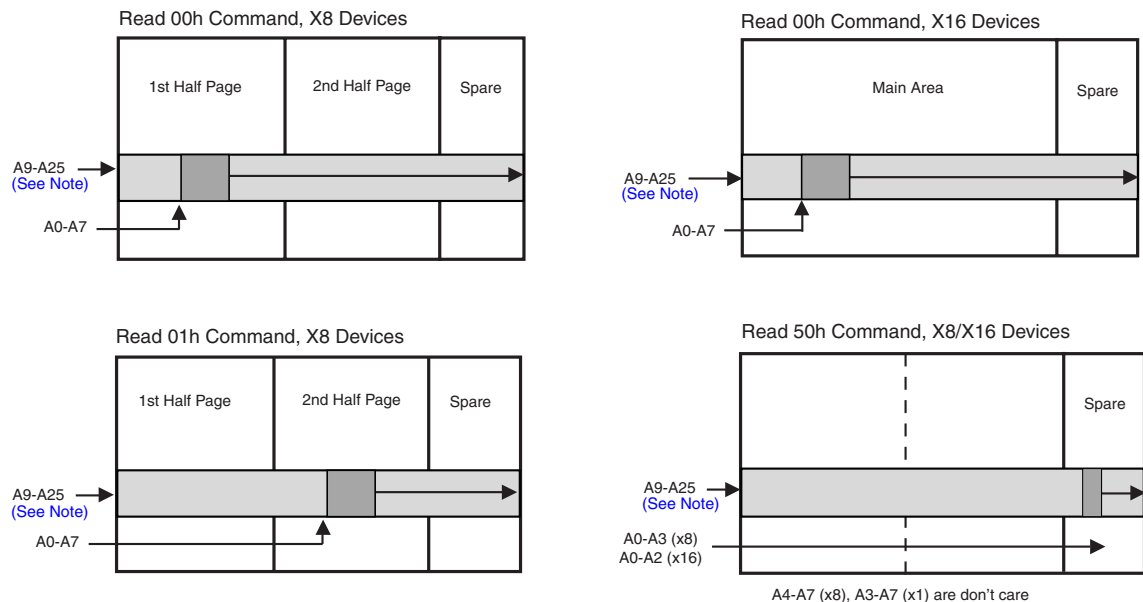
Once the 00h or 50h Read commands have been issued, the read pointer remains in their respective areas also for subsequent operations. If the 01h read command is issued, the read pointer automatically reverts to the 00h area for the next operation.

In x16 devices, there are two types of operations: reading starting at the beginning of the 256 word main page area, or reading only the 8 word spare page area. Upon the final rising edge of the WE# pulse, where all address have been latched into the device, there is an initial access delay of loading a 264-word page content from the flash memory into the page buffer before data can be clocked out of the device. The data is clocked out through consecutive RE# pulses, or the high to low transition of the RE# signal starting from the selected column address up to the last column address. The CE# signal must stay low during the entire read operation, or else the operation is automatically terminated.

The 00h Read command, along with four address cycles for 512 Mb devices, or three address cycles for 256 Mb and 128 Mb devices, sets the address pointer to the beginning of the 256-word main page area, consisting of columns 0 to 255. The 00h Read command defines only where the address pointer starts to clock out data from the page buffer. When the first 264-word page buffer contents is clocked out, the RY/BY# signal goes into the busy state (logic low) while the next sequential page content is transferred from the flash memory into the page buffer. Once the transfer process is complete, the RY/BY# signal goes into the ready state (high impedance) with the address pointer defaulted to column 0, to enable clocking out of data through consecutive RE# pulses.

To read the spare page area, consisting of columns 256 to 264, the 50h Read command along with four address cycles for 512 Mb devices, or three address cycles for 256 Mb and 128 Mb devices, is issued. Enabling the 50h Read command keeps the address pointer positioned to start clocking out data at column 256. Issuing the 00h Read command alone moves the address pointer out of the spare page area and into the main page area.

**Figure 10.3** Read Block Diagram



**Note**

Highest address depends on device density. A25 for S30ML512P. A24 for S30ML256P. A23 for S30ML128P.

## 10.3 Page Program

The 80h command, along with four address cycles for 512 Mb devices or three address cycles for 256 Mb and 128 Mb devices, points to the flash memory area where programming occurs. The device carries out an automatic page program operation when it receives a 10h program confirm command after the address and data have been input into the device. A page is divided into the 512-byte main page area and the 16-byte spare page area.

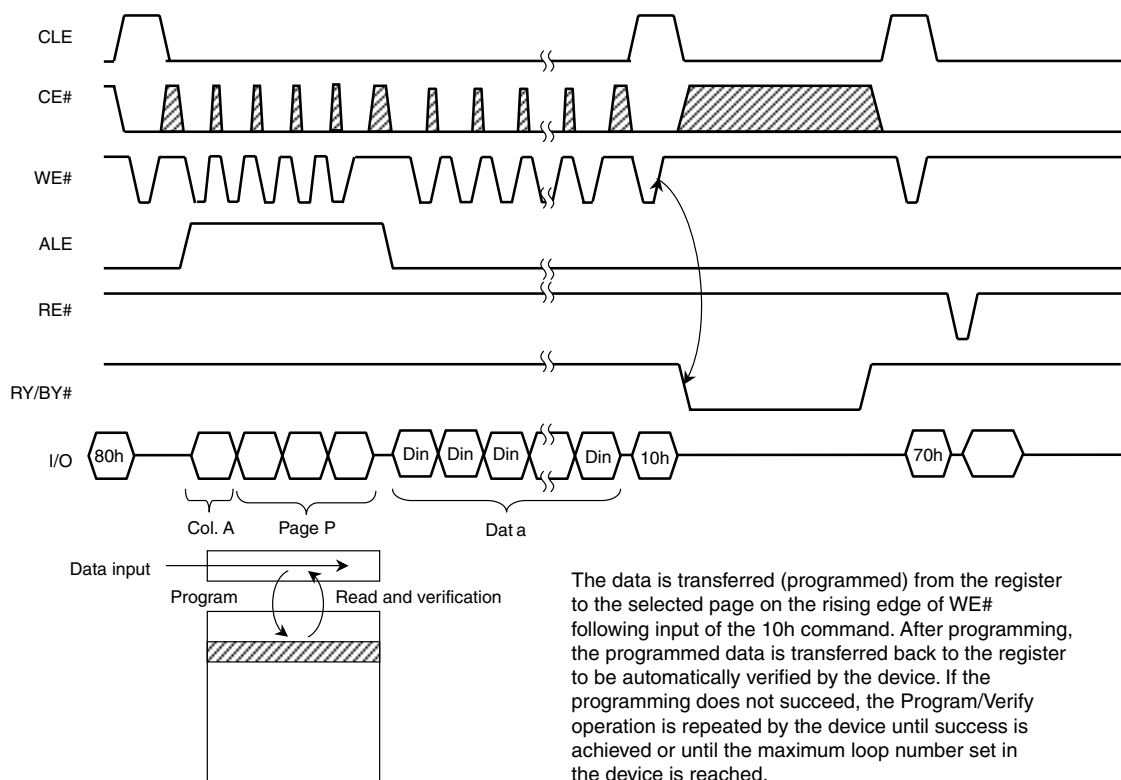
Prior to issuing a Page Program command, a read command can be given to the device in order to move the pointer to the desired column area from which the programming operation will start.

For the x8 device the commands 00h, 01h or 50h can be given to point to the designated area (Column 0, 255 or 512) to be programmed.

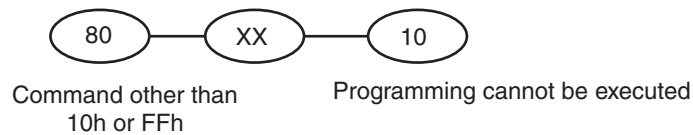
For the x16 device the commands 00h or 50h can be given to point to the designated area (Column 0 or 256 - see [Table 10.2 on page 32](#)) to be programmed.

Once the program process starts, the read status register 70h command may be entered to read the status register. The system controller detects the completion of a program cycle by monitoring the RY/BY# output or bit 6 of the status register. Only the read status register and reset commands are valid while programming operation is executing in progress. When programming operation has completed, bit 0 of status register may be checked for status. The internal write verify detects only errors for 1s that are not successfully programmed to 0s. The command register remains in the read status mode until another valid command is written to the command register.

Figure 10.4 Page Program



Once the serial input 80h command has been input, do not input any command other than 10h related to programming and FFh related to reset. If a command other than 10h, FFh is input into the device, the program operation will not be performed.

**Figure 10.5** Page Program Commands

## 10.4 Page Duplicate Program

The device is capable of loading any page content from the flash memory into the page buffer and re-programming to another page area of the flash memory. By issuing the 00h Read command, along with four address cycles for 512 Mb devices or three address cycles for 256 Mb and 128 Mb devices (source address), any specified page content can be loaded into the page buffer. Issuing the 8Ah Page Duplicate Data Input command, along with four address cycles for 512 Mb devices or three address cycles for 256 Mb and 128 Mb devices (destination address), to indicate where the page content should be re-programmed to, contents stored in the flash memory can be easily moved to enable flash file management.

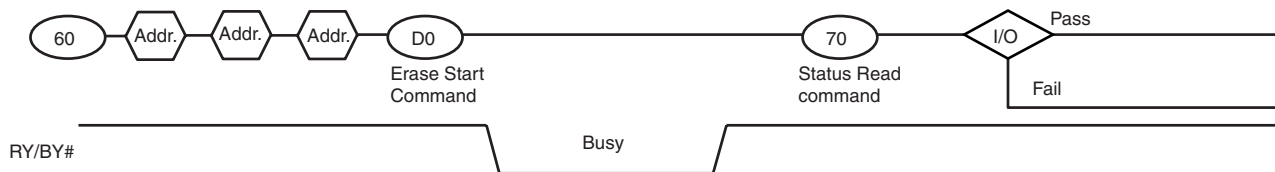
A page is divided into the 512-byte main page area and the 16-byte spare page area.

Once the program process starts, the read status register 70h command may be entered to read the status register. The system controller detects completion of a program cycle by monitoring the RY/BY# output or bit 6 of the status register. Only the read status register and reset command are valid while the programming operation is in progress. Bit 0 of the status register indicates the program cycle was successful. The internal write verify detects only errors for 1s that are not successfully programmed to 0s. The command register remains in the read status mode until another valid command is written to the command register.

## 10.5 Block Erase

A block erase operation is initiated by writing 60h-D0h to the command register, along with three address cycles for 512 Mb devices or two address cycles for 256 Mb and 128 Mb devices (row addresses), of block address to erase a selected block. Please note that page address portion of the row address is ignored.

The block erase operation starts on the rising edge of the WE# signal after the erase start D0h command is input into the device. The devices automatically execute the erase and verify operations.

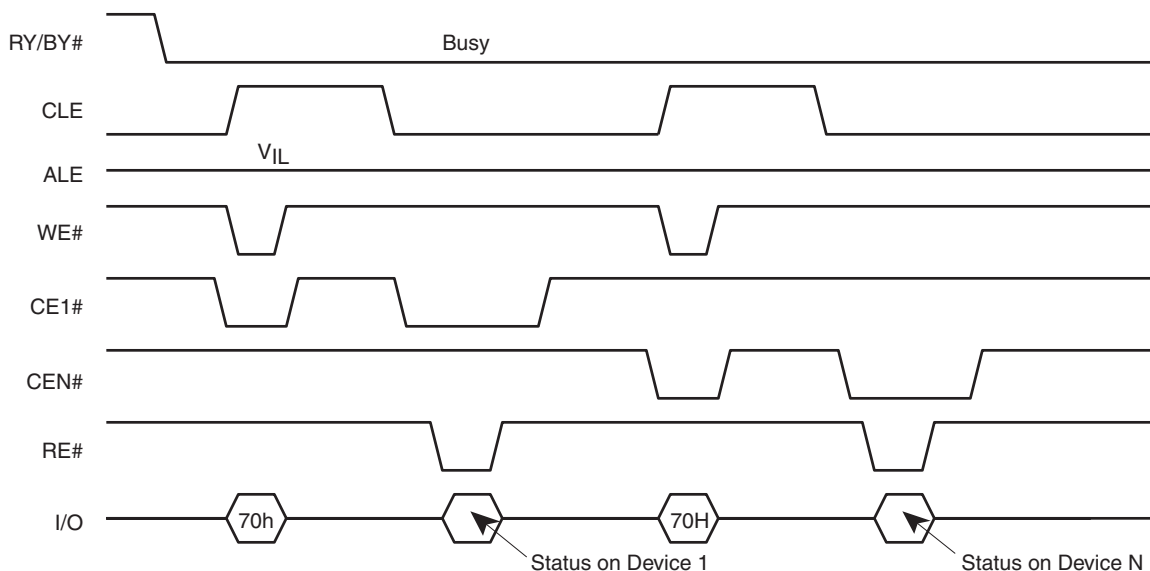
**Figure 10.6** Block Erase

## 10.6 Status Read

The device contains a status register that can be read out to indicate whether a program or erase operation has completed successfully. After writing the status read `70h` command into the command register, a read cycle output the content of the status register onto the I/O pins on the falling edge of either the CE# or the RE# signal, whichever occurs last. Since RY/BY# is an open-drain output, the system may poll the progress of multiple devices with a shared RY/BY# signal. Status Polling occurs when RY/BY# signal is at logic low. The CE# and RE# signals do not need to be toggled to update status register contents.

The device remains in status read mode until another command is issued. Therefore, if the status register is read during a random read cycle, the read `00` command should be issued before starting read cycles.

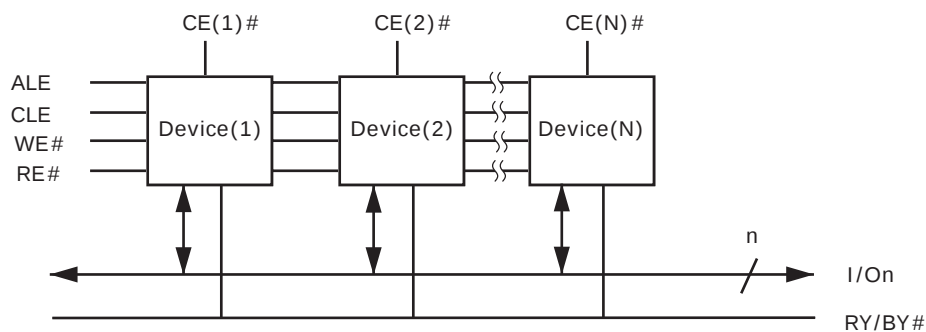
Figure 10.7 Status Read



**Note**

If RY/BY# pin of multiple devices are tied together, status read function can be used to determine status for each device.

Figure 10.8 Example with Multiple Devices

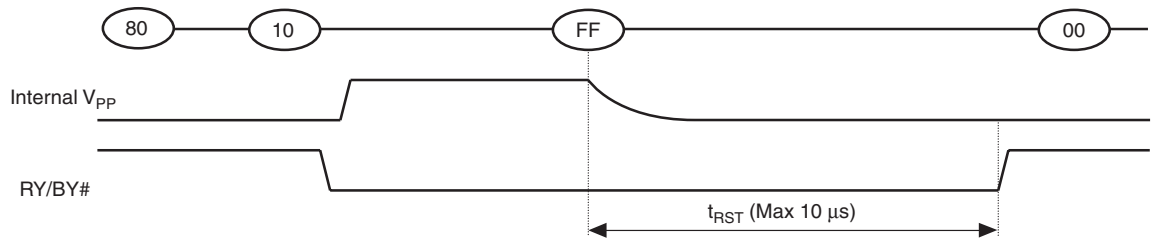


## 10.7 Reset

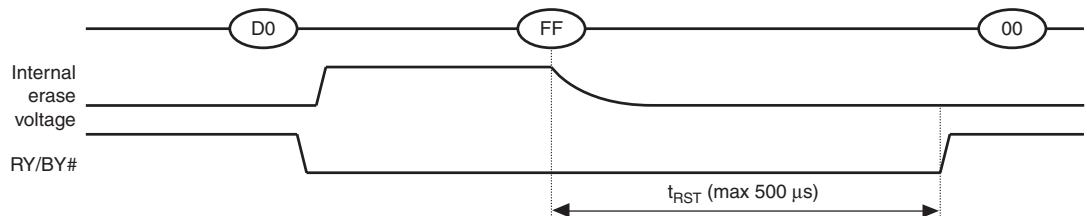
The reset mode stops all operations. For example, during a program or erase operation, the internally generated voltage for the charge pumps is discharged to 0 volts and the device enters the wait state after the reset *FFh* command is issued.

The response to the reset *FFh* command input during various device operations is shown in the following figures.

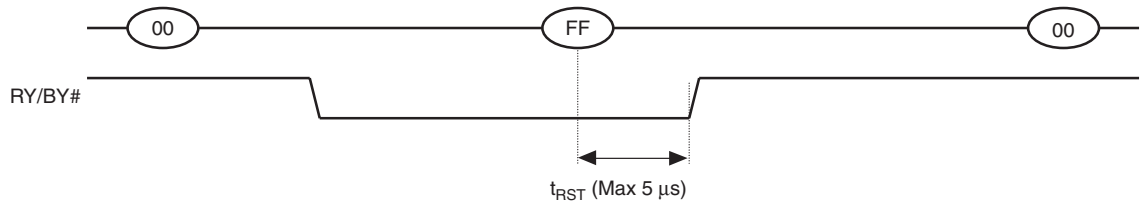
**Figure 10.9** Reset (FFh) Command Input During Programming



**Figure 10.10** Reset (FFh) Command Input During Erasing



**Figure 10.11** Reset (FFh) Command Input During a Read Operation



**Figure 10.12** Status Read Command (70h) Input after a Reset

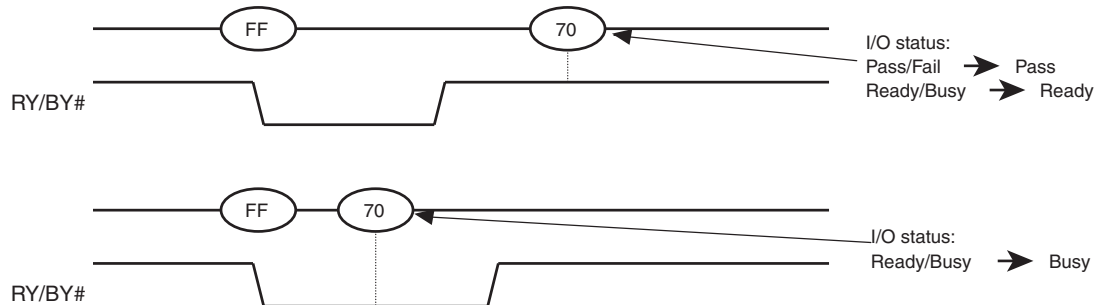
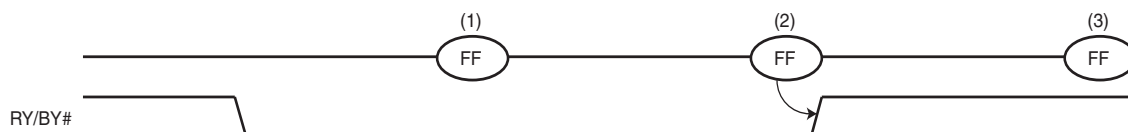


Figure 10.13 Two or More Reset Commands Input in Succession



The second Reset command is invalid since the device has not internally completed the first Reset command.

## 10.8 Fast Program/Erase Mode

The Fast Program/Erase Mode enables faster programming and erasing performance through increased device current with  $V_{CC} = 3.3V$  to  $3.6V$ . Table 10.1 on page 38 shows the program and erase times when the device is in the Fast Program/Erase mode. See *DC Characteristics—CMOS Compatible* on page 18 for the Fast Program/Erase Mode currents.

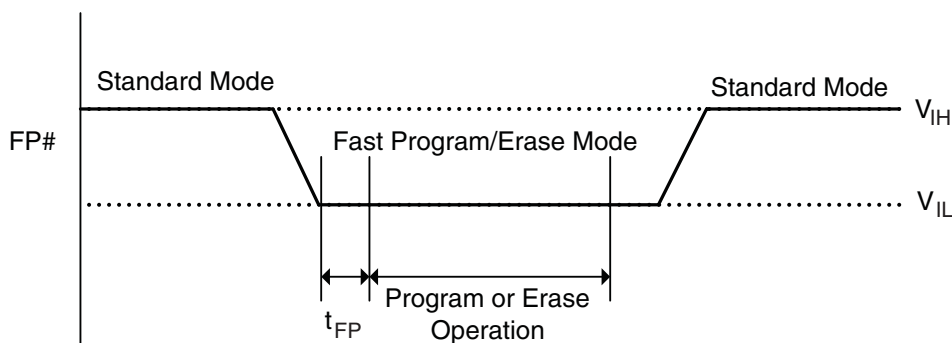
Table 10.1 Fast Program/Erase Mode Performance

| Fast Program/Erase Mode | Typ. | Unit |
|-------------------------|------|------|
| Program Time            | 2.9  | MB/s |
| Block Erase Time        | 3.1  | MB/s |

The FP# pin allows the user to choose between operating in the Fast Program/Erase mode or the Standard mode. To switch the device into Fast Program mode, first apply  $V_{IL}$  to the FP# pin and wait 100ns ( $t_{FP}$ ) before issuing a new program or erase command. Hold the FP# pin at  $V_{IL}$  for the duration of the program or erase command execution. Failure to meet this requirement results in a program or erase failure.

In the Fast Program/Erase Mode, only program, erase and read status commands are allowed. To read from the device and operate in Standard Mode, the FP# pin must be held at  $V_{IH}$  level.

Figure 10.14 Timing diagram for Fast Program/Erase Mode



## 10.9 ID Read Operation

The ID Read (90h command) allows the host system software to read device specific information from the Flash. This allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, and forward- and backward-compatible for the specified Flash device families. The device information provided by the ID Read command includes: Device Size, x8/x16 data bus, ECC requirements, Block Size, Page Size, etc. (see Table 10.2 on page 39).

Figure 10.15 ID Read Operation Timing Diagram

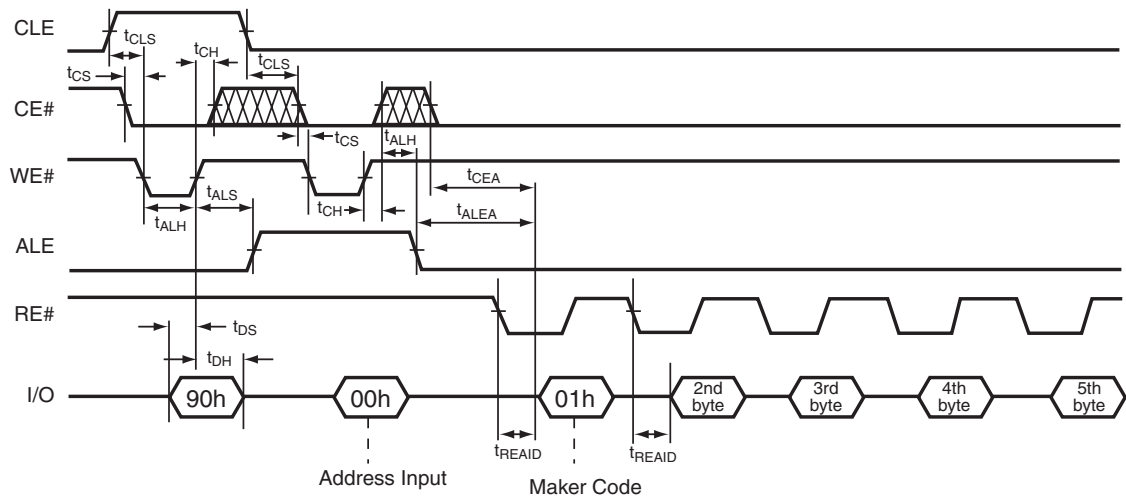


Table 10.2 ID Definition Table

| Byte | Description                                              | Hex Data                                                                                                                                                                                                                                                                                                      |
|------|----------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1    | Manufacturer Code                                        | 01h                                                                                                                                                                                                                                                                                                           |
| 2    | Device Code 1 <sup>st</sup> Byte                         | 512Mb x8 = 76h<br>512Mb x16 = 56h<br>256Mb x8 = 75h<br>256Mb x16 = 55h<br>128Mb x8 = 73h<br>128Mb x16 = 53h                                                                                                                                                                                                   |
| 3    | Device Code 2 <sup>nd</sup> Byte                         | Devices with up to 2% bad blocks:<br>512Mb x8 = 00h<br>512Mb x16 = 00h<br>256Mb x8 = 00h<br>256Mb x16 = 00h<br>128Mb x8 = 00h<br>128Mb x16 = 04h<br>Devices with guaranteed 100% valid blocks:<br>512Mb x8 = 01h<br>512Mb x16 = 01h<br>256Mb x8 = 01h<br>256Mb x16 = 01h<br>128Mb x8 = 01h<br>128Mb x16 = 03h |
| 4    | Block Size, Simultaneous Operation Programmed Pages, RFU | 01h                                                                                                                                                                                                                                                                                                           |
| 5    | Page Size, Spare Size, RFU                               | 10h                                                                                                                                                                                                                                                                                                           |
| 6    | Other MCP identifiers                                    | TBD                                                                                                                                                                                                                                                                                                           |

**Note**

In x16, I/O15-I/O8 = 00h

Table 10.3 ID Bytes (Sheet 1 of 2)

| Bits        |   |   |   |   |   |   |   | Information                                 |
|-------------|---|---|---|---|---|---|---|---------------------------------------------|
| 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                             |
| 4th ID Byte |   |   |   |   |   |   |   |                                             |
| X           | X | X | X | X | 0 | 0 | 0 | Block Size: 128Kbytes                       |
| X           | X | X | X | X | 0 | 0 | 1 | Block Size: 512KBytes                       |
| X           | X | X | X | X | 0 | 1 | 0 | Block Size: 2048KBytes                      |
| X           | X | X | 0 | 0 | X | X | X | Simultaneous Operation Programmed Pages = 1 |
| X           | X | X | 0 | 1 | X | X | X | Simultaneous Operation Programmed Pages = 2 |

**Table 10.3 ID Bytes (Sheet 2 of 2)**

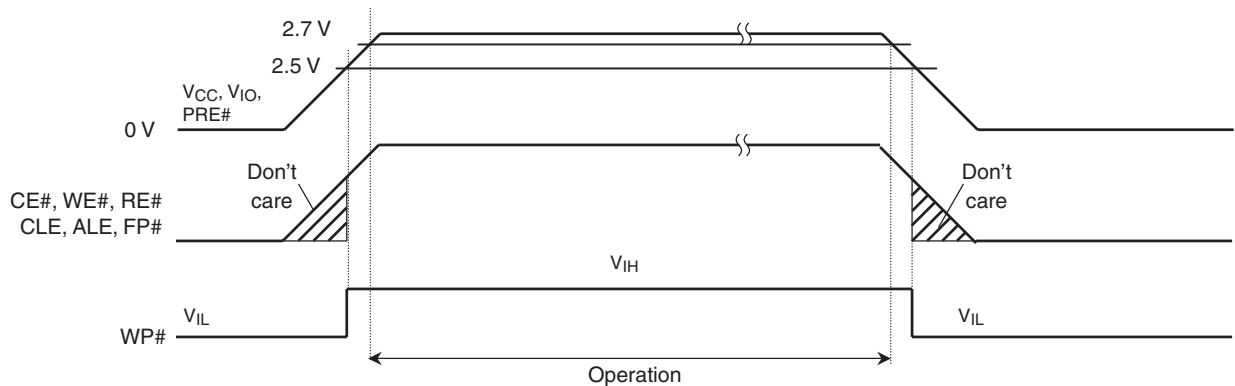
| Bits               |   |   |   |   |   |   |   | Information                                             |
|--------------------|---|---|---|---|---|---|---|---------------------------------------------------------|
| 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                                         |
| X                  | X | X | 1 | 0 | X | X | X | Simultaneous Operation Programmed Pages = 4             |
| X                  | X | X | 1 | 1 | X | X | X | Simultaneous Operation Programmed Pages = 8             |
| <b>5th ID Byte</b> |   |   |   |   |   |   |   |                                                         |
| X                  | X | X | X | X | 0 | 0 | 0 | Page Size: 512 bytes                                    |
| X                  | X | X | X | X | 0 | 0 | 1 | Page Size: 1024 bytes                                   |
| X                  | X | X | X | X | 0 | 1 | 0 | Page Size: 2048 bytes                                   |
| X                  | X | X | X | X | 0 | 1 | 1 | Page Size: 4096 bytes                                   |
| X                  | X | X | X | X | 1 | 0 | 0 | Page Size: 8192 bytes                                   |
| X                  | X | 0 | 0 | 0 | X | X | X | Spare Size: 0 bytes                                     |
| X                  | X | 0 | 0 | 1 | X | X | X | Spare Size: 8 bytes                                     |
| X                  | X | 0 | 1 | 0 | X | X | X | Spare Size: 16 bytes                                    |
| X                  | X | 0 | 1 | 1 | X | X | X | Spare Size: 32 bytes                                    |
| X                  | X | 1 | 0 | 0 | X | X | X | Spare Size: 64 bytes                                    |
| <b>6th ID Byte</b> |   |   |   |   |   |   |   |                                                         |
| X                  | X | X | X | X | X | X | X | RAM & Other MCP Identifiers:<br>Reserved for Future Use |

## 11. Application Notes

### 11.1 Power-on/off Sequence

The WP# signal is useful for protecting against data corruption at power-on/off. Figure 11.1 shows the required timing sequence. The WP# signal may be negated any time after  $V_{CC}$  reaches 2.5 V and CE# is kept high in the power up sequence.

Figure 11.1 Power-On/off Sequence



After power-on, access the device only after the RY/BY# pin indicates the device is ready. Do not issue any commands to the device while RY/BY# is busy.

### 11.2 Auto Load Page 0 After Power-On

With the PRE pulled high, the device automatically reads page 0 into the page buffer after power-up, without the need to issue a read command. Auto load page 0 is enabled by the PRE input signal. To disable this function PRE must be tied low ( $V_{SS}$ ). PRE should never be left floating.

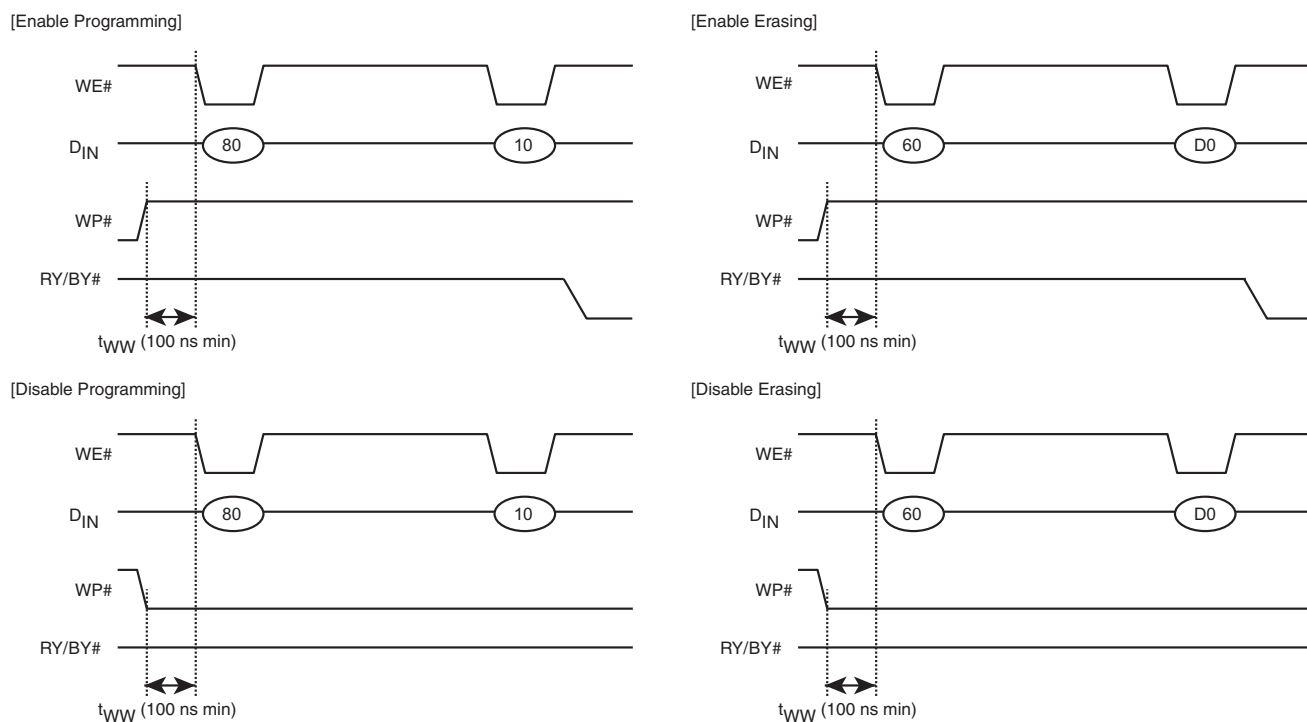
### 11.3 Bad Block Management for Devices With Up to 2% Bad Blocks

Spansion S30ML512P, S30ML256P, S30ML128P, Model Numbers 50, 51, 52, 53, are shipped with all the locations within valid blocks erased (all bits equal to 1). Bad Block information is written at the factory before shipment. A Bad Block is indicated by 6th byte (x8 device) or the 1st word (x16) of the spare area in the 1st or 2nd page of the block containing a "non FFh" value.

## 11.4 When WP# Signal Goes Low

The Erase and Program operations are automatically reset when WP# goes low. The WP# must not toggle between the 1st cycle and 2nd cycle or the erase and program operations will be disabled. The operations are enabled and disabled as shown in Figure 11.2.

Figure 11.2 WP# Functions



## 12. Revision History

| Section                                        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Revision 01 (December 14, 2006)</b>         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|                                                | Initial release                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>Revision 02 (April 24, 2007)</b>            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| Global                                         | Deleted all references to Xtreme mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Performance Characteristics                    | Changed block erase time                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Electrical Specifications                      | Added maximum positive and negative overshoot figures                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| DC Characteristics                             | Moved $I_{SB}$ specifications to $V_{IO}$ tables and changed test conditions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| AC Characteristics                             | Changed minimum $t_{DS}$ , $t_{DH}$ , $t_{RP}$ specifications                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| AC Test Conditions                             | Added $V_{IO}$ condition to table                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Programming And Erase Characteristics          | Changed specifications in table                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| Reset                                          | Corrected unit of measurement to $\mu s$ in figures                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Read ID Operation                              | <i>ID Definition Table</i> : Changed hex data for byte 5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| When WP# Signal Goes Low                       | Added section                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>Revision 03 (April 8, 2008)</b>             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| Global                                         | Added x8 and x16 versions of VBW055 Package<br>Changed x8 $V_{IO}$ AC Timing Parameters<br>Corrected Grammatical Errors                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| General Description                            | Added S30ML512P to <i>Device Organization</i> table                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Valid Combinations                             | Added VBE to Note 3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Performance Characteristics                    | Corrected Program Current Consumption Value                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Pin Descriptions                               | Reworded RY/BY# description<br>Reworded FP# description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| Capacitance                                    | Incorporated Note 3 into table <i>No <math>V_{IO}</math> Pin</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| Valid Blocks                                   | Combined table <i>Devices with up to 2% Invalid Blocks (ECC-Required)</i> and table <i>Devices with 100% Valid Blocks (ECC-Free)</i> into one table <i>Devices with up to 2% Invalid Blocks (ECC-Required)</i>                                                                                                                                                                                                                                                                                                                                                                                                        |
| DC Characteristics                             | Added note to $I_{CC3}$ and $I_{CC5}$<br>Table No $V_{IO}$ Pin <ul style="list-style-type: none"> <li>Changed <math>I_{OL}</math> typical to 12 mA</li> <li>Changed <math>V_{IH}</math> overshoot to <math>V_{CC}+2.0V</math></li> <li>Changed <math>V_{IL}</math> undershoot to <math>-2.0V</math></li> </ul> Table With $V_{IO}$ Pin, $V_{IO} = 1.8V$ <ul style="list-style-type: none"> <li>Changed <math>I_{OL}</math> min to 2mA and typical to 3 mA</li> <li>Changed <math>V_{IH}</math> overshoot to <math>V_{CC}+2.0V</math></li> <li>Changed <math>V_{IL}</math> undershoot to <math>-2.0V</math></li> </ul> |
| AC Characteristics                             | Changed $t_{REH}$ min (x8, no $V_{IO}$ ) to 5 ns                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| Figure - Page Duplicate Program Timing Diagram | Added note regarding number of address cycles                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Figure - Block Erase Timing Diagram            | Corrected note regarding number of address cycles                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Table - Device Bus Operations                  | Changed PRE state for Standby Mode to 0V / $V_{CC}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Pointer Operation                              | Modified section by removing redundant comments                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| Read Mode                                      | Changed 'logic high' to 'high impedance' in third and seventh paragraph                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| Page Program                                   | Modified first and third paragraph<br>Combined sixth and seventh paragraph                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| Figure - Page Program                          | Removed fifth address cycle from diagram                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Page Duplicate Program                         | Modified third paragraph                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Figure - Block Erase                           | Corrected figure to include address blocks and 'erase start command' for D0h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

| Section                                                   | Description                                                                                    |
|-----------------------------------------------------------|------------------------------------------------------------------------------------------------|
| Status Read                                               | Modified first paragraph                                                                       |
| Figure - Two or More Reset Commands Input in Succession   | Changed note to explain 2nd RESET command is invalid                                           |
| Fast Program/Erase Mode                                   | Added comment Fast Program/Erase Mode operates over $V_{CC} = 3.0V$ to $3.6V$                  |
| ID Read Operation                                         | Reworded section                                                                               |
| Auto Load Page 0 After Power-On                           | Modified first paragraph<br>Changed $V_{IL}$ to $V_{SS}$<br>Deleted second and third paragraph |
| Bad Block Management for Devices With Up to 2% Bad Blocks | Modified first paragraph                                                                       |
| When WP# Signal Goes Low                                  | Added comment that WP# must not toggle between first and second cycle                          |

**Colophon**

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