

74HC154; 74HCT154

4-to-16 line decoder/demultiplexer

Rev. 10 — 5 August 2024

Product data sheet

1. General description

The 74HC154; 74HCT154 is a 4-to-16 line decoder/demultiplexer. It decodes four binary weighted address inputs (A0 to A3) to sixteen mutually exclusive outputs (Y0 to Y15). The device features two input enable (E0 and E1) inputs. A HIGH on either of the input enables forces the outputs HIGH. The device can be used as a 1-to-16 demultiplexer by using one of the enable inputs as the multiplexed data input. When the other enable input is LOW the addressed output will follow the state of the applied data. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into 16 mutually-exclusive outputs
- Input levels:
 - For 74HC154: CMOS level
 - For 74HCT154: TTL level
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC154D 74HCT154D	-40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74HC154PW 74HCT154PW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74HC154BQ 74HCT154BQ	-40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

4. Functional diagram

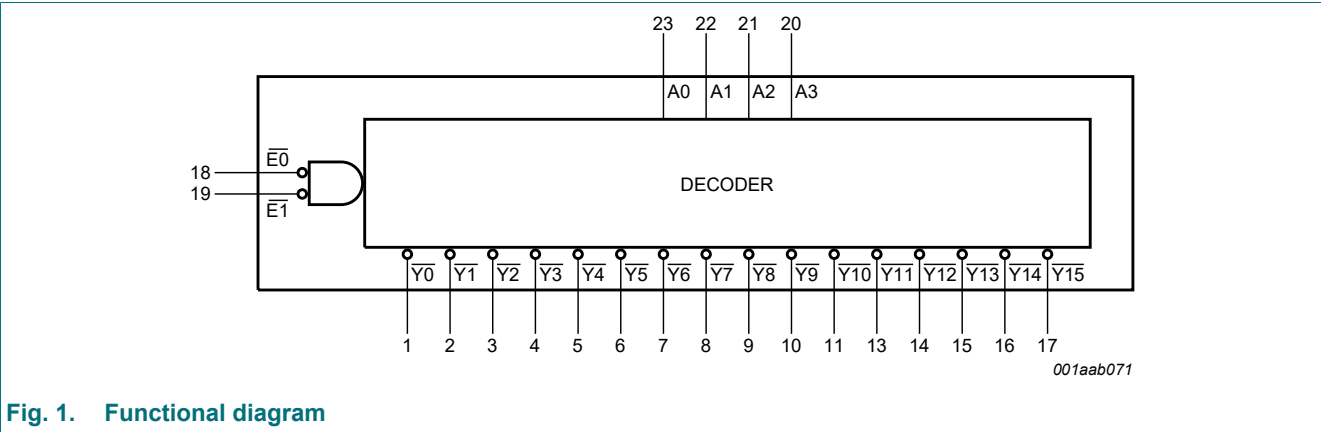


Fig. 1. Functional diagram

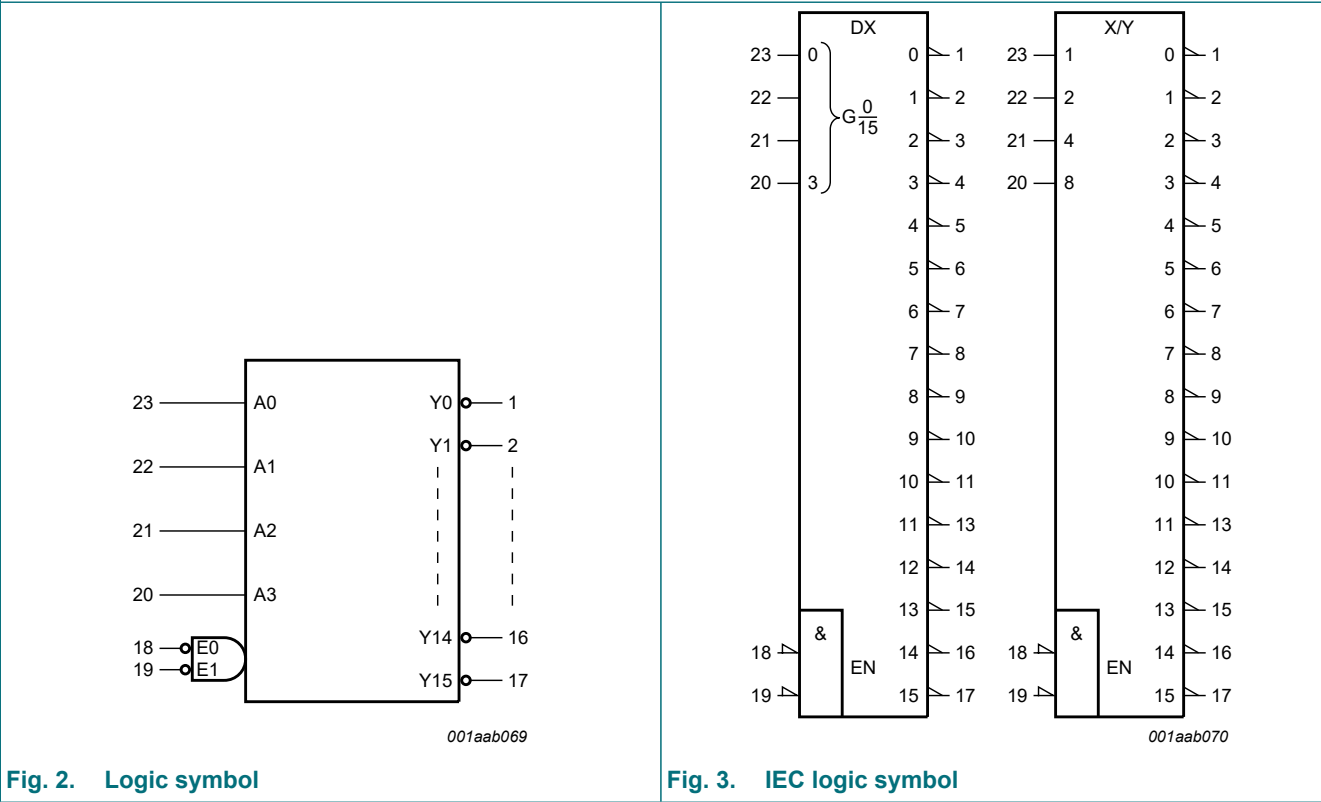


Fig. 2. Logic symbol

Fig. 3. IEC logic symbol

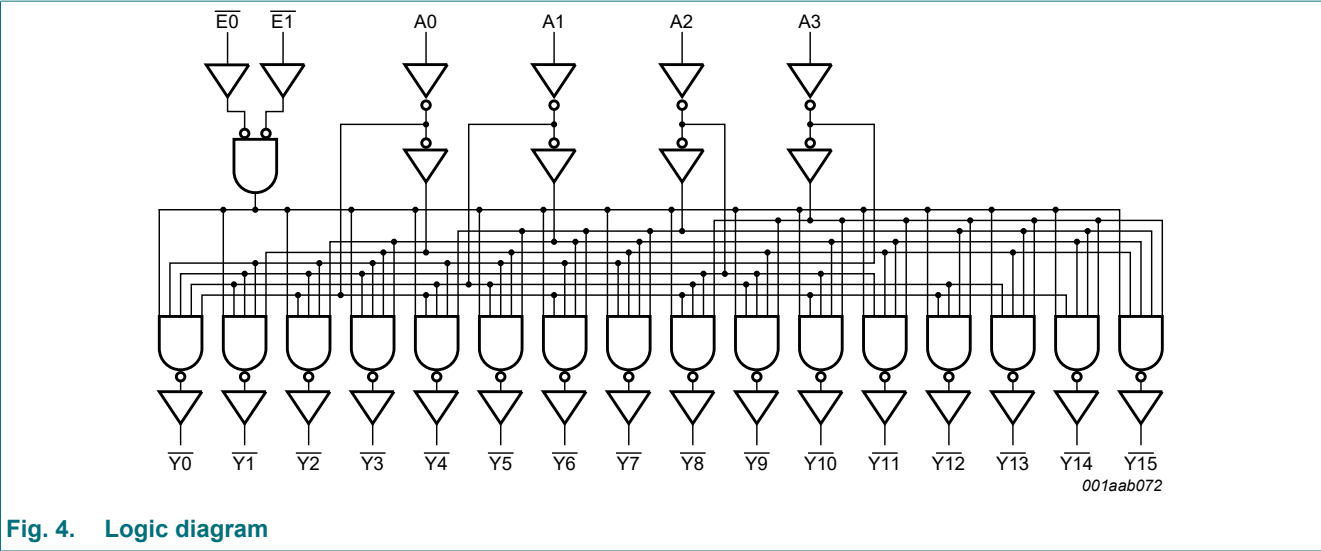
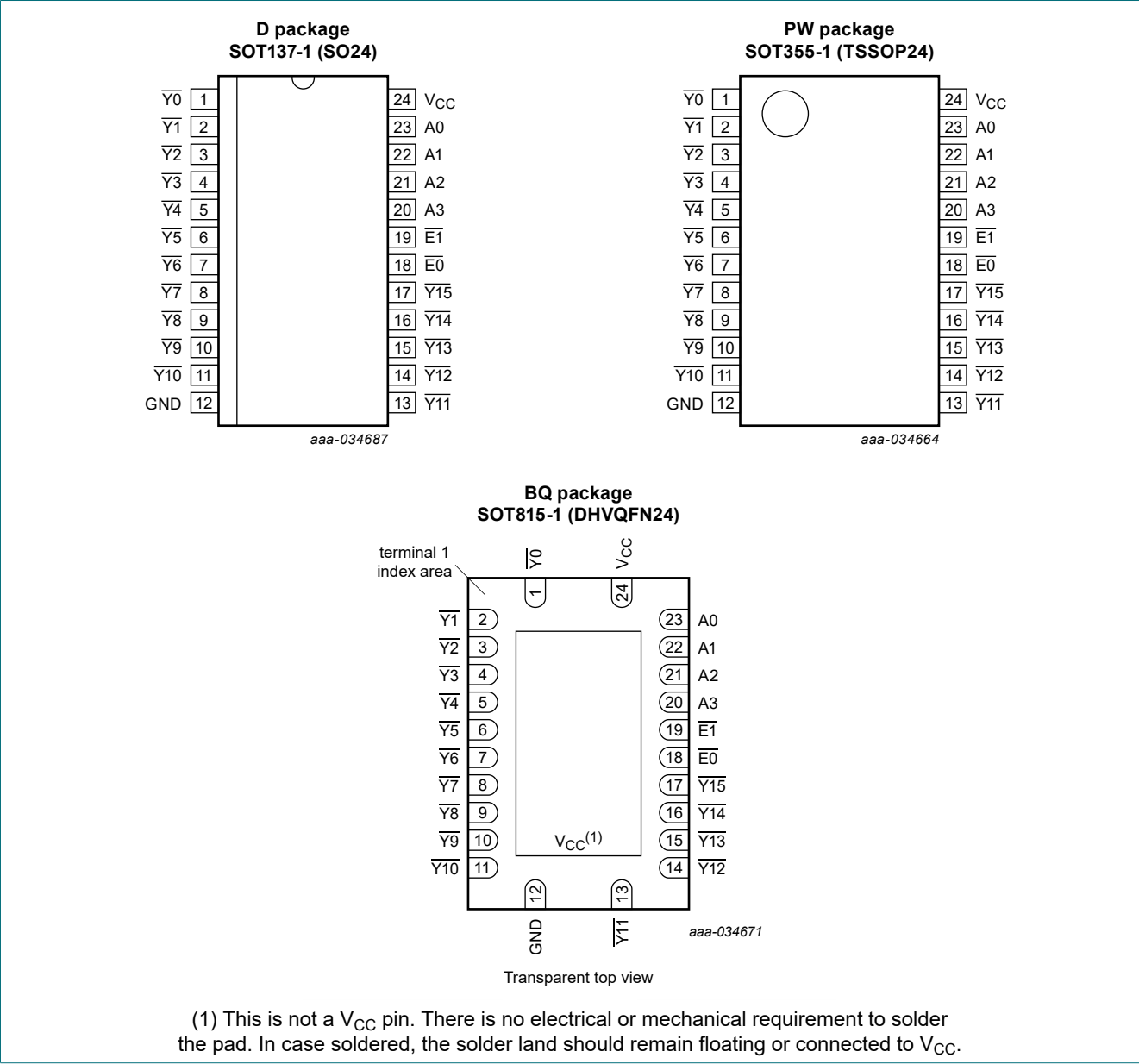


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, 17	data output (active LOW)
GND	12	ground (0 V)
E0, E1	18, 19	enable input (active LOW)
A0, A1, A2, A3	23, 22, 21, 20	address input
VCC	24	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input						Output															
E0	E1	A0	A1	A2	A3	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
		H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
		L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
		H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
		L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
		H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
		L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
		H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
		L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
		H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
		L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
		H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
		L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
		H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
		L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
		H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V [1]	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V [1]	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V [1]	-	±25	mA
I _{CC}	supply current	[1]	-	50	mA
I _{GND}	ground current	[1]	-	-50	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT137-1 (SO24) package: P_{tot} derates linearly with 16.2 mW/K above 119 °C.
For SOT355-1 (TSSOP24) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT815-1 (DHVQFN24) package: P_{tot} derates linearly with 15.0 mW/K above 117 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions
Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC154			74HCT154			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics 74HC154

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		V _{CC} = 2.0 V; I _O = -20 µA	1.9	2.0	-	V
		V _{CC} = 4.5 V; I _O = -20 µA	4.4	4.5	-	V
		V _{CC} = 6.0 V; I _O = -20 µA	5.9	6.0	-	V
		V _{CC} = 4.5 V; I _O = -4.0 mA	3.98	4.32	-	V
		V _{CC} = 6.0 V; I _O = -5.2 mA	5.48	5.81	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		V _{CC} = 2.0 V; I _O = 20 µA	-	0	0.1	V
		V _{CC} = 4.5 V; I _O = 20 µA	-	0	0.1	V
		V _{CC} = 6.0 V; I _O = 20 µA	-	0	0.1	V
		V _{CC} = 4.5 V; I _O = 4.0 mA	-	0.15	0.26	V
		V _{CC} = 6.0 V; I _O = 5.2 mA	-	0.16	0.26	V
I _I	input leakage current	V _{CC} = 6.0 V; V _I = V _{CC} or GND	-	-	±0.1	µA
I _{CC}	supply current	V _{CC} = 6.0 V; V _I = V _{CC} or GND; I _O = 0 A	-	-	8.0	µA
C _I	input capacitance		-	3.5	-	pF
T _{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		V _{CC} = 2.0 V; I _O = -20 µA	1.9	-	-	V
		V _{CC} = 4.5 V; I _O = -20 µA	4.4	-	-	V
		V _{CC} = 6.0 V; I _O = -20 µA	5.9	-	-	V
		V _{CC} = 4.5 V; I _O = -4.0 mA	3.84	-	-	V
		V _{CC} = 6.0 V; I _O = -5.2 mA	5.34	-	-	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		V _{CC} = 2.0 V; I _O = 20 µA	-	-	0.1	V
		V _{CC} = 4.5 V; I _O = 20 µA	-	-	0.1	V
		V _{CC} = 6.0 V; I _O = 20 µA	-	-	0.1	V
		V _{CC} = 4.5 V; I _O = 4.0 mA	-	-	0.33	V
		V _{CC} = 6.0 V; I _O = 5.2 mA	-	-	0.33	V
I _I	input leakage current	V _{CC} = 6.0 V; V _I = V _{CC} or GND	-	-	±1.0	µA
I _{CC}	supply current	V _{CC} = 6.0 V; V _I = V _{CC} or GND; I _O = 0 A	-	-	80	µA
T _{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		V _{CC} = 2.0 V; I _O = -20 µA	1.9	-	-	V
		V _{CC} = 4.5 V; I _O = -20 µA	4.4	-	-	V
		V _{CC} = 6.0 V; I _O = -20 µA	5.9	-	-	V
		V _{CC} = 4.5 V; I _O = -4.0 mA	3.7	-	-	V
		V _{CC} = 6.0 V; I _O = -5.2 mA	5.2	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		V _{CC} = 2.0 V; I _O = 20 µA	-	-	0.1	V
		V _{CC} = 4.5 V; I _O = 20 µA	-	-	0.1	V
		V _{CC} = 6.0 V; I _O = 20 µA	-	-	0.1	V
		V _{CC} = 4.5 V; I _O = 4.0 mA	-	-	0.4	V
		V _{CC} = 6.0 V; I _O = 5.2 mA	-	-	0.4	V
I _I	input leakage current	V _{CC} = 6.0 V; V _I = V _{CC} or GND	-	-	±0.1	µA
I _{CC}	supply current	V _{CC} = 6.0 V; V _I = V _{CC} or GND; I _O = 0 A	-	-	160	µA

Table 7. Static characteristics 74HCT154

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		V _{CC} = 4.5 V; I _O = -20 µA	4.4	4.5	-	V
		V _{CC} = 4.5 V; I _O = -4 mA	3.98	4.32	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		V _{CC} = 4.5 V; I _O = 20 µA	-	0	0.1	V
		V _{CC} = 4.5 V; I _O = 4 mA	-	0.15	0.25	V
I _I	input leakage current	V _{CC} = 5.5 V; V _I = V _{CC} or GND	-	-	±0.1	µA
I _{CC}	supply current	V _{CC} = 5.5 V; V _I = V _{CC} or GND; I _O = 0 A	-	-	8.0	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 4.5 V to 5.5 V; V _I = V _{CC} - 2.1 V; I _O = 0 A	-	-	360	µA
C _I	input capacitance		-	3.5	-	pF
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		V _{CC} = 4.5 V; I _O = -20 µA	4.4	-	-	V
		V _{CC} = 4.5 V; I _O = -4 mA	3.84	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		V _{CC} = 4.5 V; I _O = 20 µA	-	-	0.1	V
		V _{CC} = 4.5 V; I _O = 4 mA	-	-	0.33	V
I _I	input leakage current	V _{CC} = 5.5 V; V _I = V _{CC} or GND	-	-	±1.0	µA
I _{CC}	supply current	V _{CC} = 5.5 V; V _I = V _{CC} or GND; I _O = 0 A	-	-	80	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 4.5 V to 5.5 V; V _I = V _{CC} - 2.1 V; I _O = 0 A	-	-	450	µA
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		V _{CC} = 4.5 V; I _O = -20 µA	4.4	-	-	V
		V _{CC} = 4.5 V; I _O = -4 mA	3.7	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		V _{CC} = 4.5 V; I _O = 20 µA	-	-	0.1	V
		V _{CC} = 4.5 V; I _O = 4 mA	-	-	0.4	V
I _I	input leakage current	V _{CC} = 5.5 V; V _I = V _{CC} or GND	-	-	±1.0	µA
I _{CC}	supply current	V _{CC} = 5.5 V; V _I = V _{CC} or GND; I _O = 0 A	-	-	160	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 4.5 V to 5.5 V; V _I = V _{CC} - 2.1 V; I _O = 0 A	-	-	490	µA

10. Dynamic characteristics

Table 8. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 7.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC154										
t _{pd}	propagation delay	An to $\overline{Y_n}$; see Fig. 5 [1]								
		V _{CC} = 2.0 V	-	36	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	13	30	-	38	-	45	ns
		V _{CC} = 5 V; C _L = 15 pF	-	11	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	10	26	-	33	-	38	ns
		$\overline{E_n}$ to $\overline{Y_n}$; see Fig. 6								
		V _{CC} = 2.0 V	-	39	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	14	30	-	38	-	45	ns
		V _{CC} = 5 V; C _L = 15 pF	-	11	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	11	26	-	33	-	38	ns
t _t	transition time	see Fig. 5 and Fig. 6 [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C _{PD}	power dissipation capacitance	per gate; V _I = GND to V _{CC} [3]	-	60	-	-	-	-	-	pF
74HCT154										
t _{pd}	propagation delay	An to $\overline{Y_n}$; see Fig. 5 [1]								
		V _{CC} = 4.5 V	-	16	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF	-	13	-	-	-	-	-	ns
		$\overline{E_n}$ to $\overline{Y_n}$; see Fig. 6								
		V _{CC} = 4.5 V	-	15	32	-	40	-	48	ns
		V _{CC} = 5 V; C _L = 15 pF	-	13	-	-	-	-	-	ns
t _t	transition time	see Fig. 5 and Fig. 6 [2]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
C _{PD}	power dissipation capacitance	per gate; V _I = GND to (V _{CC} - 1.5 V) [3]	-	60	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}

[2] t_t is the same as t_{TLH} and t_{THL}

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms and test circuit

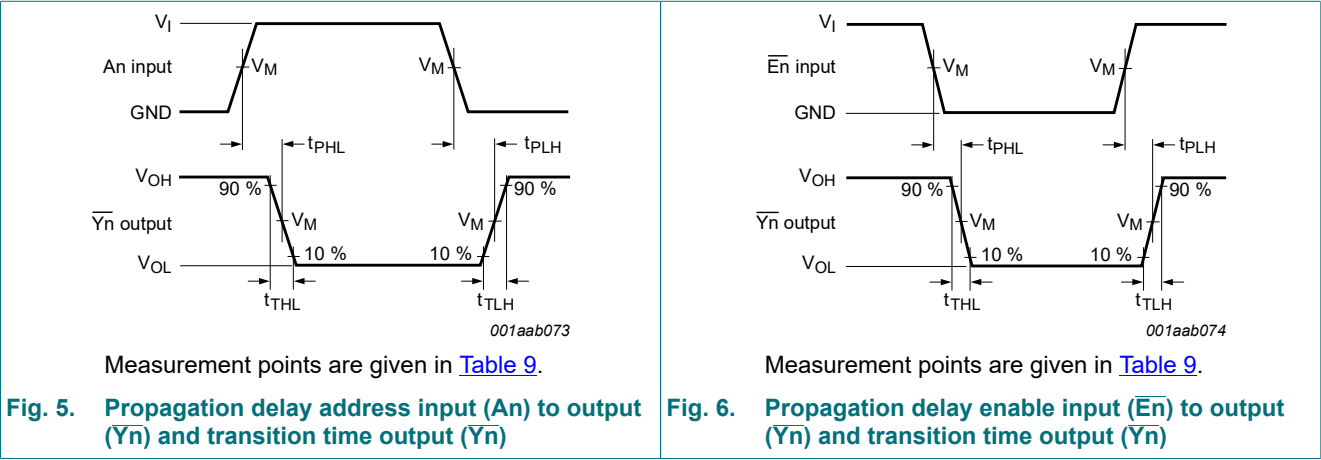


Table 9. Measurement points

Type	Input	Output
	V _M	V _M
74HC154	0.5V _{CC}	0.5V _{CC}
74HCT154	1.3 V	1.3 V

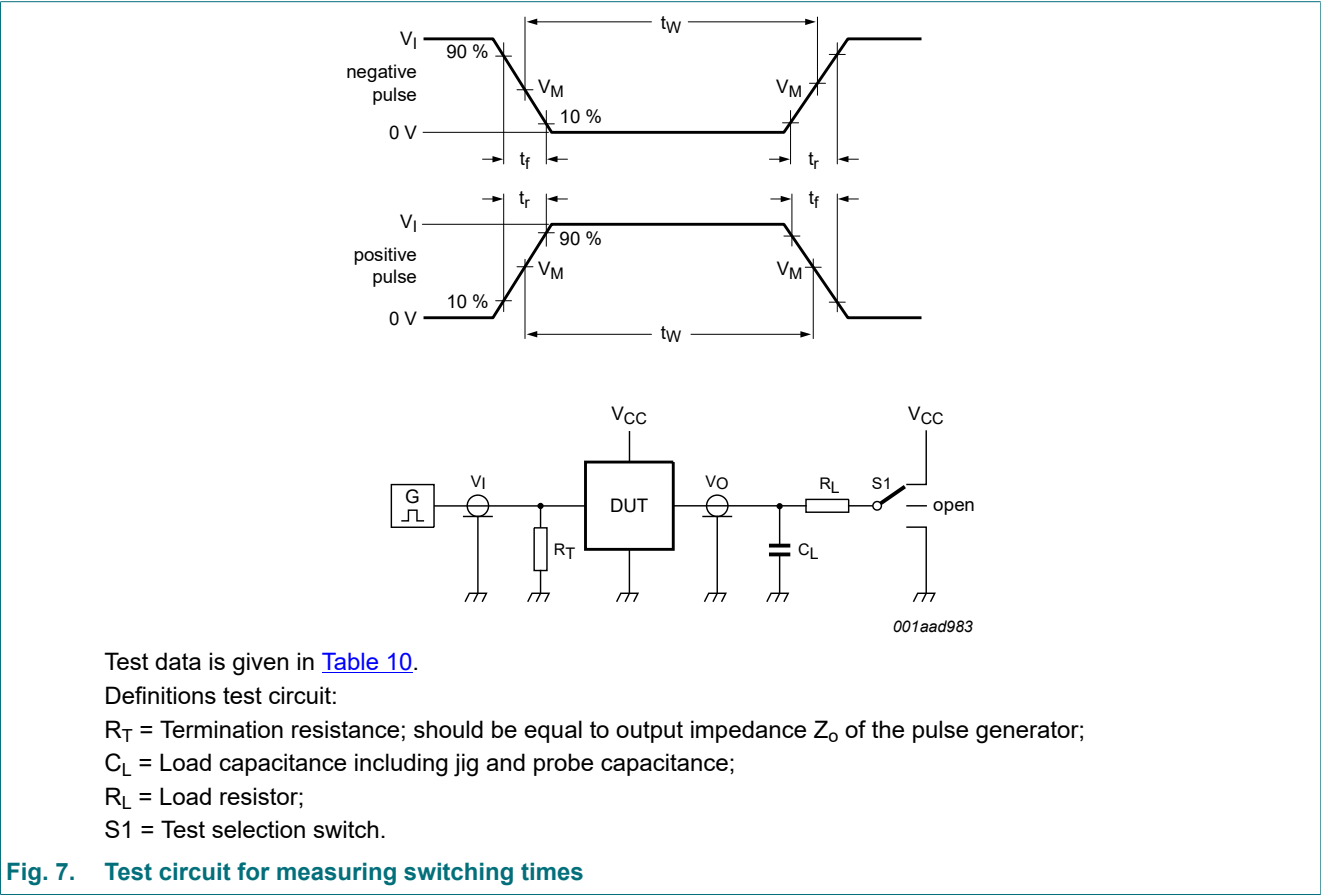
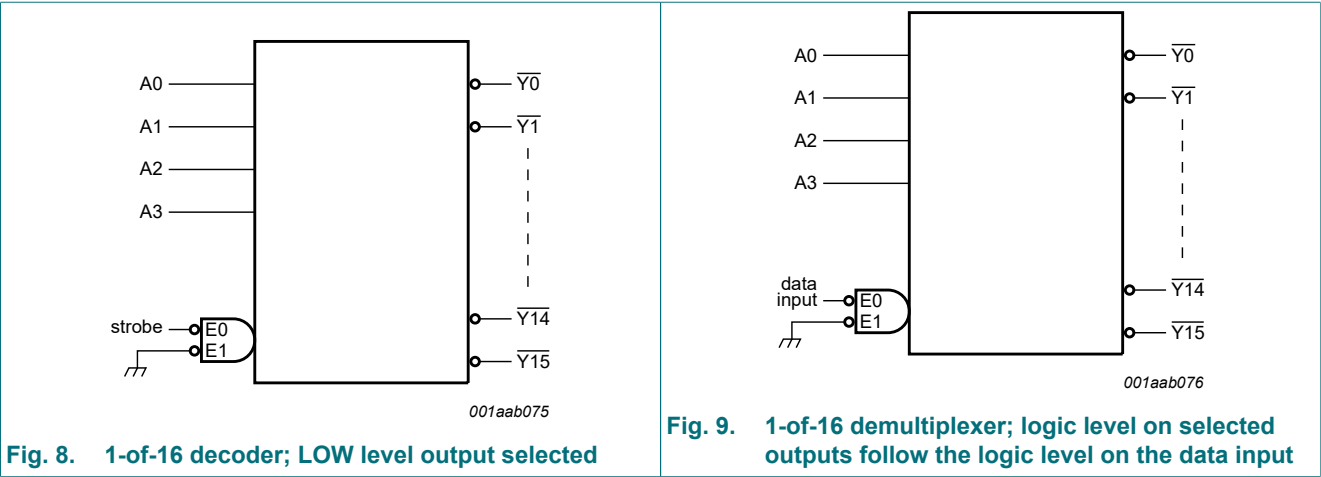


Table 10. Test data

Type	Input		Load		S1 position
	V _I	t _r , t _f	C _L	R _L	t _{pHL} , t _{pLH}
74HC154	V _{CC}	6 ns	15 pF, 50 pF	1 kΩ	open
74HCT154	3 V	6 ns	15 pF, 50 pF	1 kΩ	open

11. Application information



12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

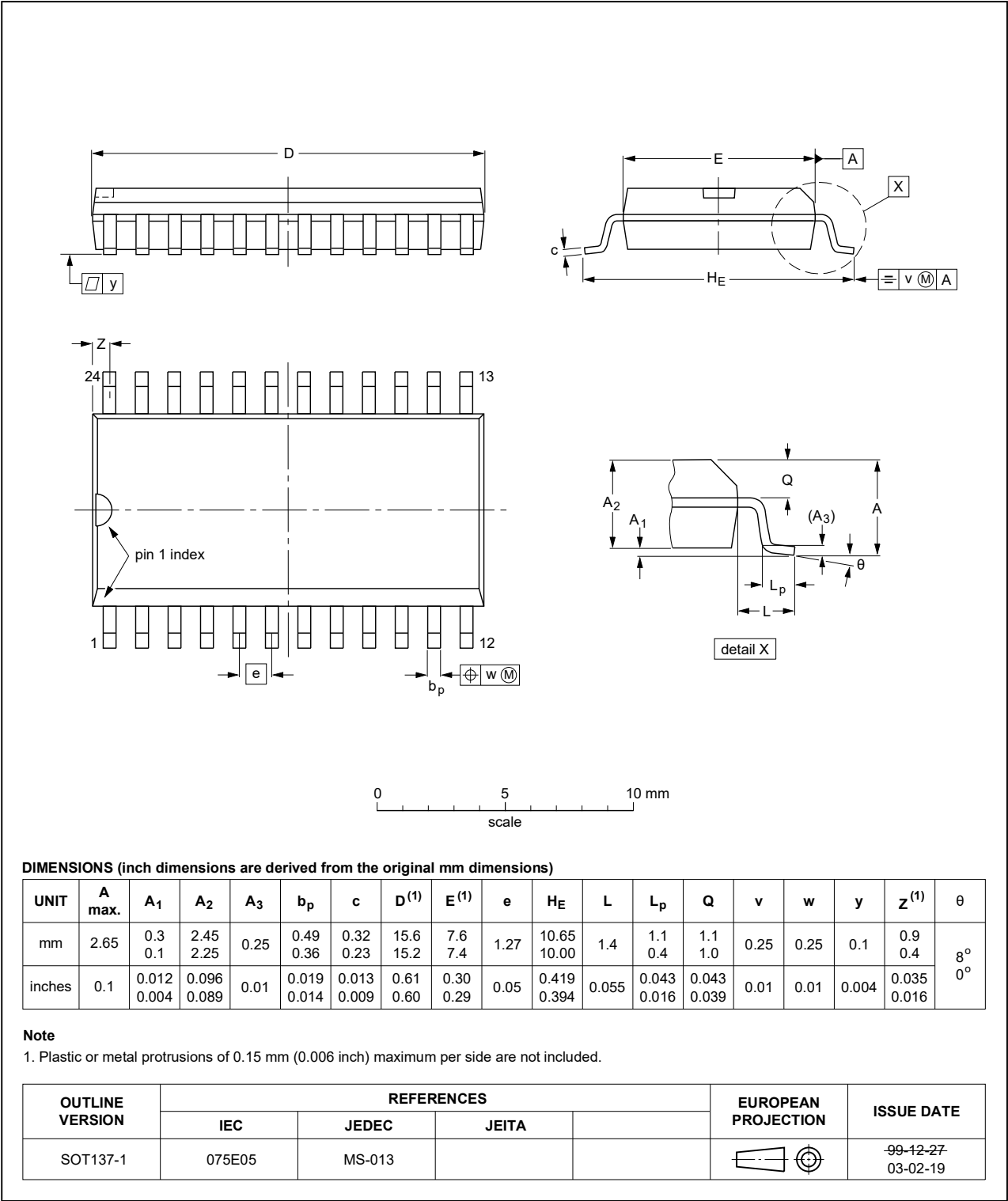


Fig. 10. Package outline SOT137-1 (SO24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

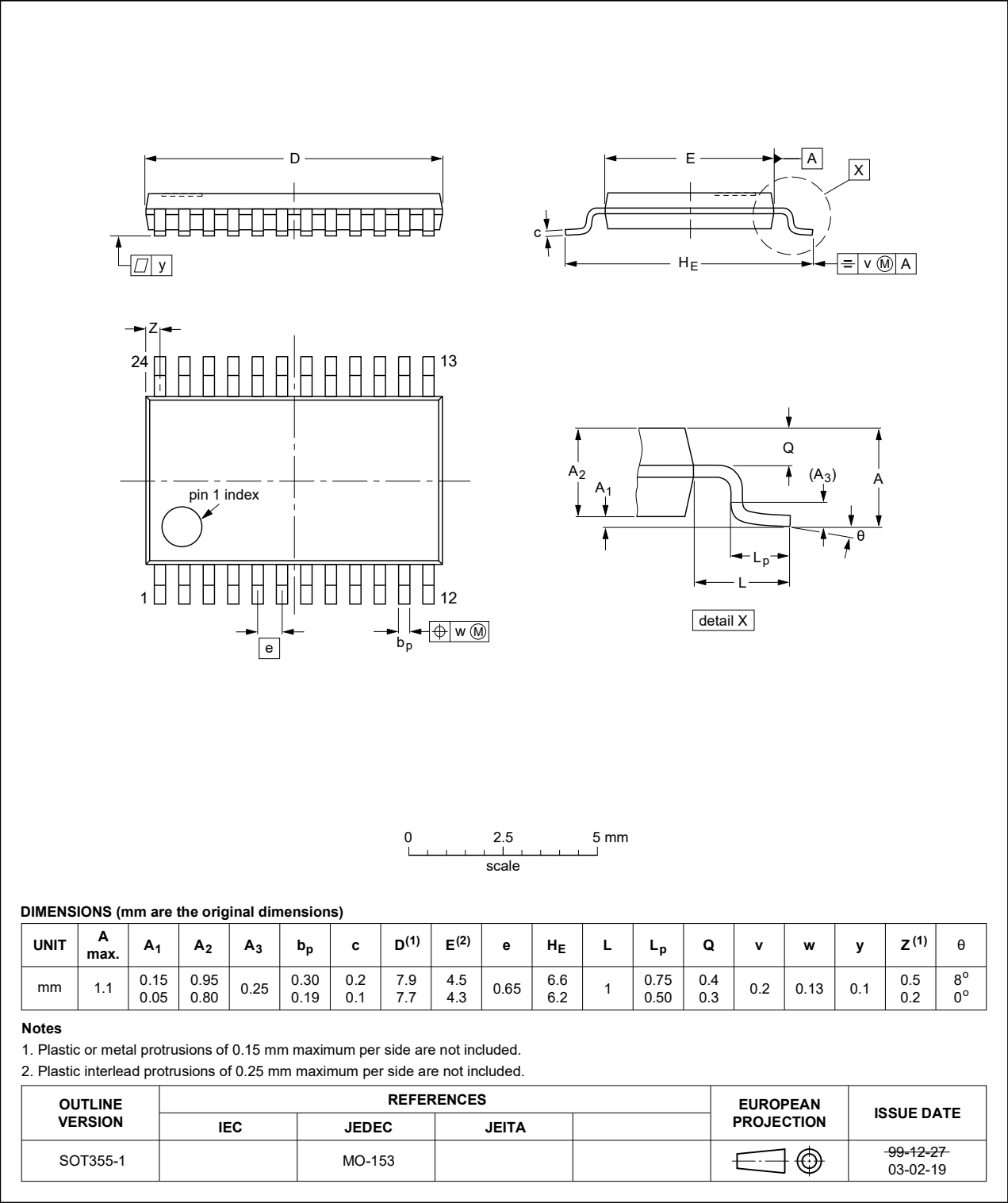


Fig. 11. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package;
no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1

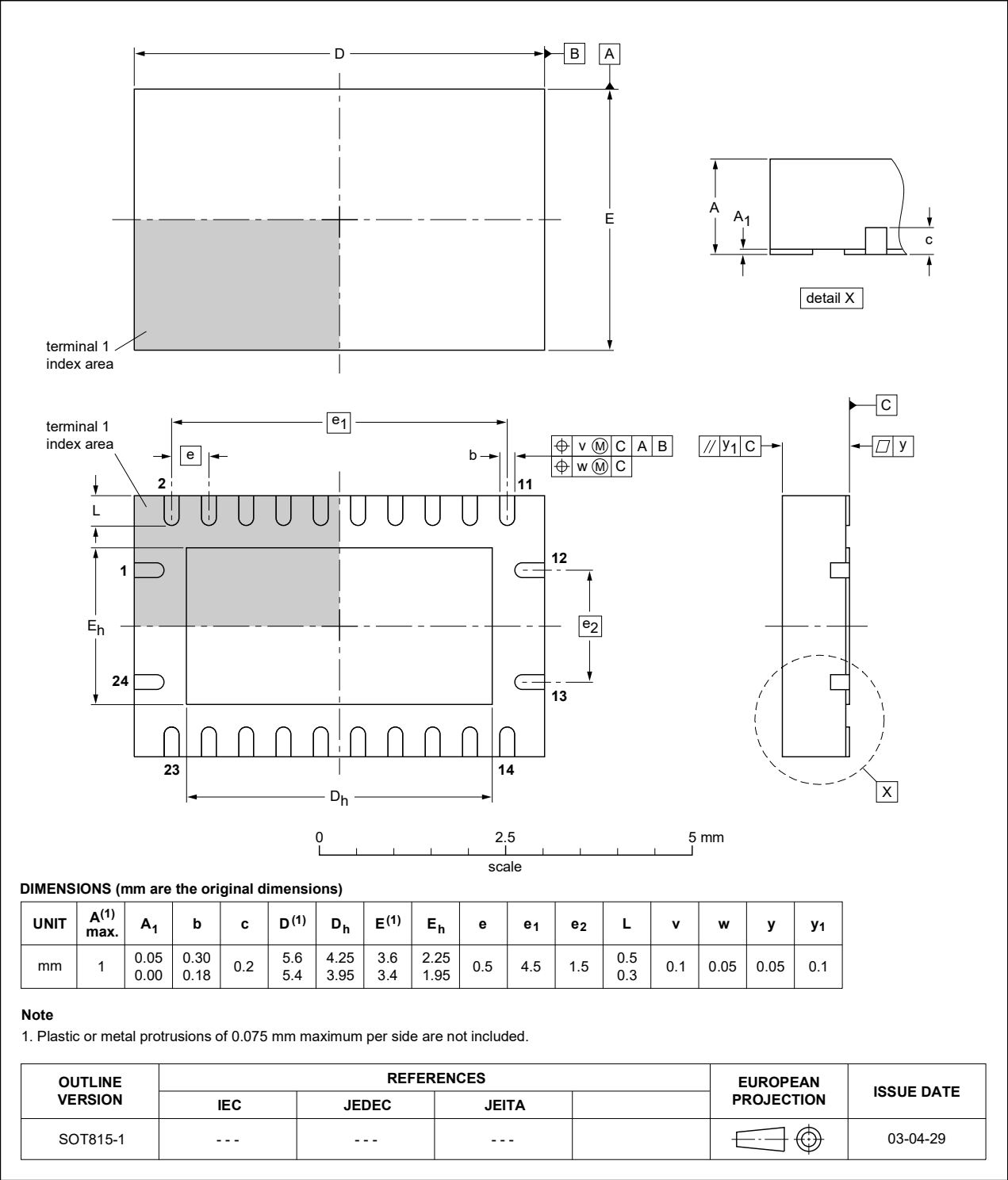


Fig. 12. Package outline SOT815-1 (DHVQFN24)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT154 v.10	20240805	Product data sheet	-	74HC_HCT154 v.9
Modifications:	Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT154 v.9	20210819	Product data sheet	-	74HC_HCT154 v.8
Modifications:	Section 2 updated. - Type number 74HC154DB (SOT340-1/SSOP24) removed.			
74HC_HCT154 v.8	20210511	Product data sheet	-	74HC_HCT154 v.7
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Type number 74HCT154DB (SOT340-1/SSOP24) removed. Section 5.1: overline corrected (errata). Section 7: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT154 v.7	20160229	Product data sheet	-	74HC_HCT154 v.6
Modifications:	Type numbers 74HC154N and 74HCT154N (SOT101-1) removed.			
74HC_HCT154 v.6	20070212	Product data sheet	-	74HC_HCT154 v.5
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. Table 3: Corrected errors in output information.			
74HC_HCT154 v.5	20041012	Product specification	-	74HC_HCT154 v.4
74HC_HCT154 v.4	20041005	Product specification	-	74HC_HCT154 v.3
74HC_HCT154 v.3	20040601	Product specification	-	74HC_HCT154_CNV v.2

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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