

SN74CBTS6800

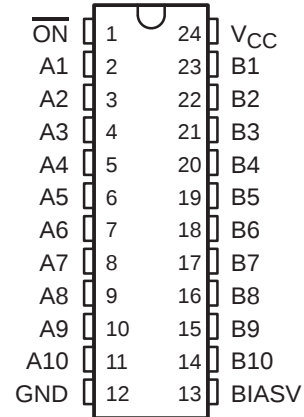
10-BIT FET BUS SWITCH

WITH PRECHARGED OUTPUTS AND SCHOTTKY DIODE CLAMPING

SCDS102C – JUNE 1999 – REVISED OCTOBER 2000

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion
- Schottky Diodes on the I/Os to Clamp Undershoots up to -2 V

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74CBTS6800 provides ten bits of high-speed TTL-compatible bus switching with Schottky diodes on the I/Os to clamp undershoots.

The low on-state resistance of the switch allows bidirectional connections to be made, while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The SN74CBTS6800 is organized as one 10-bit switch with a single enable ($\overline{ON}$) input. When $\overline{ON}$ is low, the switch is on, and port A is connected to port B. When $\overline{ON}$ is high, the switch between port A and port B is open. When $\overline{ON}$ is high or V_{CC} is 0 V, B port is precharged to BIASV through the equivalent of a 10-kΩ resistor.

ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – DW	Tube	SN74CBTS6800DW	CBTS6800
		Tape and reel	SN74CBTS6800DWR	
	SSOP – DB	Tape and reel	SN74CBTS6800DBR	CS6800
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBTS6800DBQR	CBTS6800
	TSSOP – PW	Tape and reel	SN74CBTS6800PWR	CS6800
	TVSOP – DGV	Tape and reel	SN74CBTS6800DGVR	CS6800

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

$\overline{ON}$	B1–B10	FUNCTION
L	A1–A10	Connect
H	BIASV	Precharge



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**TEXAS
INSTRUMENTS**

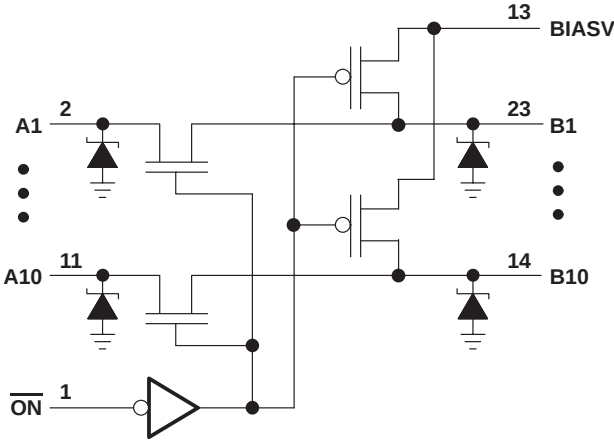
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Bias voltage range, BIASV	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	63°C/W
DBQ package	61°C/W
DGV package	86°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4	5.5	V
BIASV Supply voltage	1.3	V_{CC}	V
V_{IH} High-level control input voltage	2		V
V_{IL} Low-level control input voltage		0.8	V
T_A Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V _{IK}	A or B inputs	V _{CC} = 4.5 V, I _I = –18 mA				–0.7	V
	Control inputs					–1.2	
I _{IL}		V _{CC} = 5.5 V, V _I = GND				–5	μA
I _{IH}		V _{CC} = 5.5 V, V _I = 5.5 V				150	μA
I _O		V _{CC} = 4.5 V, BIASV = 2.4 V, V _O = 0		0.25			mA
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND				3	μA
ΔI _{CC} [‡]	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND				2.5	mA
C _i	Control inputs	V _I = 3 V or 0			3.5		pF
C _{io(OFF)}		V _O = 3 V or 0, $\overline{\text{ON}} = V_{CC}$			4.5		pF
r _{on} [§]		V _{CC} = 4 V, TYP at V _{CC} = 4 V	V _I = 2.4 V, I _I = 15 mA		11	20	Ω
		V _{CC} = 4.5 V	V _I = 0, I _I = 64 mA		3	7	
			I _I = 30 mA		3	7	
			V _I = 2.4 V, I _I = 15 mA		6	15	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t _{pd} [¶]	A or B	B or A			0.35		0.25	ns
t _{PZH}	$\overline{\text{ON}}$	A or B	BIASV = GND		6	2	5.1	ns
t _{PZL}			BIASV = 3 V		6	2	5.6	
t _{PHZ}	$\overline{\text{ON}}$	A or B	BIASV = GND		5.5	1	5	ns
t _{PLZ}			BIASV = 3 V		5.5	2	5.9	

[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

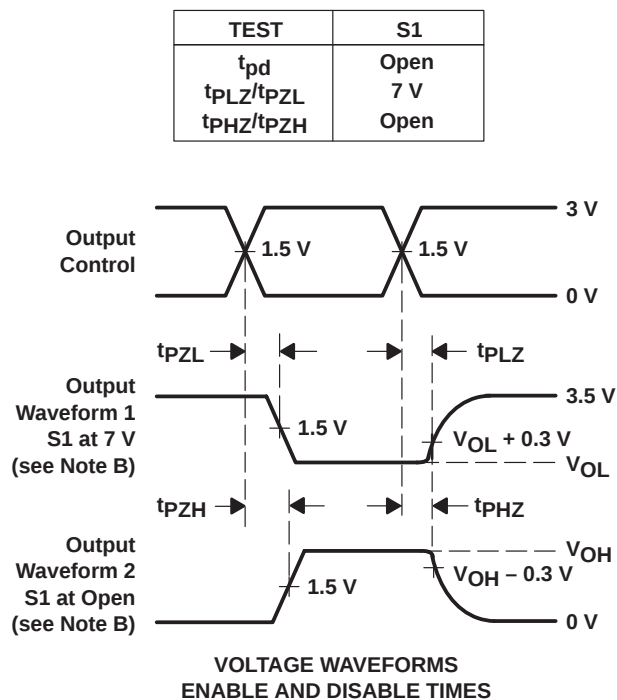
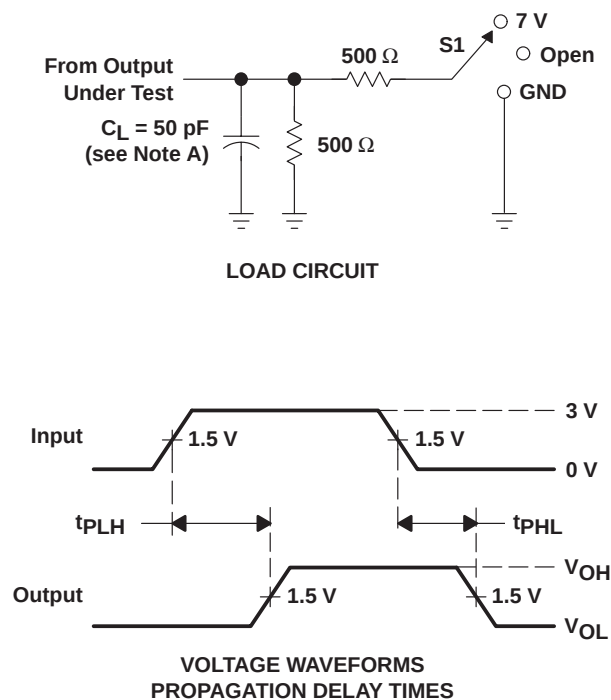
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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CBTS6800DGVR	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CS6800
SN74CBTS6800DGVR.A	Active	Production	TVSOP (DGV) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CS6800
SN74CBTS6800PWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CS6800
SN74CBTS6800PWR.A	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CS6800

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTS6800PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

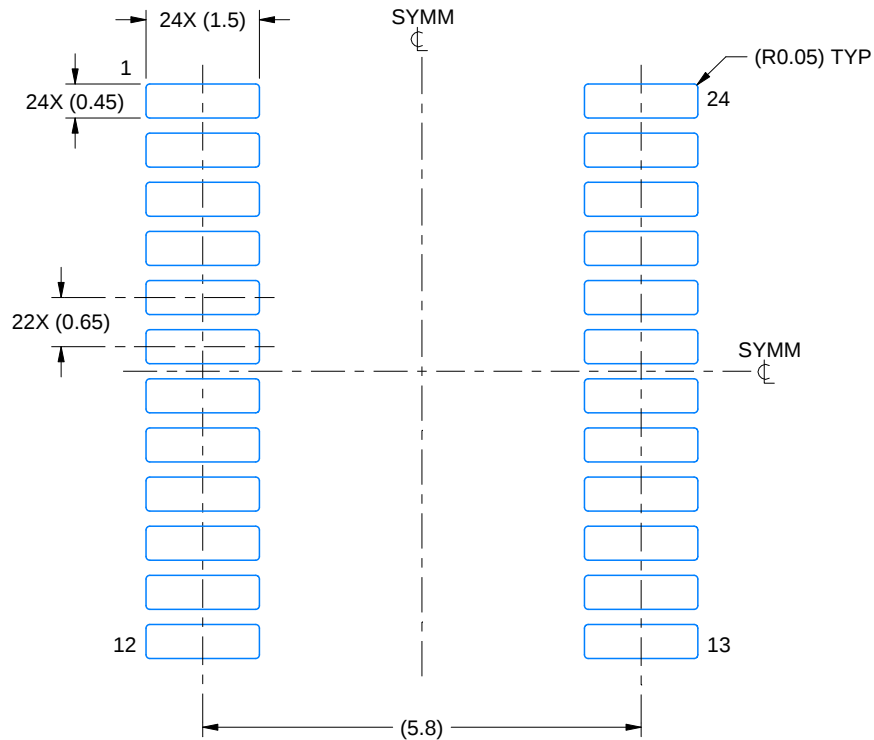
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTS6800PWR	TSSOP	PW	24	2000	353.0	353.0	32.0

EXAMPLE BOARD LAYOUT

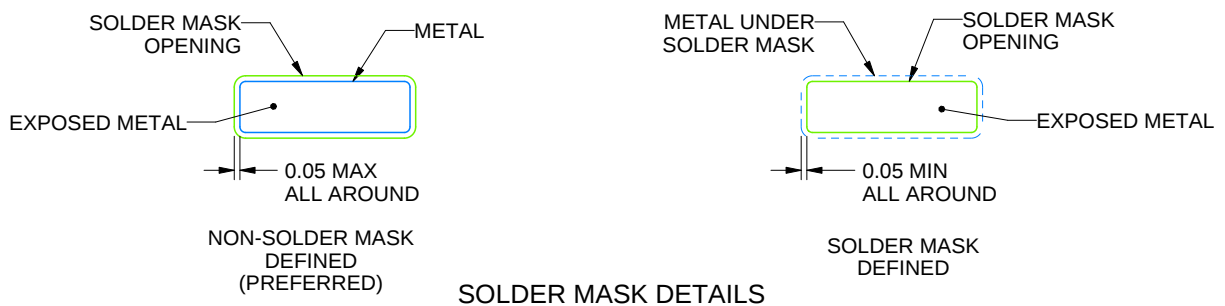
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220208/A 02/2017

NOTES: (continued)

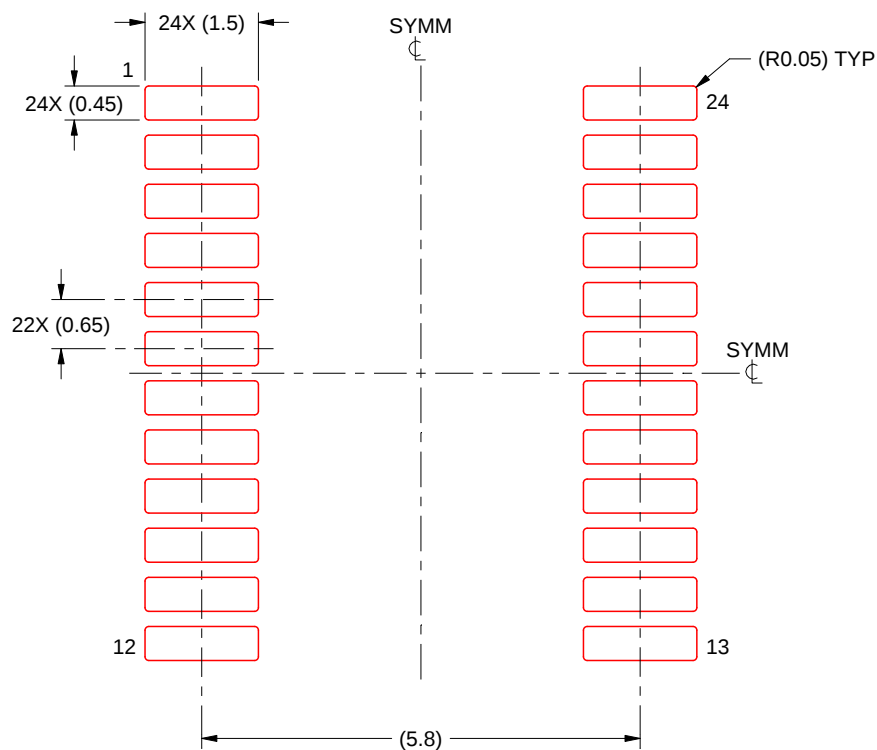
6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

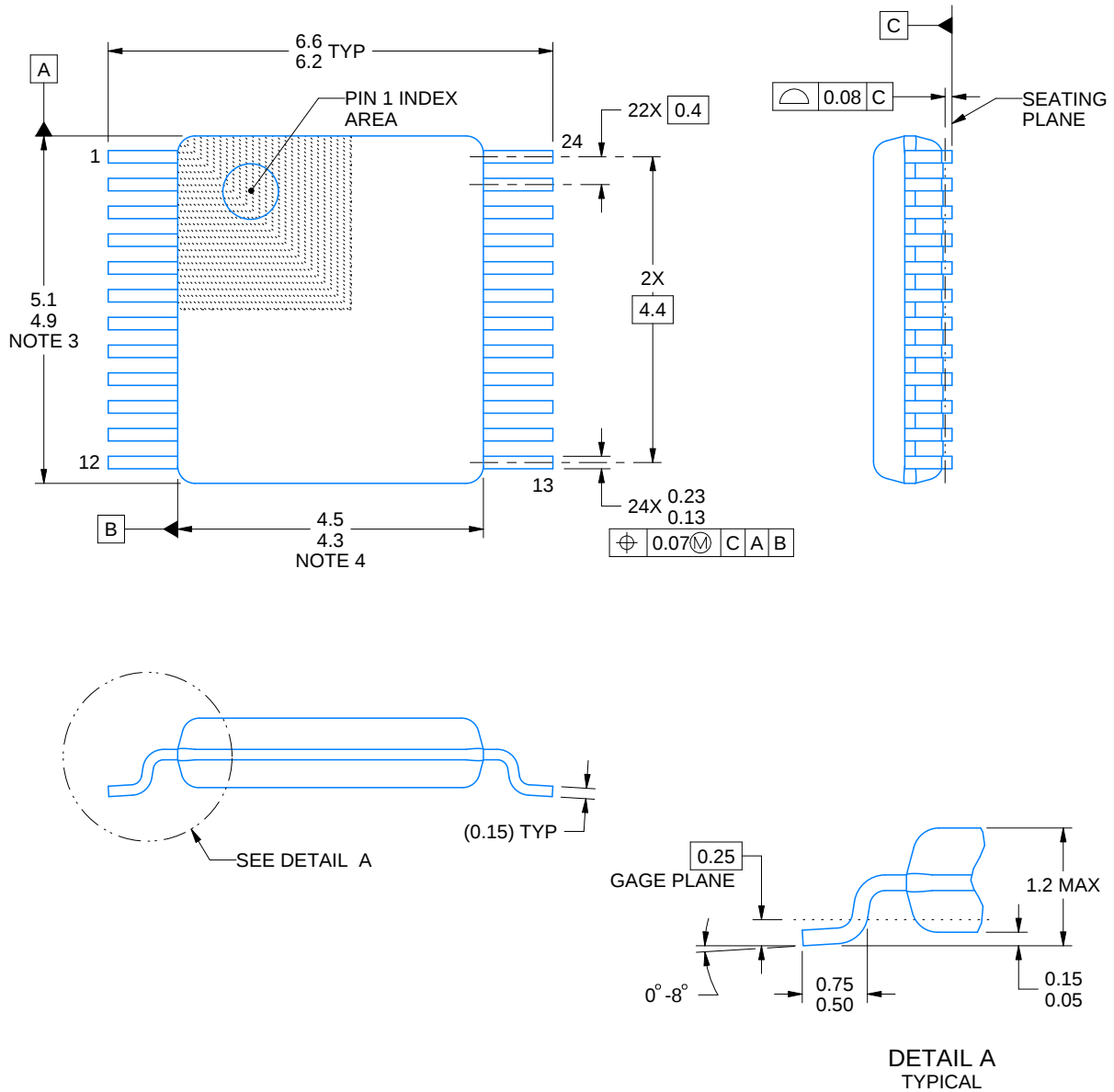
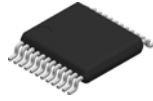


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4229221/A 12/2022

NOTES:

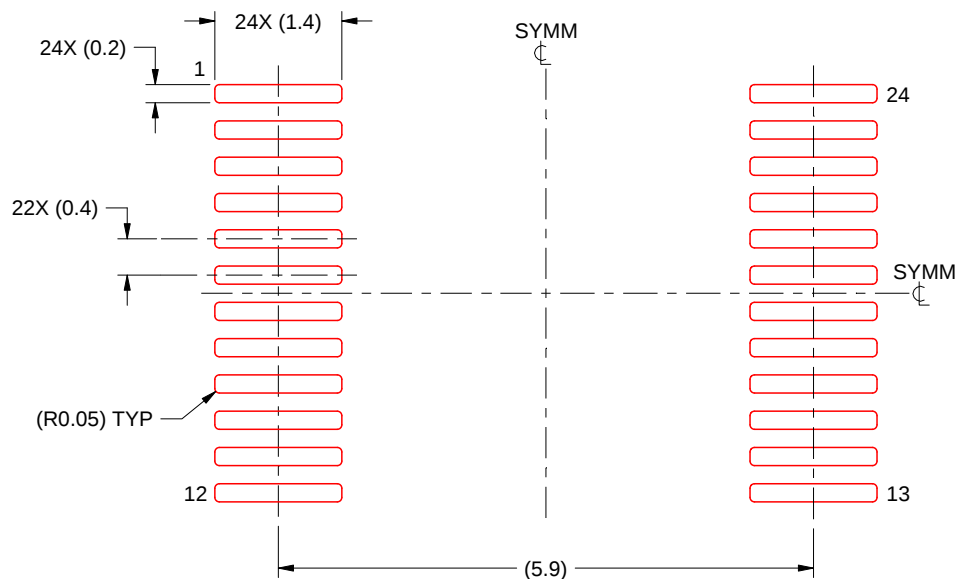
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE STENCIL DESIGN

DGV0024A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

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NOTES: (continued)

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9. Board assembly site may have different recommendations for stencil design.

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