

74VHC132

Quad 2-Input NAND Schmitt Trigger

Features

- High Speed: $t_{PD} = 3.9\text{ns}$ (Typ.) at $V_{CC} = 5\text{V}$
- Power down protection is provided on all inputs
- Low power dissipation: $I_{CC} = 2\mu\text{A}$ (Max.) at $T_A = 25^\circ\text{C}$
- Low noise: $V_{OLP} = 0.8\text{V}$ (Max.)
- Pin and function compatible with 74HC132

General Description

The VHC132 is an advanced high speed CMOS 2-input NAND Schmitt Trigger Gate fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to Bipolar Schottky TTL while maintaining the CMOS low power dissipation. Pin configuration and function are the same as the VHC00 but the inputs have hysteresis between the positive-going and negative-going input thresholds, which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Thus greater noise margin than conventional gates is provided. An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Ordering Information

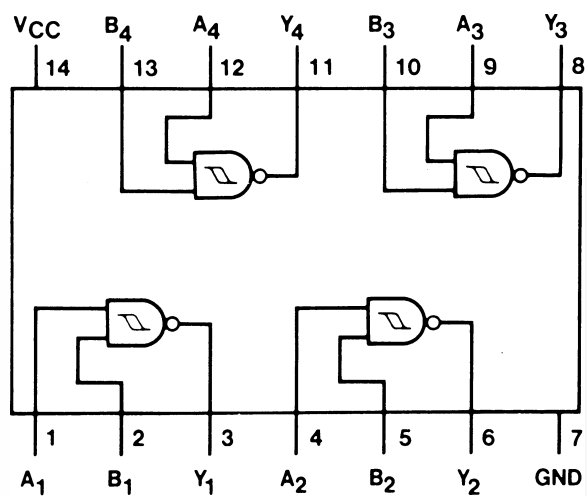
Order Number	Package Number	Package Description
74VHC132M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC132SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC132MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



All packages are lead free per JEDEC: J-STD-020B standard.

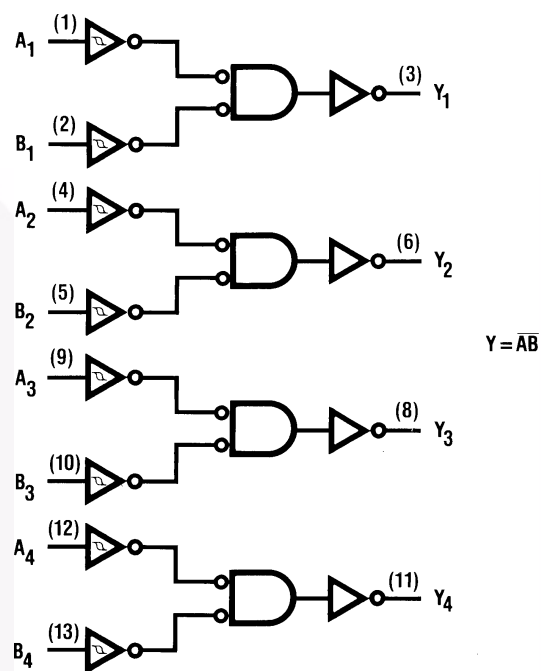
Connection Diagram



Pin Description

Pin Names	Description
A_n, B_n	Inputs
Y_n	Outputs

Logic Diagram



Truth Table

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	−0.5V to +7.0V
V_{IN}	DC Input Voltage	−0.5V to +7.0V
V_{OUT}	DC Output Voltage	−0.5V to $V_{CC} + 0.5V$
I_{IK}	Input Diode Current	−20mA
I_{OK}	Output Diode Current	±20mA
I_{OUT}	DC Output Current	±25mA
I_{CC}	DC V_{CC} / GND Current	±50mA
T_{STG}	Storage Temperature	−65°C to +150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions⁽¹⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to +5.5V
V_{IN}	Input Voltage	0V to +5.5V
V_{OUT}	Output Voltage	0V to V_{CC}
T_{OPR}	Operating Temperature	−40°C to +85°C

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units
				Min.	Typ.	Max.	Min.	Max.	
V_P	Positive Threshold Voltage	3.0				2.20		2.20	V
		4.5				3.15		3.15	
		5.5				3.85		3.85	
V_N	Negative Threshold Voltage	3.0		0.90			0.90		V
		4.5		1.35			1.35		
		5.5		1.65			1.65		
V_H	Hysteresis Output Voltage	3.0		0.30		1.20	0.30	1.20	V
		4.5		0.40		1.40	0.40	1.40	
		5.5		0.50		1.60	0.50	1.60	
V_{OH}	HIGH Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu\text{A}$	1.9	2.0		1.9	V
		3.0			2.9	3.0		2.9	
		4.5			4.4	4.5		4.4	
		3.0		$I_{OH} = -4\text{mA}$	2.58			2.48	
		4.5		$I_{OH} = -8\text{mA}$	3.94			3.80	
V_{OL}	LOW Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\mu\text{A}$		0.0	0.1	0.1	V
		3.0				0.0	0.1	0.1	
		4.5				0.0	0.1	0.1	
		3.0		$I_{OL} = 4\text{mA}$			0.36	0.44	
		4.5		$I_{OL} = 8\text{mA}$			0.36	0.44	
I_{IN}	Input Leakage Current	0–5.5	$V_{IN} = 5.5\text{V or GND}$				± 0.1	± 1.0	μA
I_{CC}	Quiescent Supply Current	5.5	$V_{IN} = V_{CC} \text{ or GND}$				2.0	20.0	μA

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25^\circ\text{C}$		Units
				Typ.	Limits	
$V_{OLP}^{(2)}$	Quiet Output Maximum Dynamic V_{OL}	5.0	$C_L = 50\text{pF}$	0.3	0.8	V
$V_{OLV}^{(2)}$	Quiet Output Maximum Dynamic V_{OL}	5.0	$C_L = 50\text{pF}$	–0.3	–0.8	V
$V_{IHD}^{(2)}$	Maximum HIGH Level Dynamic Input Voltage	5.0	$C_L = 50\text{pF}$		3.5	V
$V_{ILD}^{(2)}$	Maximum LOW Level Dynamic Input Voltage	5.0	$C_L = 50\text{pF}$		1.5	V

Note:

2. Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C			T _A = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
t _{PHL} , t _{PLH}	Propagation Delay	3.3 ± 0.3	C _L = 15pF		6.1	11.9	1.0	14.0	ns
			C _L = 50pF		8.0	15.4	1.0	17.5	
		5.0 ± 0.5	C _L = 15pF		3.9	7.7	1.0	9.0	
			C _L = 50pF		5.9	9.7	1.0	11.0	
C _{IN}	Input Capacitance		V _{CC} = Open		4	10		10	pF
C _{PD}	Power Dissipation Capacitance		⁽³⁾		16				pF

Note:

3. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation:

$$I_{CC} (\text{Opr.}) = C_{PD} \cdot V_{CC} \cdot I_{IN} + I_{CC} / 4 \text{ (per gate)}$$

Physical Dimensions

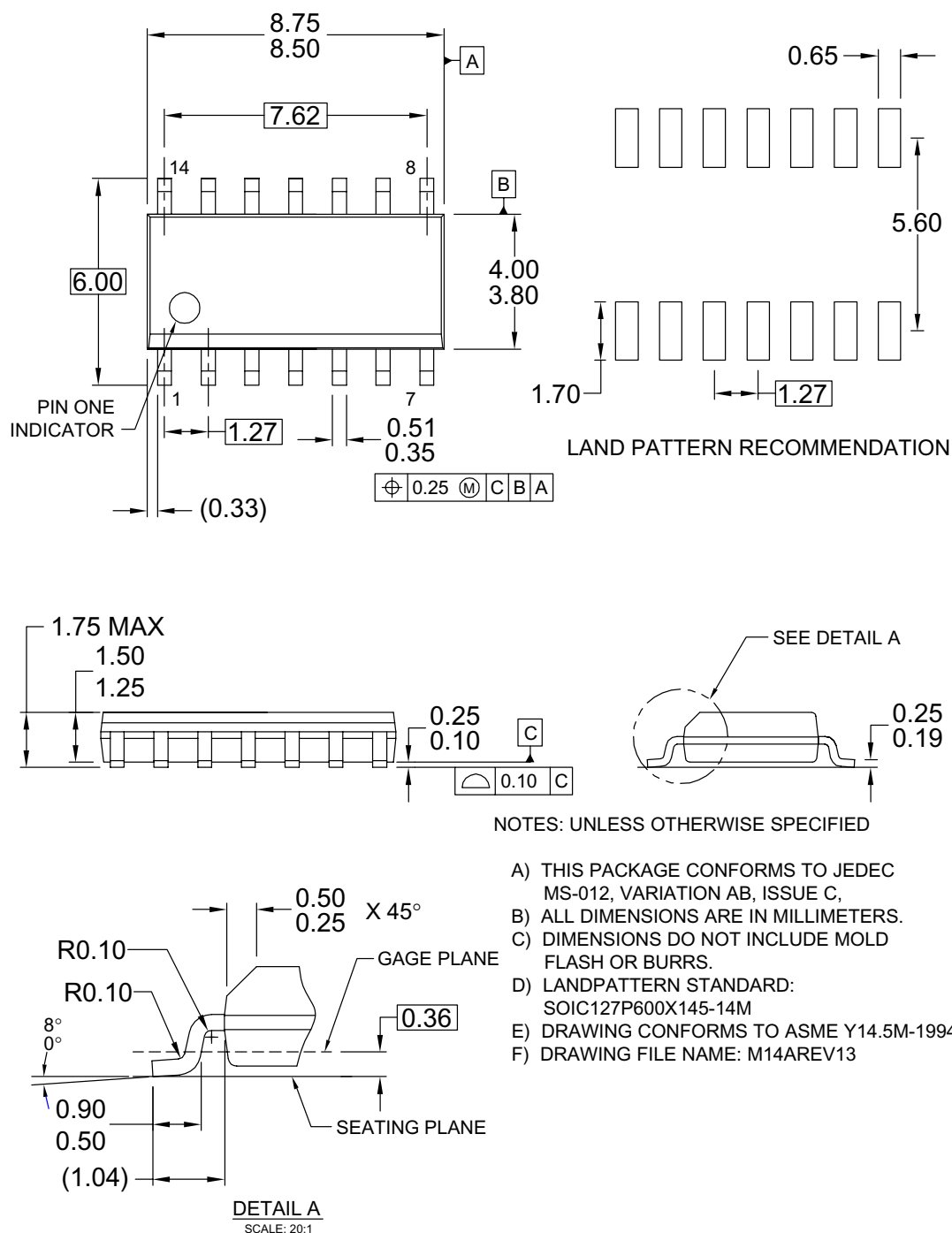


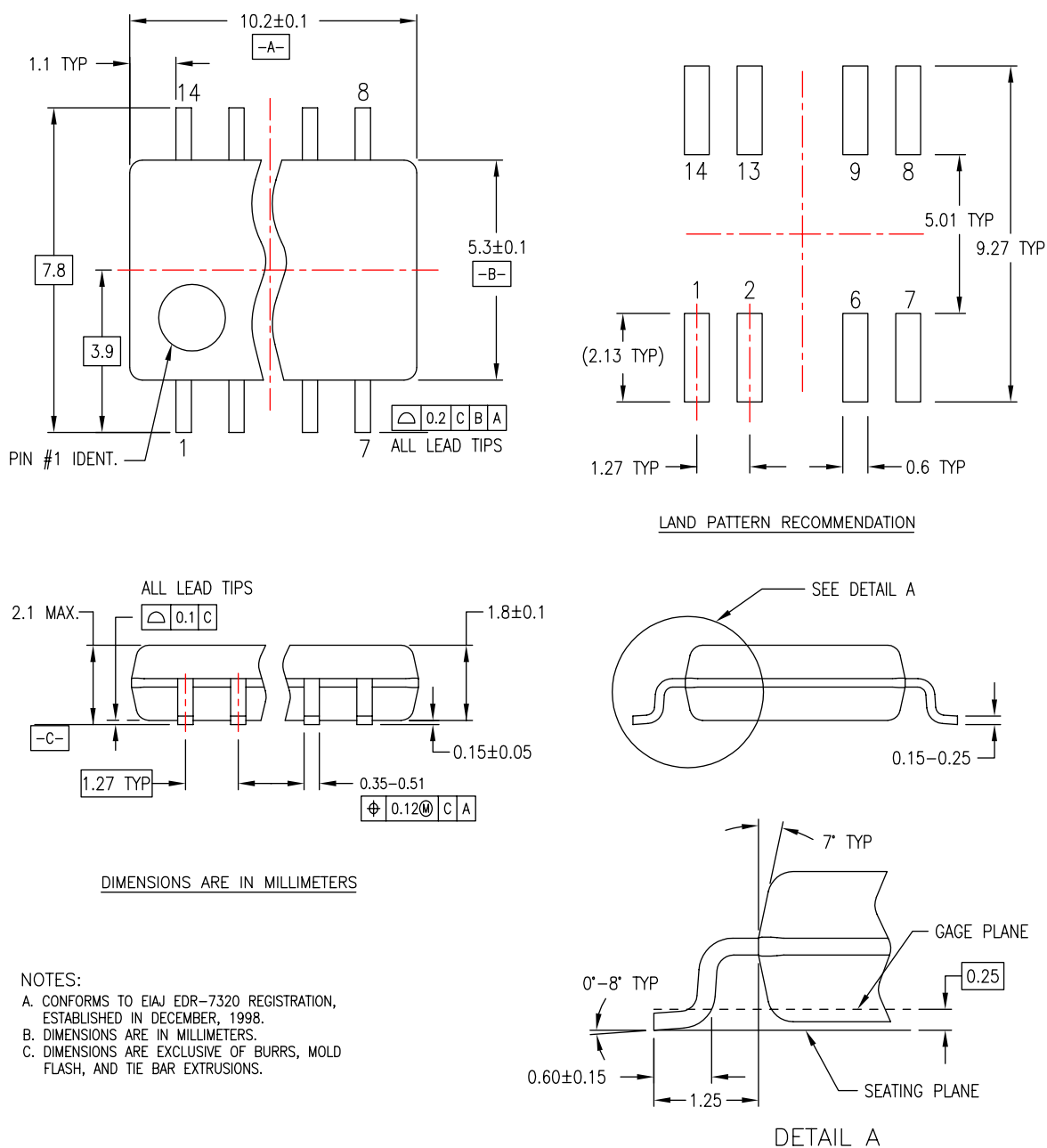
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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Physical Dimensions (Continued)



M14DREVC

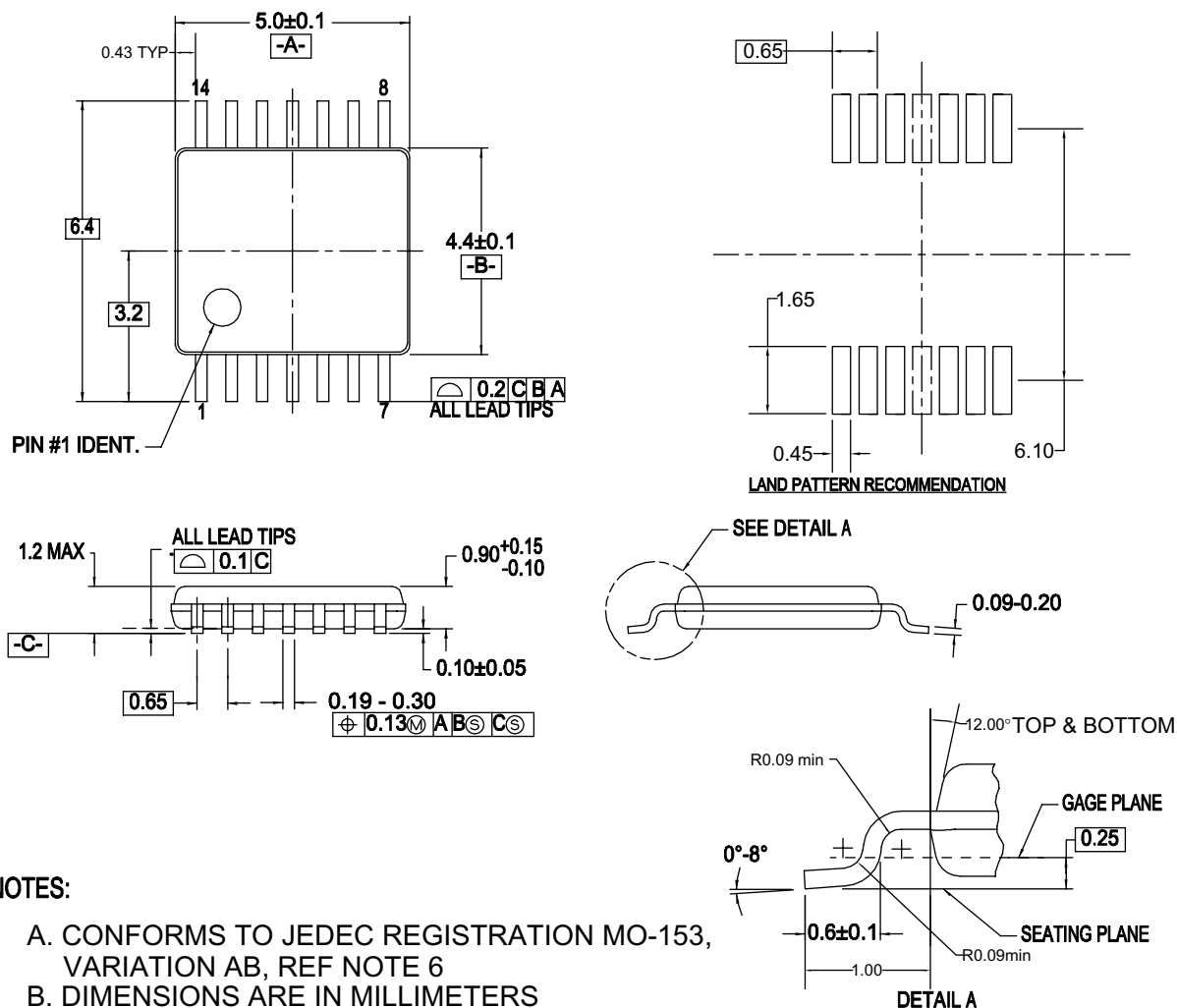
Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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