

74HC4050

Hex non-inverting HIGH-to-LOW level shifter

Rev. 6 — 12 March 2023

Product data sheet

1. General description

The 74HC4050 is a hex buffer with over-voltage tolerant inputs. Inputs are overvoltage tolerant to 15 V which enables the device to be used in HIGH-to-LOW level shifting applications.

2. Features and benefits

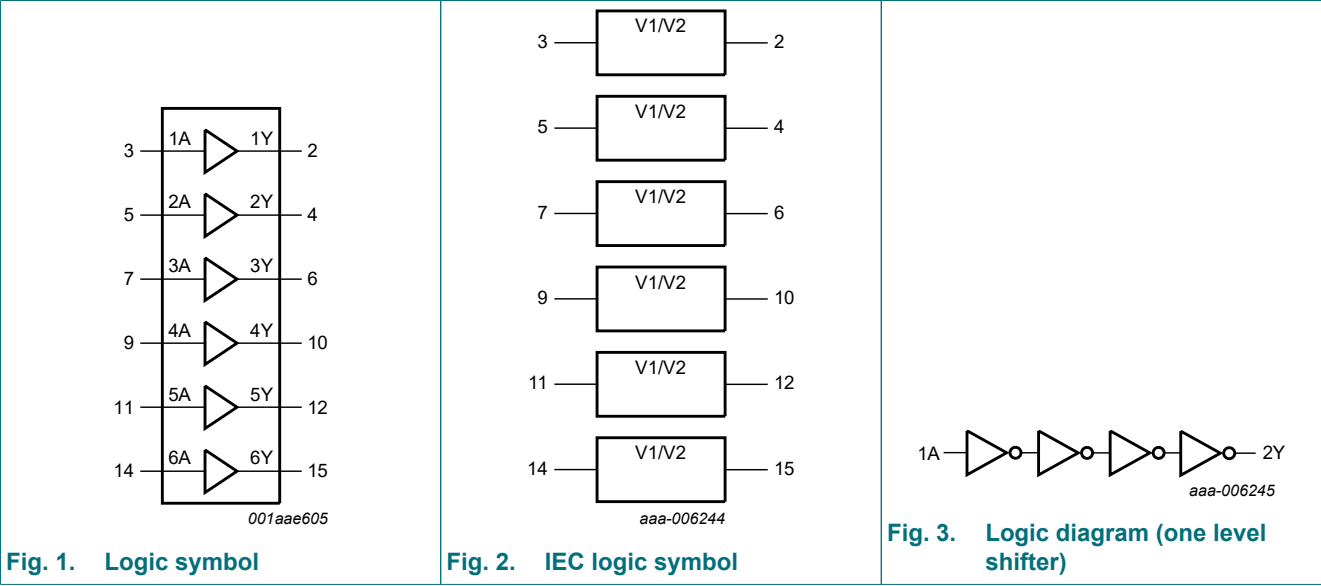
- Wide supply voltage range from 2.0 to 6.0 V
- Overvoltage tolerant inputs to 15 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

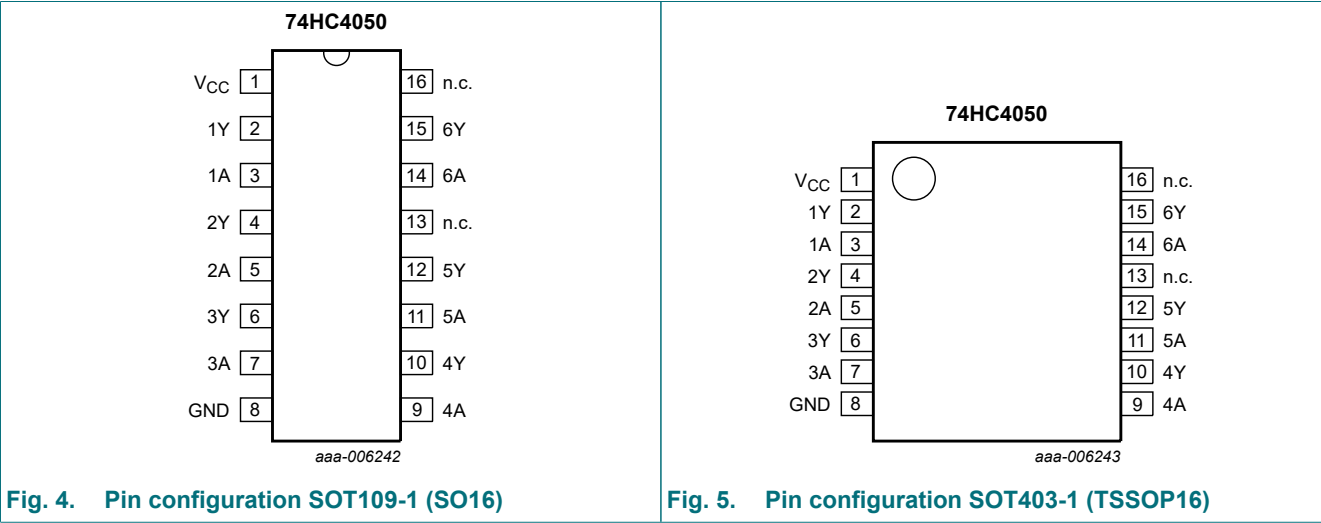
Type number	Package			
	Temperature range	Name	Description	Version
74HC4050D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4050PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
V _{CC}	1	supply voltage
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 10, 12, 15	output
1A, 2A, 3A, 4A, 5A, 6A	3, 5, 7, 9, 11, 14	input
GND	8	ground (0 V)
n.c.	13, 16	not connected

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Output
nA	nY
L	L
H	H

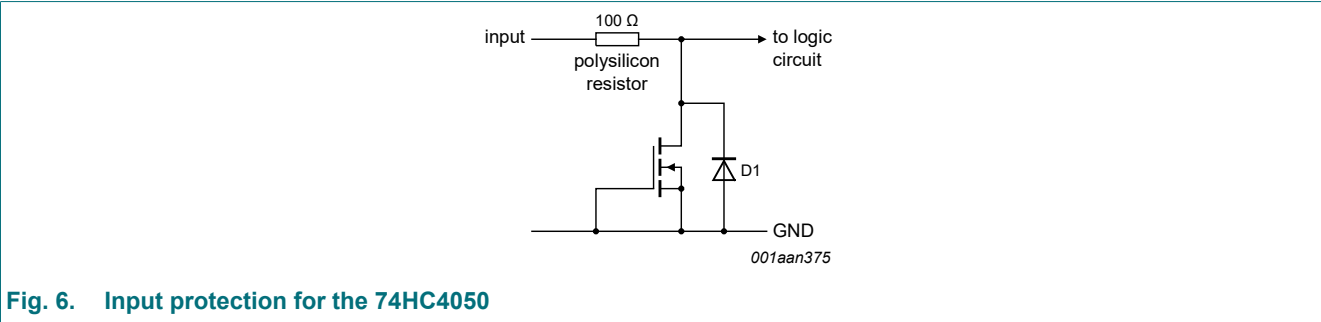
7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
V _{IK}	input clamping voltage		-0.5	+16	V
I _{IK}	input clamping current	V _I < -0.5 V	-20	-	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	-	±25	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-	-50	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[1]	-	500	mW

[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.



8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.0	5.0	6.0	V
V _I	input voltage		0	-	15	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}; V_I = 2.0\text{ V}$	-	-	625	ns/V
		$V_{CC} = 4.5\text{ V}; V_I = 4.5\text{ V}$	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}; V_I = 6.0\text{ V}$	-	-	83	ns/V
		$V_{CC} = 6.0\text{ V}; V_I = 10.0\text{ V}$	-	-	81	ns/V
		$V_{CC} = 6.0\text{ V}; V_I = 15.0\text{ V}$	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.3	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.1	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.7	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	1.8	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.3	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$								
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	3.98	-	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$I_O = -5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	5.48	-	-	5.34	-	5.2	-	V
		$V_I = V_{IH}\text{ or }V_{IL}$								
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	-	-	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	-	-	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	-	-	0.1	-	0.1	-	0.1	V
I_I	input leakage current	$I_O = 4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	-	-	0.26	-	0.33	-	0.4	V
		$I_O = 5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	-	-	0.26	-	0.33	-	0.4	V
		$V_I = V_{CC}\text{ or GND}; V_{CC} = 6.0\text{ V}$	-	-	± 0.1	-	± 1.0	-	± 1.0	μA
		$V_I = 15\text{ V}; V_{CC} = 2.0\text{ V to }6.0\text{ V}$	-	-	± 0.5	-	± 5.0	-	± 5.0	μA
I_{CC}	supply current	$V_I = 15\text{ V or GND}; I_O = 0\text{ A}; V_{CC} = 6.0\text{ V}$	-	-	2.0	-	20	-	40	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

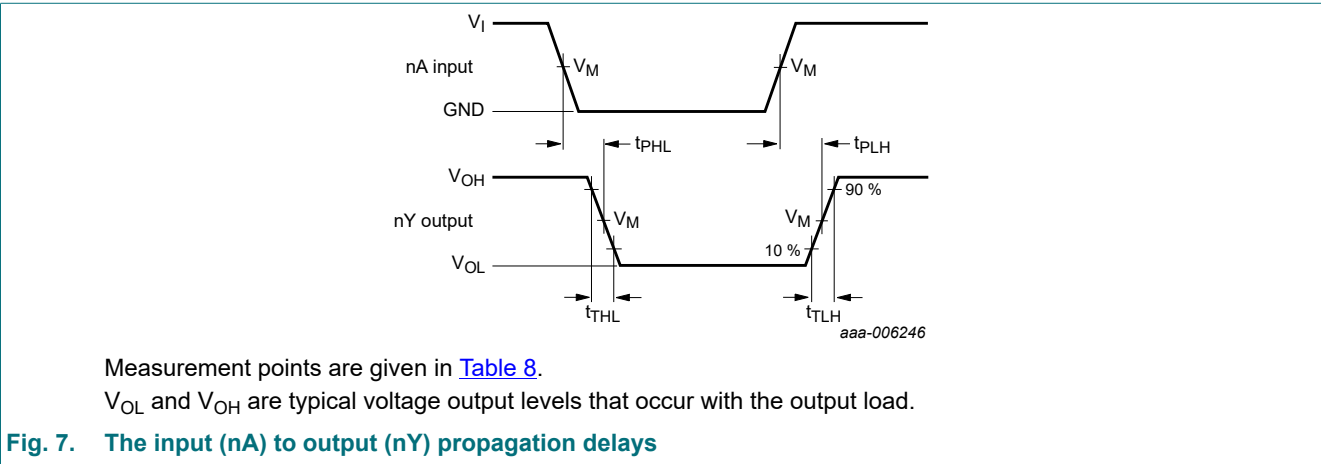
10. Dynamic characteristics

Table 7. Dynamic characteristics
 Voltages are referenced to GND (ground = 0 V); $C_L = 50\text{ pF}$ unless otherwise specified; for test circuit see Fig. 8.

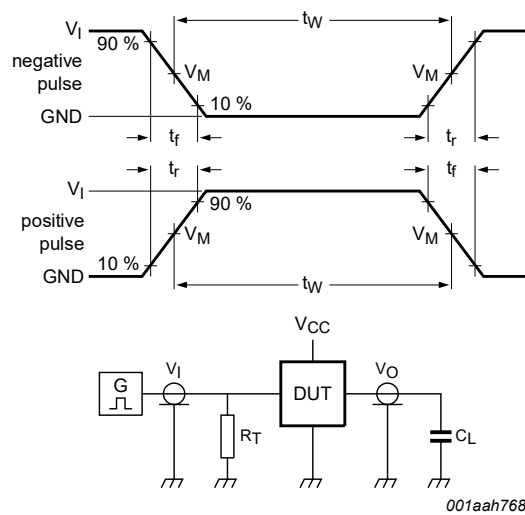
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Fig. 7 [1]								
		$V_{CC} = 2.0\text{ V}$	-	25	85	-	105	-	130	ns
		$V_{CC} = 4.5\text{ V}$	-	9	17	-	21	-	26	ns
		$V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$	-	7	-	-	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	-	7	14	-	18	-	22	ns
t_t	transition time	Yn; see Fig. 7 [2]								
		$V_{CC} = 2.0\text{ V}$	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5\text{ V}$	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0\text{ V}$	-	6	13	-	16	-	19	ns
C_{PD}	power dissipation capacitance	$C_L = 50\text{ pF}; f = 1\text{ MHz}; V_I = \text{GND to } V_{CC}$ [3]	-	14	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [2] t_t is the same as t_{THL} and t_{TLH} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



Input	Output
V_M	V_M
$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in [Table 9](#).
Definitions test circuit:
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 C_L = Load capacitance including jig and probe capacitance.
 R_L = Load resistance.
 $S1$ = Test selection switch.

Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Input		Load	Test
V_I	t_r, t_f	C_L	
V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1

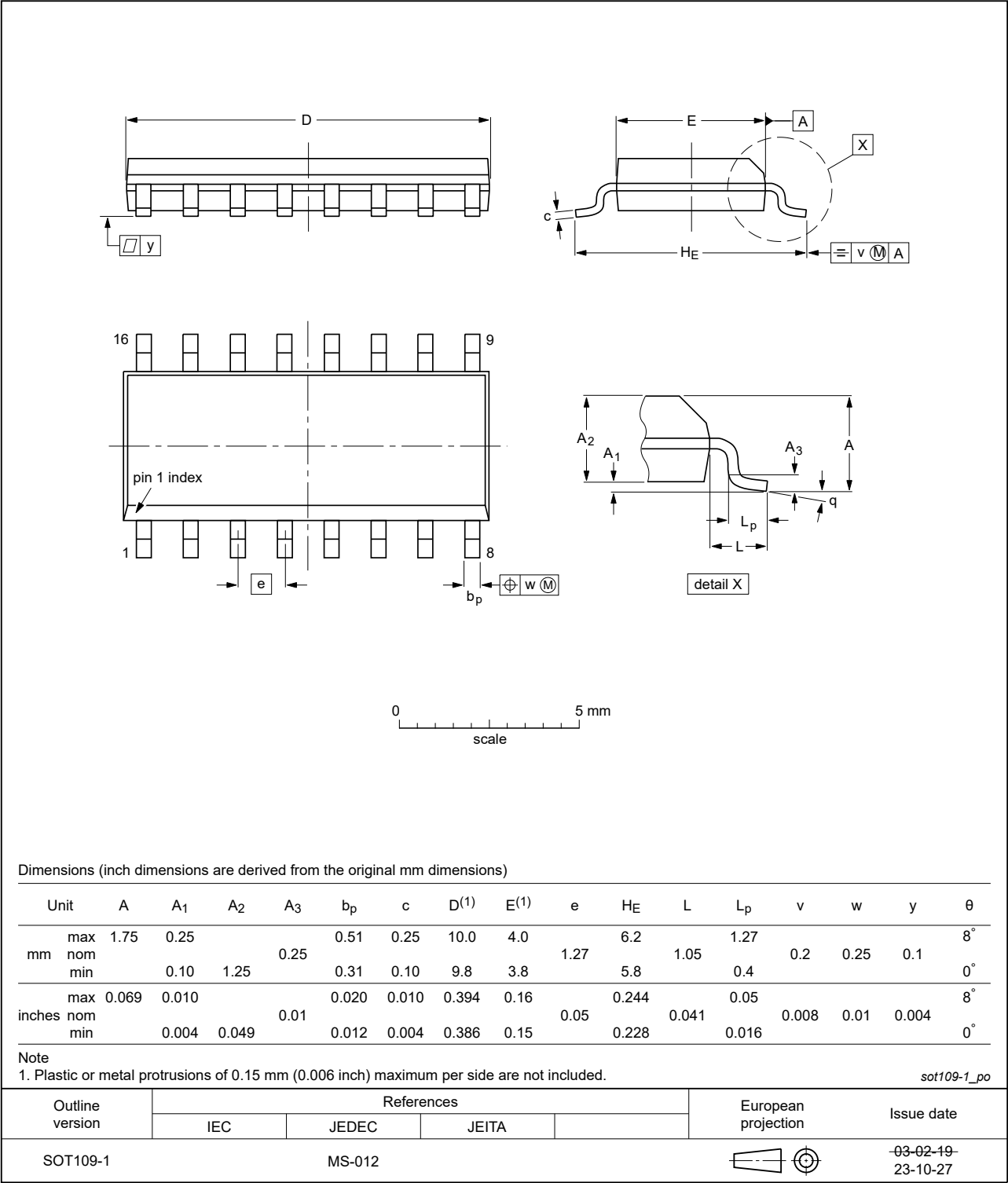


Fig. 9. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

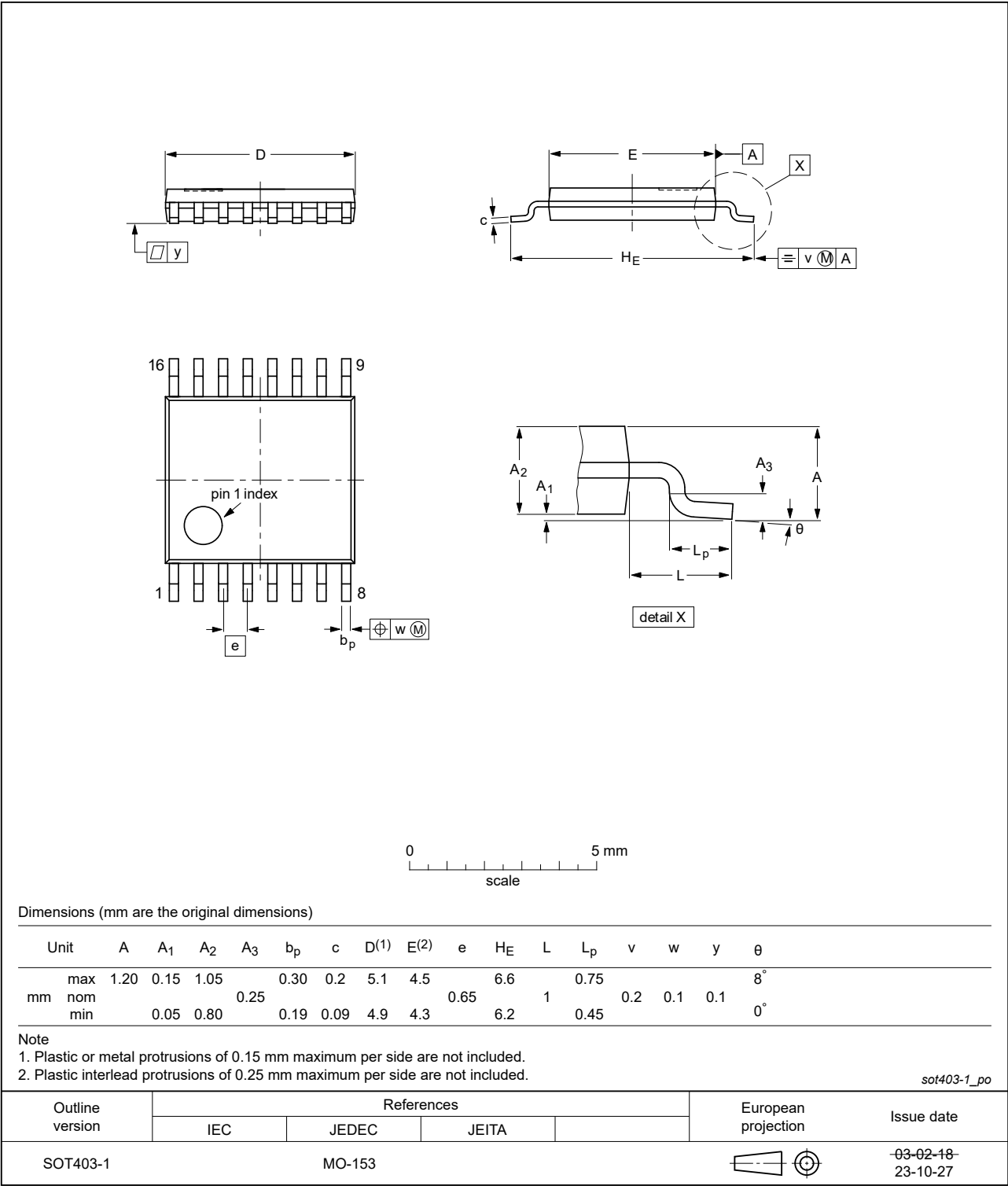


Fig. 10. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC4050 v.6	20240312	Product data sheet	-	74HC4050 v.5
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 9 and Fig. 10: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74HC4050 v.5	20210803	Product data sheet	-	74HC4050 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74HC4050DB (SOT339-1/SSOP20) removed. • Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation updated.			
74HC4050 v.4	20160205	Product data sheet	-	74HC4050 v.3
Modifications:	• Type number 74HC4050N (SOT38-4) removed.			
74HC4050 v.3	20130131	Product data sheet	-	74HC4050_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC4050_CNV v.2	19970826	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 12 March 2023