

STRUCTURE	Silicon Monolithic Integrated circuit
PRODUCT SERIES	Low ESR Capacitor Built in shut down SW, Low Dropout 500mA Regulator IC
TYPE	<b>B D X X K A 5 W F P</b>
FEATURES	<ul style="list-style-type: none"> <li>• Maximum Output Current : 500mA</li> <li>• High Precision Output Voltage : <math>\pm 1\%</math></li> </ul>

## ○ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage ※1	Vcc	-0.3~7.0	V
Control Input Voltage	VCTL	-0.3~Vcc	V
Power Dissipation ※2	Pd	1300	mW
Operating temperature range	Topr	-40~+105	°C
Storage Temperature range	Tstg	-55~+150	°C
Junction temperature	Tjmax	150	°C

※1 Do not however exceed Pd.

※2 Mounted on 70mm×70mm×1.6mm Glass Epoxy PCB, Pd derated at 10.4mW/°C for tempearure above Ta=25°C

## ○OPERATING CONDITIONS (Ta=-40~105°C, Do not however exceed Pd.)

Parameter	Symbol	Min	Max	Unit
Input Voltage	Vcc	2.3	5.5	V
Output current	Io	0	500	mA
Control Pin Input Voltage	VCTL	0	Vcc	V

NOTE : The product described in this specification is a strategic product (and/or service) subject to COCOM regulations. It should not be exported without authorization from the appropriate government.

NOTE : This product is not designed for protection against radioactive rays.

## Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.  
If there are any differences in translation version of this document, formal version takes priority.

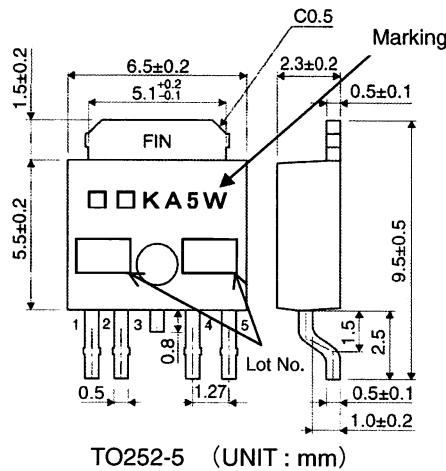
## ○ELECTRICAL CHARACTERISTICS

Unless otherwise specified,  $T_a=25^\circ\text{C}$ ,  $V_{CTL}=2\text{V}$   $V_{CC}=2.5\text{V}$  ( $V_o=1.0\text{V}, 1.2\text{V}, 1.5\text{V}, 1.8\text{V}$ ),  $V_{CC}=3.3\text{V}$  ( $V_o=2.5\text{V}$ ),  $V_{CC}=5.0\text{V}$  ( $V_o=3.0\text{V}, 3.3\text{V}$ )

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Output Voltage	$V_o$	$V_o(T)-0.015$	$V_o(T)$	$V_o(T)+0.015$	V	$I_o=200\text{mA}$ ( $V_o=1.0\text{V}, 1.2\text{V}$ )
		$V_o(T) \times 0.99$	$V_o(T)$	$V_o(T) \times 1.01$		$I_o=200\text{mA}$ ( $V_o \geq 1.5\text{V}$ )
Shut Down Current	$I_{SD}$	—	0	1	$\mu\text{A}$	$V_{CTL}=0\text{V}$ , $I_o=0\text{mA}$ (OFFmode)
Bias Current	$I_b$	—	350	550	$\mu\text{A}$	$I_o=0\text{mA}$
Dropout Voltage $\times 3$	$\Delta V_d$	—	0.12	0.20	V	$I_o=200\text{mA}$ , $V_{CC}=0.95 \times V_o$
Peak Output Current	$I_o$	500	—	—	mA	
Ripple Rejection	R.R.	—	50	—	dB	$f=120\text{Hz}$ , $ein^{\times 6}=-10\text{dBV}$ , $I_o=100\text{mA}$
Line Regulation $\times 4$	Reg.I	—	10	35	mV	$V_{CC}=V_o+0.5\text{V} \rightarrow 5.5\text{V}$ , $I_o=200\text{mA}$
Load Regulation	Reg.L	—	25	75	mV	$I_o=0\text{mA} \rightarrow 500\text{mA}$
Temperature Coefficient of Output Voltage $\times 5$	$T_{Cvo}$	—	$\pm 100$	—	ppm/ $^\circ\text{C}$	$I_o=5\text{mA}$ , $T_j=0 \sim 125^\circ\text{C}$
CTL ON Mode Voltage	$V_{CTLON}$	2.0	—	—	V	ACTIVE MODE, $I_o=0\text{mA}$
CTL OFF Mode Voltage	$V_{CTLOFF}$	—	—	0.8	V	OFF MODE, $I_o=0\text{mA}$
CTL Input Current	$I_{CTL}$	20	40	60	$\mu\text{A}$	$I_o=0\text{mA}$

 $V_o(T)$  : Output Voltage $\times 3$   $V_o \geq 2.5\text{V}$  $\times 4$   $1.0 \leq V_o \leq 1.8\text{V}$ ,  $V_{CC}=2.3\text{V} \rightarrow 5.5\text{V}$  $\times 5$  Designed Guarantee. (Outgoing inspection is not done on all products.) $\times 6$   $ein$  : Input Voltage Ripple

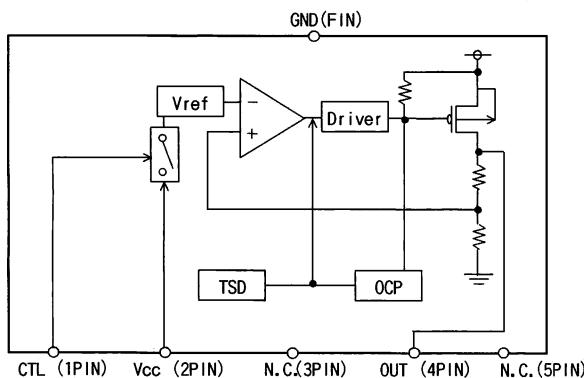
## ○PHYSICAL DIMENSIONS, MARKING



## ○OUTPUT VOLTAGE, MARKING

Type	Marking	Output Voltage(V)	Type	Marking	Output Voltage(V)
BD10KA5WFP	10KA5W	1.0	BD25KA5WFP	25KA5W	2.5
BD12KA5WFP	12KA5W	1.2	BD30KA5WFP	30KA5W	3.0
BD15KA5WFP	15KA5W	1.5	BD33KA5WFP	33KA5W	3.3
BD18KA5WFP	18KA5W	1.8			

## OBLOCK DIAGRAM



## OPIN NO. , PIN NAME

Pin Number	Pin Name
1	CTL
2	Vcc
3	N.C.
4	OUT
5	N.C.
FIN	GND

\* Please refer to technical note concerning application circuit, and etc.

## ONOTES FOR USE

## 1. Absolute maximum range

Absolute Maximum Ratings are those values beyond which the life of a device may be destroyed we cannot be defined the failure mode, such as short mode or open mode.

Therefore physical security countermeasure, like fuse, is to be given when a specific mode to be beyond absolute maximum ratings is considered.

## 2. GND pin voltage

GND terminal should be connected the lowest voltage, under all conditions. And all terminals except GND should be under GND terminal voltage under all conditions including transient situations.

## 3. Power dissipation

If IC is used on condition that the power loss is over the power dissipation, the reliability will become worse by heat up, such as reduced output current capability.

Also, be sure to use this IC within a power dissipation range allowing enough of margin.

## 4. Electrical characteristics described in these specifications may vary, depending on temperature, supply voltage, external circuits and other conditions. Therefore, be sure to check all relevant factors, including transient characteristics.

5. Be sure to connect a capacitor between the output pin and GND to prevent oscillation. Note that if the capacity of the capacitor changes due to factors such as changes in temperature, oscillation may occur. A ceramic capacitor or other low ESR ( $1\ \mu F$ ) capacitor is recommended to prevent oscillation. Ceramic capacitors generally have thermal and DC bias characteristics to consider. In selecting a ceramic capacitor, high voltage X5R or X7R versions or better are recommended for their superior thermal and DC bias characteristics. However, in situations such as rapid fluctuation of the input voltage or the load, please check the operation in real application to determine the proper capacitor.

## 6. Overcurrent protection circuit

The built-in overcurrent protection circuit is designed to respond to the output current and prevent destruction of the IC from load short circuits; however, it is only effective in protecting the IC from destruction in sudden overcurrent accidents. The protection circuit is not to be used continuously, or for transitions. In executing thermal design, bear in mind that overcurrent protection has negative characteristic according with the temperature.

## 7. Thermal shutdown circuit

A built-in internal shutdown (TSD) circuit is provided to protect the IC from heat destruction. Operation has to be done within the allowable loss range, but in continuous use beyond the range, chip temperature  $T_j$  will increase to the threshold, activating the TSD circuit and turning the output power  $T_r$  OFF. Once the chip temperature  $T_j$  returns to the normal range, the circuit is automatically restored. Note that the TSD circuit is designed to operate over the maximum absolute rating. Therefore, make absolutely certain not to use the TSD function in set design.

## 8. Mounting Failures

Mounting failure, such as misdirection or mismount, may cause a malfunction in the device.

9. Internal circuits or elements may be damaged when Vcc and pin voltage are reversed. For example, Vcc short circuit to GND while a external capacitor is charged. Output pin capacitor is recommended no larger than  $1000\ \mu F$ . In addition, inserting a Vcc series countercurrent prevention diode, or a bypass diode between the various pins and the vcc, is recommended.

10. Malfunction may be happened when the device is used in the strong electromagnetic field.
11. We recommend to put Diode for protection purpose in case of output pin connected with large load of impedance or reserve current occurred at initial and output off.

12. Precautions for board inspection

Connecting low-impedance capacitors to run inspections with the board may produce stress on the IC. Therefore, be certain to use proper discharge procedure before each process of the test operation. To prevent electrostatic accumulation and discharge in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handling, transfer and storage operations. Before attempting to connect components to the test setup, make certain that the power supply is OFF. Likewise, be sure the power supply is OFF before removing any component connected to the test setup.

13. GND pattern

When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid voltage fluctuations in any connected external component GND.

## Appendix

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(Contact address for overseas customers in Japan)

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