

Features

- 'HC161, 'HCT161 4-Bit Binary Counter, Asynchronous Reset
- 'HC163, 'HCT163 4-Bit Binary Counter, Synchronous Reset
- Synchronous Counting and Loading
- Two Count Enable Inputs for n-Bit Cascading
- Look-Ahead Carry for High-Speed Counting
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The 'HC161, 'HCT161, 'HC163, and 'HCT163 are presettable synchronous counters that feature look-ahead carry logic for use in high-speed counting applications. The 'HC161 and 'HCT161 are asynchronous reset decade and binary counters, respectively; the 'HC163 and 'HCT163 devices are decade and binary counters, respectively, that are reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

A low level on the synchronous parallel enable input, SPE, disables counting operation and allows data at the P0 to P3 inputs to be loaded into the counter (provided that the setup and hold requirements for SPE are met).

All counters are reset with a low level on the Master Reset input, MR. In the 'HC163 and 'HCT163 counters (synchronous reset types), the requirements for setup and hold time with respect to the clock must be met.

Two count enables, PE and TE, in each counter are provided for n-bit cascading. In all counters reset action occurs regardless of the level of the $\overline{SPE}$, PE and TE inputs (and the clock input, CP, in the 'HC161 and 'HCT161 types).

If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count as shown in state diagram.

The look-ahead carry feature simplifies serial cascading of the counters. Both count enable inputs (PE and TE) must be high to count. The TE input is gated with the Q outputs of all four stages so that at the maximum count the terminal count (TC) output goes high for one clock period. This TC pulse is used to enable the next cascaded stage.

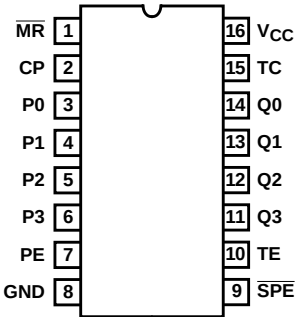
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC161F3A	-55 to 125	16 Ld CERDIP
CD54HC163F3A	-55 to 125	16 Ld CERDIP
CD54HCT163F3A	-55 to 125	16 Ld CERDIP
CD74HC161E	-55 to 125	16 Ld PDIP
CD74HC161M	-55 to 125	16 Ld SOIC
CD74HC161MT	-55 to 125	16 Ld SOIC
CD74HC161M96	-55 to 125	16 Ld SOIC
CD74HC163E	-55 to 125	16 Ld PDIP
CD74HC163M	-55 to 125	16 Ld SOIC
CD74HC163MT	-55 to 125	16 Ld SOIC
CD74HC163M96	-55 to 125	16 Ld SOIC
CD74HCT161E	-55 to 125	16 Ld PDIP
CD74HCT161M	-55 to 125	16 Ld SOIC
CD74HCT161MT	-55 to 125	16 Ld SOIC
CD74HCT161M96	-55 to 125	16 Ld SOIC
CD74HCT163E	-55 to 125	16 Ld PDIP
CD74HCT163M	-55 to 125	16 Ld SOIC
CD74HCT163MT	-55 to 125	16 Ld SOIC
CD74HCT163M96	-55 to 125	16 Ld SOIC

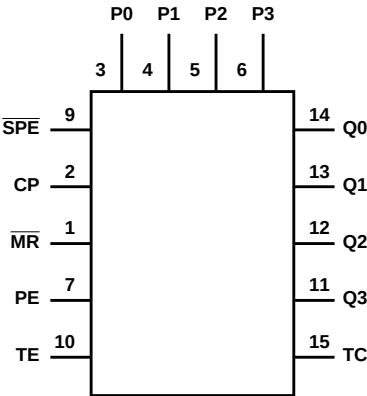
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

CD54HC161, CD54HCT161, CD54HC163, CD54HCT163
(CERDIP)
CD74HC161, CD74HCT161, CD74HC163, CD74HCT163
(PDIP, SOIC)
TOP VIEW



Functional Diagram



CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163

MODE SELECT - FUNCTION TABLE FOR 'HC161 AND 'HCT161

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	P_n	Q_n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(Note 1)
Count	H	↑	h	h	h (Note 3)	X	Count	(Note 1)
Inhibit	H	X	l (Note 2)	X	h (Note 3)	X	q_n	(Note 1)
	H	X	X	l (Note 2)	h (Note 3)	X	q_n	L

MODE SELECT - FUNCTION TABLE FOR 'HC163 AND 'HCT163

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	P_n	Q_n	TC
Reset (Clear)	l	↑	X	X	X	X	L	L
Parallel Load	h (Note 3)	↑	X	X	l	l	L	L
	h (Note 3)	↑	X	X	l	h	H	(Note 1)
Count	h (Note 3)	↑	h	h	h (Note 3)	X	Count	(Note 1)
Inhibit	h (Note 3)	X	l (Note 2)	X	h (Note 3)	X	q_n	(Note 1)
	h (Note 3)	X	X	l (Note 2)	h (Note 3)	X	q_n	L

H = High voltage level steady state; L = Low voltage level steady state; h = High voltage level one setup time prior to the Low-to-High clock transition; l = Low voltage level one setup time prior to the Low-to-High clock transition; X = Don't Care; q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition; ↑ = Low-to-High clock transition.

NOTES:

1. The TC output is High when TE is High and the counter is at Terminal Count (HHHH for HC/HCT161 and 'HC/HCT163).
2. The High-to-Low transition of PE or TE on the 'HC/HCT161 and the 'HC/HCT163 should only occur while CP is HIGH for conventional operation.
3. The Low-to-High transition of $\overline{SPE}$ on the 'HC/HCT161 and $\overline{SPE}$ or $\overline{MR}$ on the 'HC/HCT163 should only occur while CP is HIGH for conventional operation.

CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} -0.5V to 7V
 DC Input Diode Current, I_{IK}
 For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ $\pm 20mA$
 DC Output Diode Current, I_{OK}
 For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ $\pm 20mA$
 DC Drain Current, per Output, I_O
 For $-0.5V < V_O < V_{CC} + 0.5V$ $\pm 25mA$
 DC Output Source or Sink Current per Output Pin, I_O
 For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ $\pm 25mA$
 DC V_{CC} or Ground Current, I_{CC} $\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} ($^{\circ}C/W$)
 E (PDIP) Package 67
 M (SOIC) Package 73
 Maximum Junction Temperature $150^{\circ}C$
 Maximum Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 Maximum Lead Temperature (Soldering 10s) $300^{\circ}C$
 (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range, T_A $-55^{\circ}C$ to $125^{\circ}C$
 Supply Voltage Range, V_{CC}
 HC Types 2V to 6V
 HCT Types 4.5V to 5.5V
 DC Input or Output Voltage, V_I , V_O 0V to V_{CC}
 Input Rise and Fall Time
 2V 1000ns (Max)
 4.5V 500ns (Max)
 6V 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	V _{OH}	V _{IH} or V _{IL}	-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V _{OL}	V _{IH} or V _{IL}	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA

CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μA
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	0	5.5	-		±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 5)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

5. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
P0 - P3	0.25
PE	0.65
CP	1.05
MR	0.8
SPE	0.5
TE	1.05

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163

Prerequisite For Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Maximum CP Frequency (Note 6)	f _{MAX}	-	2	6	-	-	5	-	4	-	MHz
			4.5	30	-	-	24	-	20	-	MHz
			6	35	-	-	28	-	24	-	MHz
CP Width (Low)	t _{W(L)}	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
MR Pulse Width (161)	t _W	-	2	100	-	-	125	-	150	-	ns
			4.5	20	-	-	25	-	30	-	ns
			6	17	-	-	21	-	26	-	ns
Setup Time, Pn to CP	t _{SU}	-	2	60	-	-	75	-	90	-	ns
			4.5	12	-	-	15	-	18	-	ns
			6	10	-	-	13	-	15	-	ns
Setup Time, PE or TE to CP	t _{SU}	-	2	50	-	-	65	-	75	-	ns
			4.5	10	-	-	13	-	15	-	ns
			6	9	-	-	11	-	13	-	ns
Setup Time, $\overline{SPE}$ to CP	t _{SU}	-	2	60	-	-	75	-	90	-	ns
			4.5	12	-	-	15	-	18	-	ns
			6	10	-	-	13	-	15	-	ns
Setup Time, $\overline{MR}$ to CP (163)	t _{SU}	-	2	65	-	-	80	-	100	-	ns
			4.5	13	-	-	16	-	20	-	ns
			6	11	-	-	14	-	17	-	ns
Hold Time, PN to CP	t _H	-	2	3	-	-	3	-	3	-	ns
			4.5	3	-	-	3	-	3	-	ns
			6	3	-	-	3	-	3	-	ns
Hold Time, TE or PE to CP	t _H	-	2	0	-	-	0	-	0	-	ns
			4.5	0	-	-	0	-	0	-	ns
			6	0	-	-	0	-	0	-	ns
Hold Time, $\overline{SPE}$ to CP	t _H	-	2	0	-	-	0	-	0	-	ns
			4.5	0	-	-	0	-	0	-	ns
			6	0	-	-	0	-	0	-	ns
Recovery Time, $\overline{MR}$ to CP (161)	t _{REC}	-	2	75	-	-	95	-	110	-	ns
			4.5	15	-	-	19	-	22	-	ns
			6	13	-	-	16	-	19	-	ns

CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163

Prerequisite For Switching Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES											
Maximum CP Frequency	f _{MAX}	-	4.5	30	-	-	24	-	20	-	MHz
CP Width (Low) (Note 6)	t _{W(L)}	-	4.5	16	-	-	20	-	24	-	ns
$\overline{\text{MR}}$ Pulse Width (161)	t _W	-	4.5	20	-	-	25	-	30	-	ns
Setup Time, Pn to CP	t _{SU}	-	4.5	10	-	-	13	-	15	-	ns
Setup Time, PE or TE to CP	t _{SU}	-	4.5	13	-	-	16	-	20	-	ns
Setup Time, $\overline{\text{SPE}}$ to CP	t _{SU}	-	4.5	12	-	-	15	-	18	-	ns
Setup Time, $\overline{\text{MR}}$ to CP (163)	t _{SU}	-	4.5	13	-	-	16	-	20	-	ns
Hold Time, PN to CP	t _H	-	4.5	5	-	-	5	-	5	-	ns
Hold Time, TE or PE to CP	t _H	-	4.5	3	-	-	3	-	3	-	ns
Hold Time, $\overline{\text{SPE}}$ to CP	t _H	-	4.5	3	-	-	3	-	3	-	ns
Recovery Time, $\overline{\text{MR}}$ to CP (161)	t _{REC}	-	4.5	15	-	-	19	-	22	-	ns

NOTE:

6. Applies to non-cascaded operation only. With cascaded counters clock to terminal count propagation delays, count enables (PE or TE)-to-clock setup times, and count enables (PE or TE)-to-clock hold times determine maximum clock frequency. For example with these HC devices:

$$f_{\text{MAX}} (\text{CP}) = \frac{1}{\text{CP-to-TC prop. delay} + \text{TE-to-CP setup} + \text{TE-to-CP Hold}} = \frac{1}{37 + 10 + 0} \approx 21\text{MHz}(\text{min})$$

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay CP to TC	t _{PHL} , t _{PLH}	C _L = 50pF	2	-	-	185	-	230	-	280	ns
			4.5	-	-	37	-	46	-	56	ns
		C _L = 15pF	5	-	15	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	31	-	39	-	48	ns
CP to Qn	t _{PHL} , t _{PLH}	C _L = 50pF	2	-	-	185	-	230	-	280	ns
			4.5	-	-	37	-	46	-	56	ns
		C _L = 15pF	5	-	15	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	31	-	39	-	48	ns
TE to TC	t _{PHL} , t _{PLH}	C _L = 50pF	2	-	-	120	-	150	-	180	ns
			4.5	-	-	24	-	30	-	36	ns
		C _L = 15pF	5	-	9	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	20	-	26	-	31	ns

CD54/74HC161, CD54/74HCT161, CD54/74HC163, CD54/74HCT163

Switching Specifications $C_L = 50\text{pF}$, Input t_r , $t_f = 6\text{ns}$ (Continued)

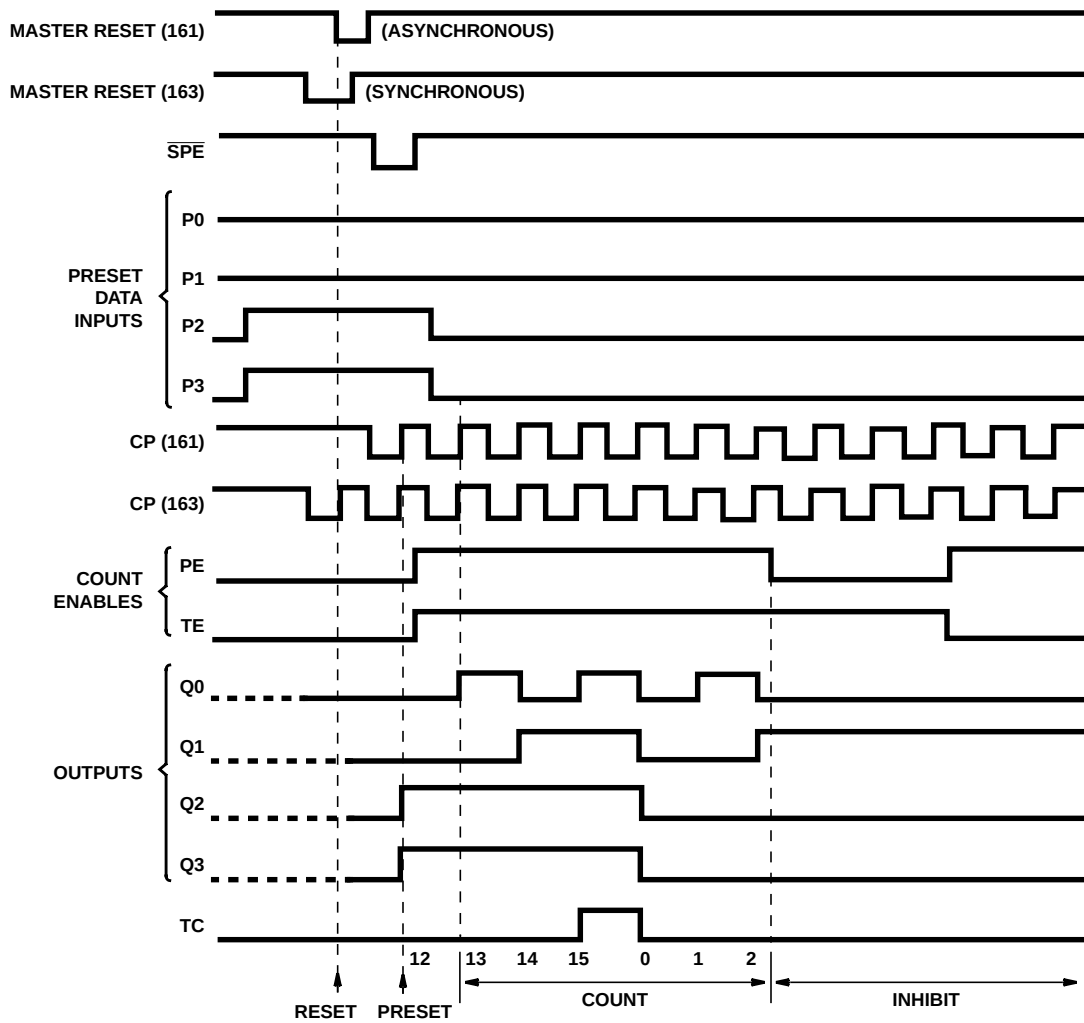
PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{MR}$ to Qn (161)	t_{PHL}	$C_L = 50\text{pF}$	2	-	-	210	-	265	-	315	ns
			4.5	-	-	42	-	53	-	63	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	36	-	45	-	54	ns
$\overline{MR}$ to TC (161)	t_{PHL}	$C_L = 50\text{pF}$	2	-	-	210	-	265	-	315	ns
			4.5	-	-	42	-	53	-	63	ns
		$C_L = 50\text{pF}$	6	-	-	36	-	45	-	54	ns
Output Transition Time	t_{THL}, t_{TLH}	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Power Dissipation Capacitance (Notes 7, 8)	C_{PD}	-	5	-	60	-	-	-	-	-	pF
Input Capacitance	C_{IN}	$C_L = 50\text{pF}$	-	10	-	10	-	10	-	10	pF
HCT TYPES											
Propagation Delay CP to TC	t_{PHL}, t_{PLH}	$C_L = 50\text{pF}$	4.5	-	-	42	-	53	-	63	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
CP to Qn	t_{PHL}, t_{PLH}	$C_L = 50\text{pF}$	4.5	-	-	39	-	49	-	59	ns
		$C_L = 15\text{pF}$	5	-	16	-	-	-	-	-	ns
TE to TC	t_{PHL}, t_{PLH}	$C_L = 50\text{pF}$	4.5	-	-	32	-	40	-	48	ns
		$C_L = 15\text{pF}$	5	-	13	-	-	-	-	-	ns
$\overline{MR}$ to Qn (161)	t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	50	-	63	-	75	ns
		$C_L = 15\text{pF}$	5	-	21	-	-	-	-	-	ns
$\overline{MR}$ to TC (161)	t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	50	-	63	-	75	ns
Output Transition Time	t_{THL}, t_{TLH}	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Power Dissipation Capacitance (Notes 7, 8)	C_{PD}	-	5	-	63	-	-	-	-	-	pF
Input Capacitance	C_{IN}	$C_L = 50\text{pF}$	-	10	-	10	-	10	-	10	pF

NOTES:

7. C_{PD} is used to determine the dynamic power consumption, per package.

8. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_O)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

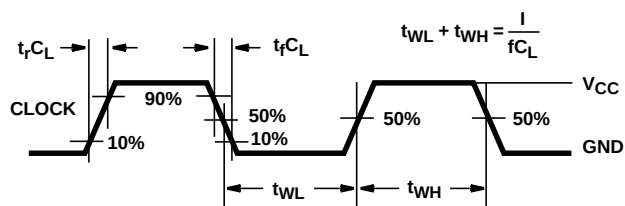
Timing Diagram



Sequence illustrated on waveforms:

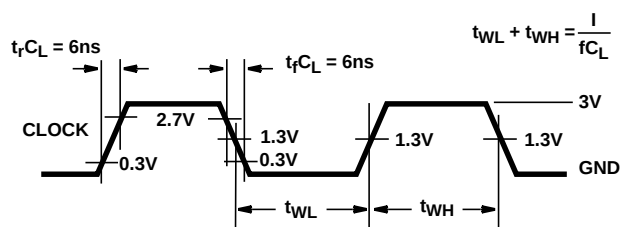
1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

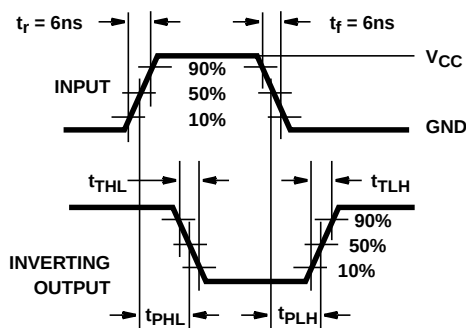


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

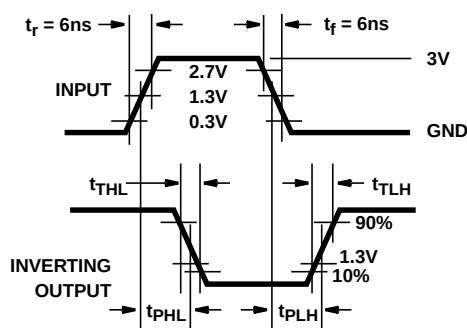


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

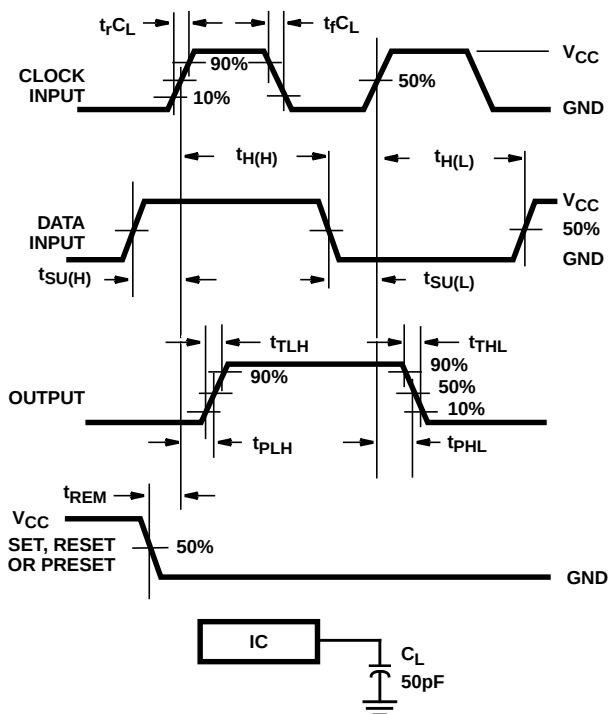


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

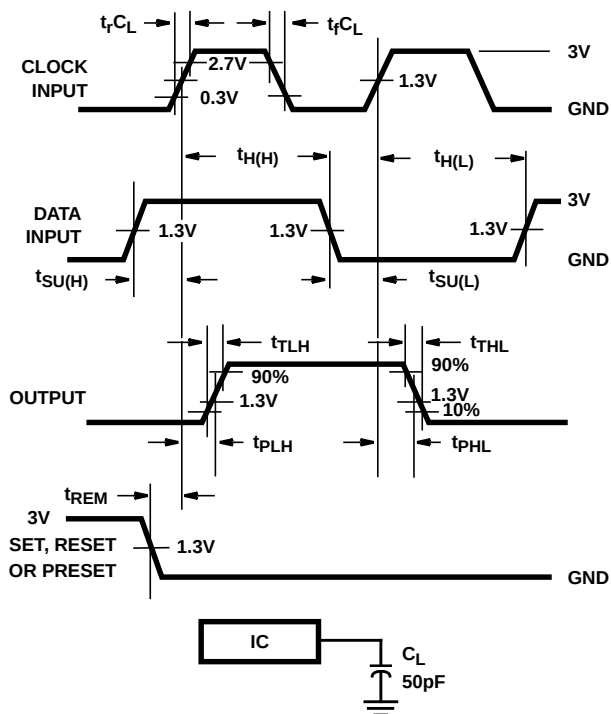


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54HC161F	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC161F
CD54HC161F.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC161F
CD54HC161F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407501EA CD54HC161F3A
CD54HC161F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407501EA CD54HC161F3A
CD54HC163F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8607601EA CD54HC163F3A
CD54HC163F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8607601EA CD54HC163F3A
CD54HCT163F	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT163F
CD54HCT163F.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT163F
CD54HCT163F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT163F3A
CD54HCT163F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT163F3A
CD74HC161E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC161E
CD74HC161E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC161E
CD74HC161M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC161M
CD74HC161M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC161M
CD74HC161M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC161M
CD74HC163E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC163E
CD74HC163E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC163E
CD74HC163M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC163M
CD74HC163M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC163M
CD74HC163M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC163M
CD74HC163MT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC163M
CD74HCT161E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT161E
CD74HCT161E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT161E
CD74HCT161EE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT161E
CD74HCT161M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT161M
CD74HCT161M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT161M

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HCT161M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT161M
CD74HCT163E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT163E
CD74HCT163E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT163E
CD74HCT163M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT163M
CD74HCT163M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT163M
CD74HCT163M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT163M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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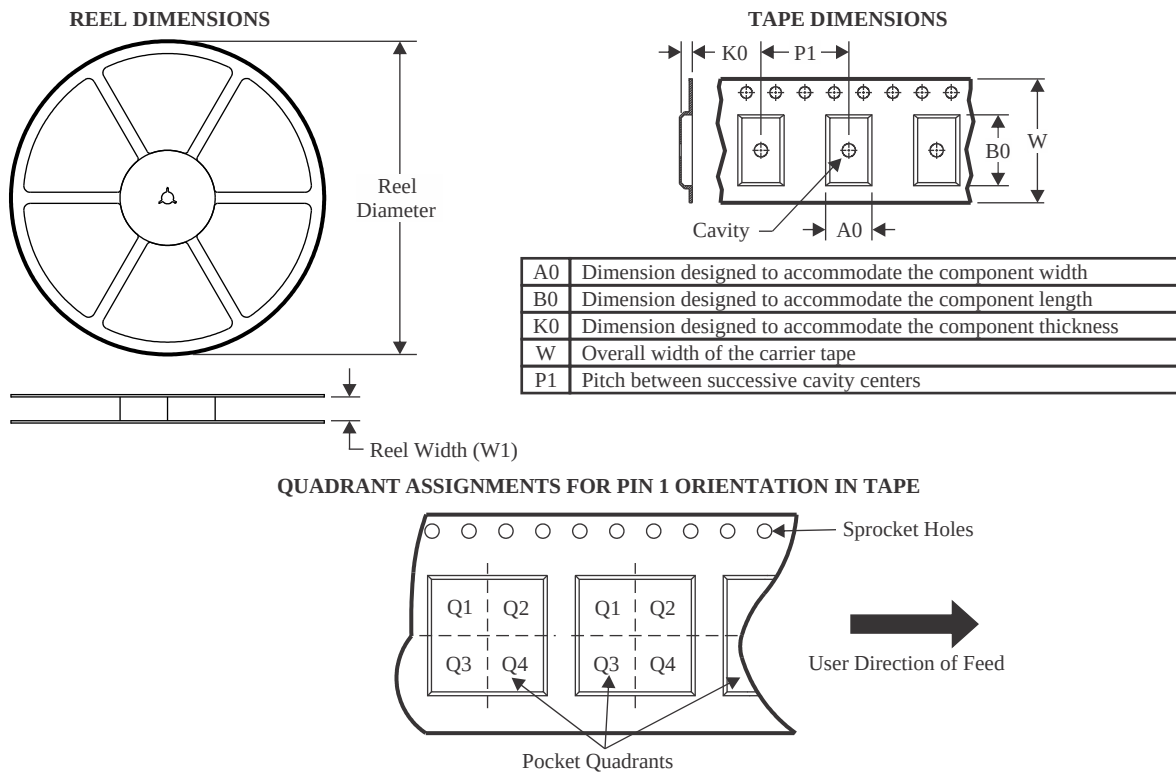
OTHER QUALIFIED VERSIONS OF CD54HC161, CD54HC163, CD54HCT163, CD74HC161, CD74HC163, CD74HCT163 :

- Catalog : [CD74HC161](#), [CD74HC163](#), [CD74HCT163](#)
- Military : [CD54HC161](#), [CD54HC163](#), [CD54HCT163](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

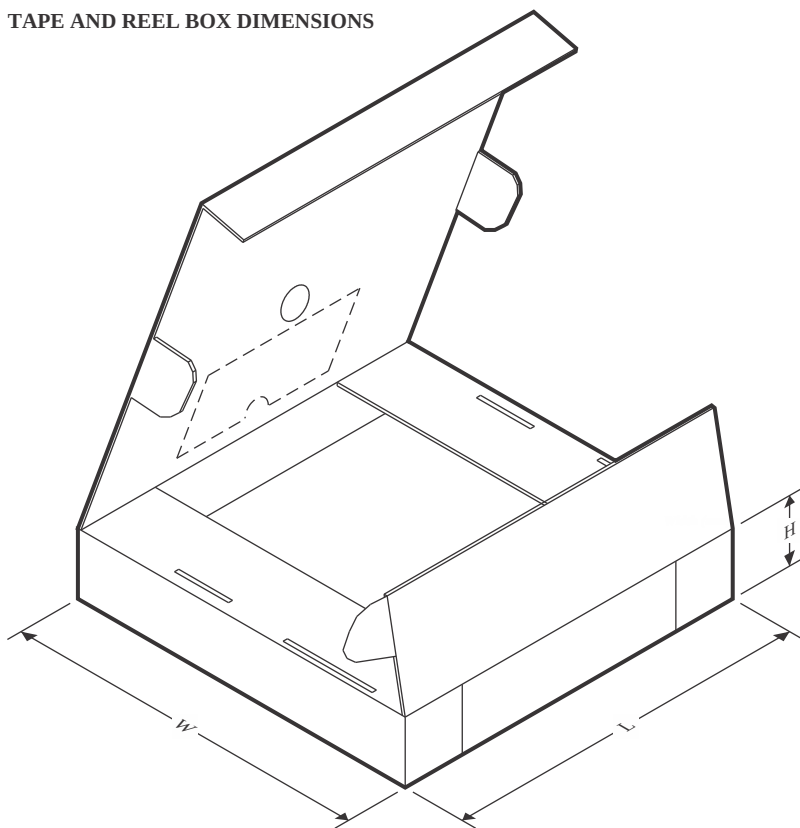
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC161M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC163M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT161M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT163M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC161M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC163M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HCT161M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT163M96	SOIC	D	16	2500	353.0	353.0	32.0

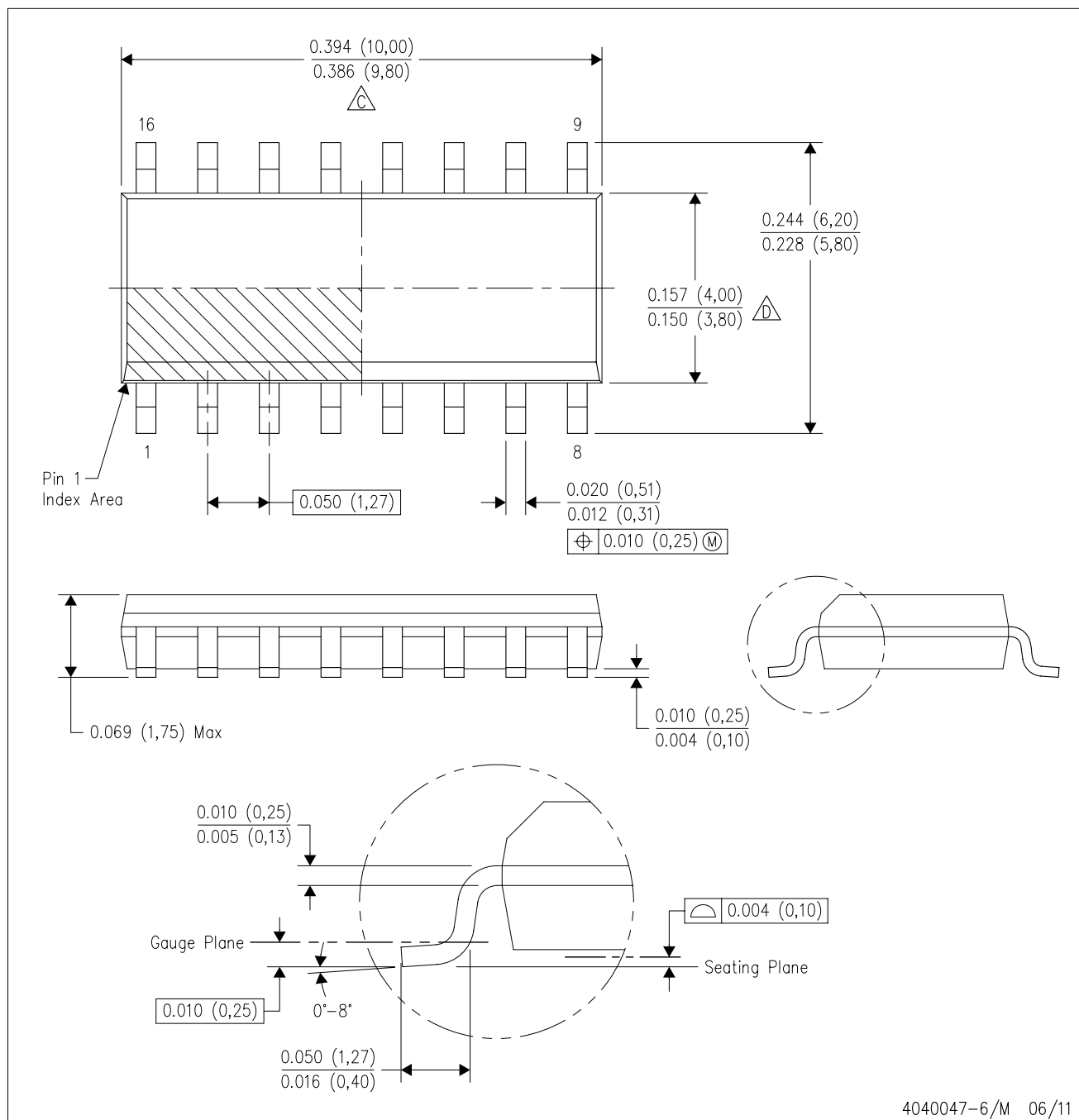
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC161E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC161E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC161E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC161E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC163E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC163E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC163E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC163E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT161E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT161E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT161E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT161E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT161EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT161EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT163E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT163E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT163E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT163E.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

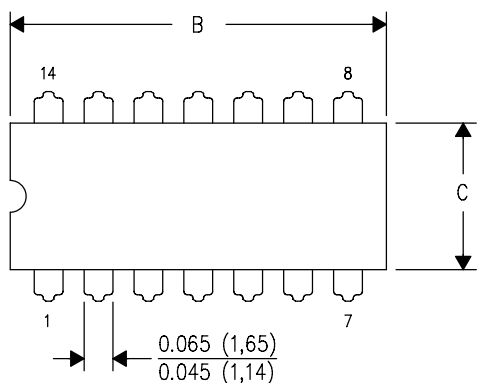


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

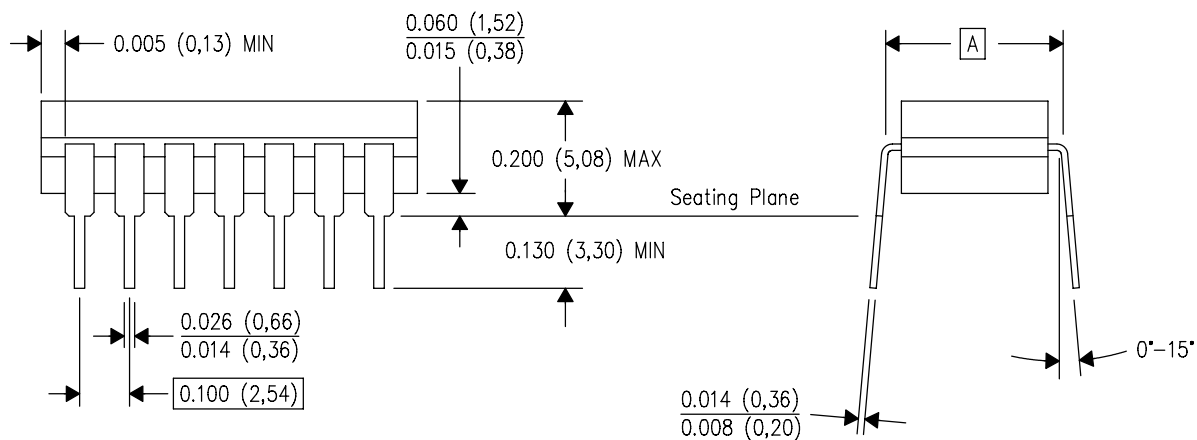
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



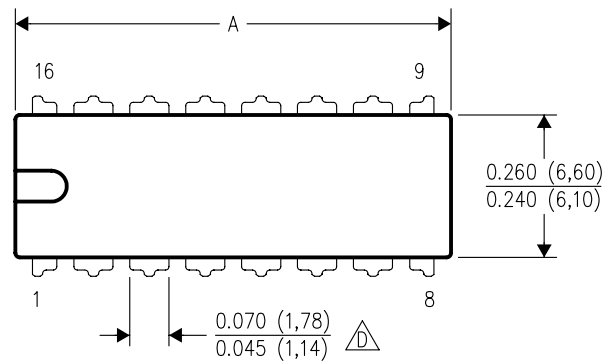
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

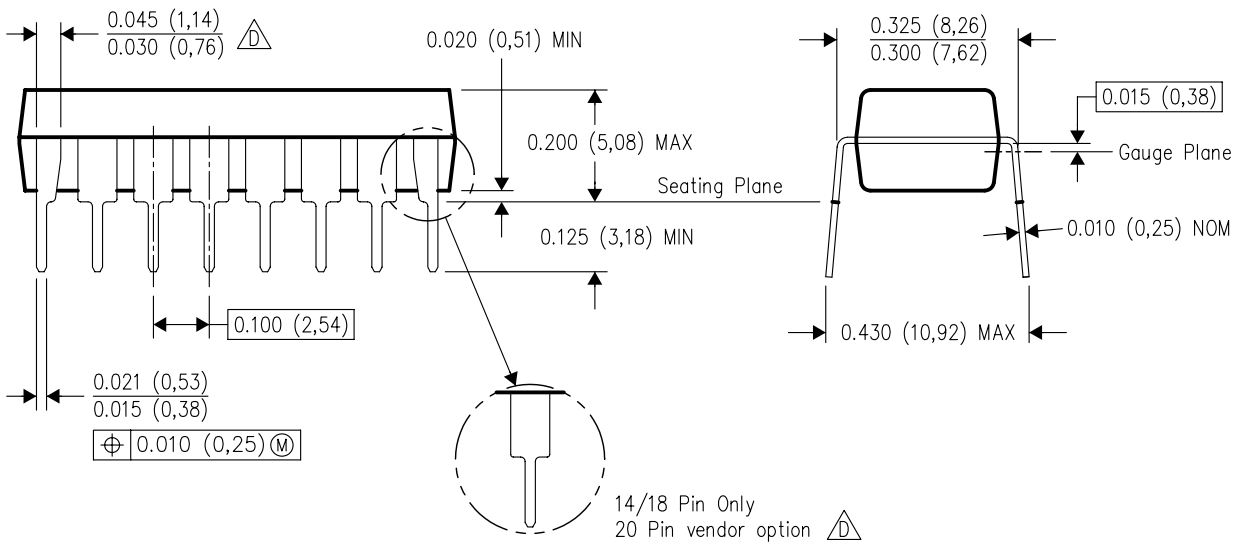
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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