

DATA SHEET

SKY65120-21: 2110-2170 MHz High Linearity, 2 W Power Amplifier

Applications

- WCDMA, PCS, DCS, UMTS, TD-SCDMA
- Repeaters
- ISM band transmitters
- WCS fixed wireless systems

Features

- High linearity: OIP3 > +48 dBm
- OP1dB = +33.5 dBm
- ACLR = -45 dBc for P_{OUT} = +25.4 dBm
- High efficiency: PAE = 42%
- High gain = 24.6 dB
- Internal RF match and bias circuits
- Single DC supply: 5 V
- Small footprint, MCM (20-pin, 6 x 6 mm) SMT package (MSL3, 260 °C per JEDEC J-STD-020)



Skyworks Pb-free products are compliant with all applicable legislation. For additional information, refer to *Skyworks Definition of Lead (Pb)-Free*, document number SQ04-0073.

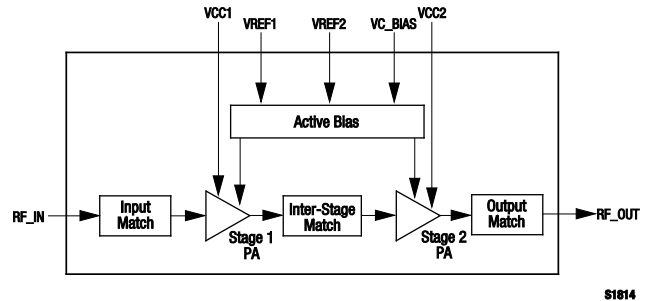


Figure 1. SKY65120-21 Block Diagram

Description

Skyworks SKY65120-21 is a fully-matched, surface mount Power Amplifier (PA) designed for WCDMA, PCS, DCS, UMTS, and TD-SCDMA radio, repeaters, transmitters, and WCS fixed wireless units operating in the 2110 to 2170 MHz bandwidth.

All active circuitry in the module is contained in a single GaAs Microwave Monolithic Integrated Circuit (MMIC). The device is manufactured using Skyworks AlGaAs Heterojunction Bipolar Transistor (HBT) process, which allows for single supply operation while maintaining high efficiency and good linearity.

A block diagram of the SKY65120-21 is shown in Figure 1. The device package and pinout for the 20-pin MCM are shown in Figure 2.

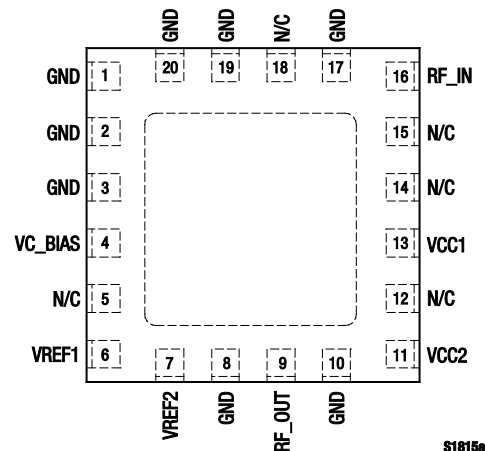


Figure 2. SKY65120-21 Pinout – 20-Pin MCM (Top View)

Table 1. SKY65120-21 Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	GND	Ground	11	VCC2	Stage 2 collector voltage
2	GND	Ground	12	N/C	No connection
3	GND	Ground	13	VCC1	Stage 1 collector voltage
4	VC_BIAS	Bias voltage	14	N/C	No connection
5	N/C	No connection	15	N/C	No connection
6	VREF1	Bias reference voltage 1	16	RF_IN	RF input
7	VREF2	Bias reference voltage 2	17	GND	Ground
8	GND	Ground	18	N/C	No connection
9	RF_OUT	RF output	19	GND	Ground
10	GND	Ground	20	GND	Ground

Note: The center ground pad must have a low inductance and low thermal resistance connection to the application's printed circuit board ground plane.

Table 2. SKY65120-21 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
RF input power (for pulsed operation with duty cycle <25%)	P _{IN}		+10	dBm
Power dissipation	P _{DISS}		2.7	W
RF output power	P _{OUT}		+33.5	dBm
Supply voltage	VC_BIAS, VREF1, VREF2, VCC1, and VCC2		5.5	V
Supply current	I _{CC}		1100	mA
Operating temperature	T _{OP}	-40	+85	°C
Storage temperature	T _{ST}	-55	+125	°C
Junction temperature	T _J		+150	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Technical Description

The SKY65120-21 PA contains two amplifier stages. The matching circuits for the input stage, interstage, and output stage are contained within the device. An on-chip active bias circuit is included within the device for both input and output stages, which provides excellent gain tracking over temperature and voltage variations.

The SKY65120-21 is internally matched for optimum linearity and efficiency. The input and output stages are independently supplied using the VCC1 and VCC2 supply lines (pins 13 and 11, respectively). The bias reference voltages for stages 1 and 2 are supplied using common lines VREF1 and VREF2 (pins 6 and 7,

respectively). The DC control voltage that sets the bias to stages 1 and 2 is supplied by the VC_BIAS signal (pin 4).

Electrical and Mechanical Specifications

Signal pin assignments and functional pin descriptions are described in Table 1. The absolute maximum ratings of the SKY65120-21 are provided in Table 2. Recommended operating conditions are specified in Table 3 and electrical specifications are provided in Table 4.

Typical performance characteristics are shown in Figures 3 through 30.

Table 3. SKY65120-21 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	VC_BIAS, VREF1, VREF2, VCC1, and VCC2		5.0	5.5	V
Operating frequency	f	2110		2170	MHz
Operating temperature	T _{OP}	−40	+25	+85	°C

Table 4. SKY65120-21 Electrical Specifications (Note 1)(VCC1 = VCC2 = VREF1 = VREF2 = VC_BIAS = 5 V, T_{OP} = +25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Frequency	f		2110		2170	MHz
Small signal gain	S ₂₁	P _{IN} = −25 dBm	23.0	24.6		dB
Input return loss	S ₁₁	P _{IN} = −25 dBm	10.0	16.8		dB
1 dB Output Compression Point	OP1dB	CW	+32.5	+33.5		dBm
3 rd Order Output Intercept Point	OIP3	P _{OUT} /tone = +24 dBm, Δf = 5 MHz	+44	+48		dBm
Noise Figure	NF	CW		8.4	9.0	dB
Adjacent Channel Leakage Ratio @ P _{OUT} = −45 dBc	ACLR	WCDMA test tone #1: 64 DPCH	+25.0	+25.4		dBm
Power Added Efficiency @ ACLR = −45 dBc	PAE _{ACLR}	WCDMA test tone #1: 64 DPCH		12		%
Power Added Efficiency	PAE	CW, P _{OUT} @ P1dB	33	42		%
Quiescent Current	I _{CCQ}	No RF signal	420	447	470	mA
Thermal resistance	Θ _{JC}	Junction to case		24		°C/W

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Typical Performance Characteristics

(VCC1 = VCC2 = VREF1 = VREF2 = VC_BIAS = 5 V, T_{OP} = +25 °C, f = 2140 MHz, P_{IN} = -25 dBm, Unless Otherwise Noted)

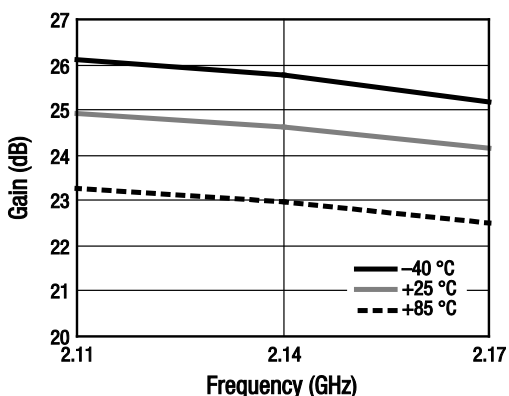


Figure 3. Gain vs Frequency Over Temperature

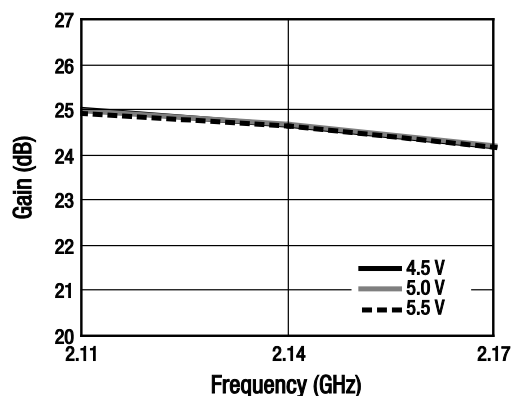


Figure 4. Gain vs Frequency Over Voltage

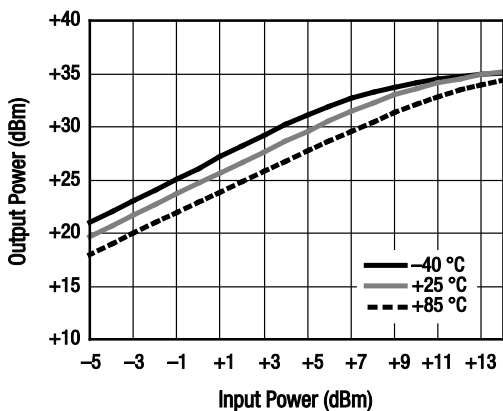


Figure 5. Output Power vs Input Power Over Temperature

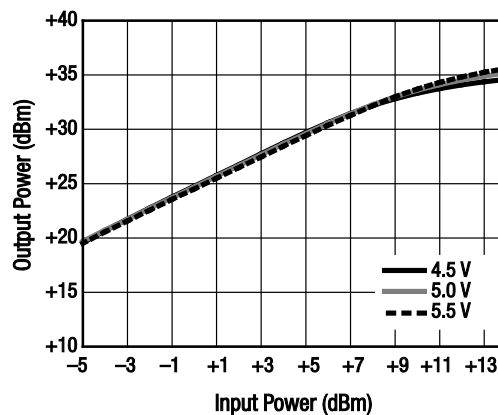


Figure 6. Output Power vs Input Power Over Voltage

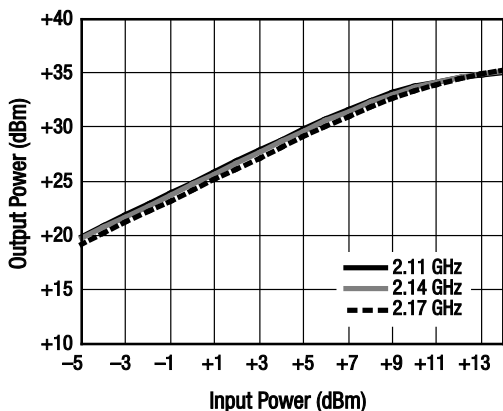


Figure 7. Output Power vs Input Power Over Frequency

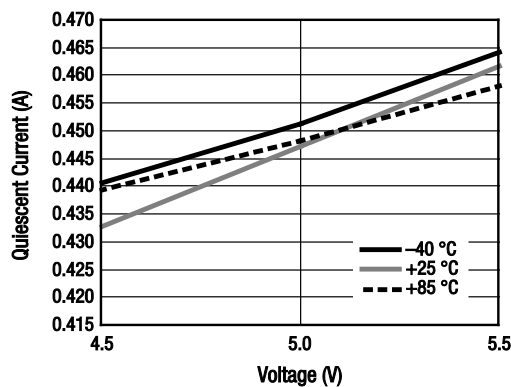


Figure 8. Quiescent Current vs Voltage Over Temperature

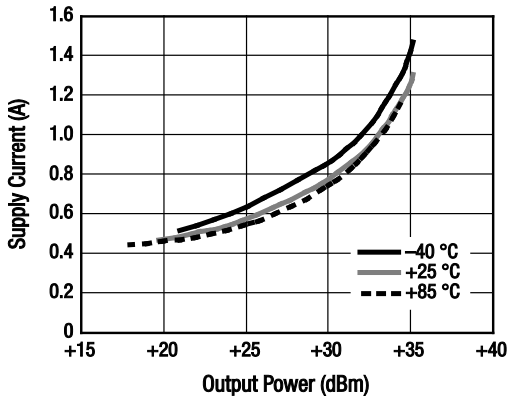


Figure 9. Supply Current vs Output Power Over Temperature

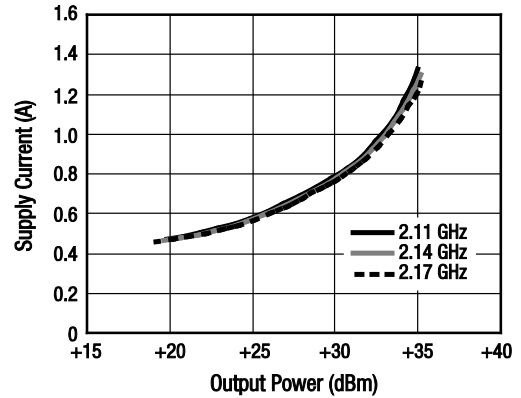


Figure 10. Supply Current vs Output Power Over Frequency

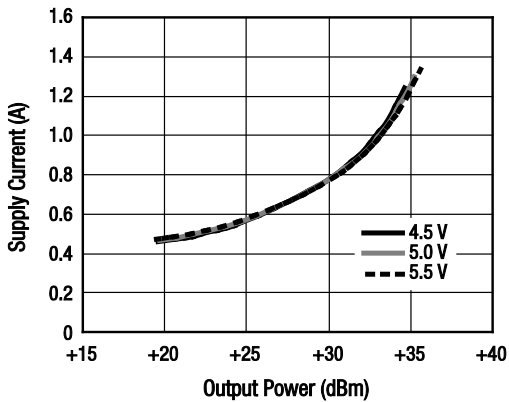


Figure 11. Supply Current vs Output Power Over Voltage

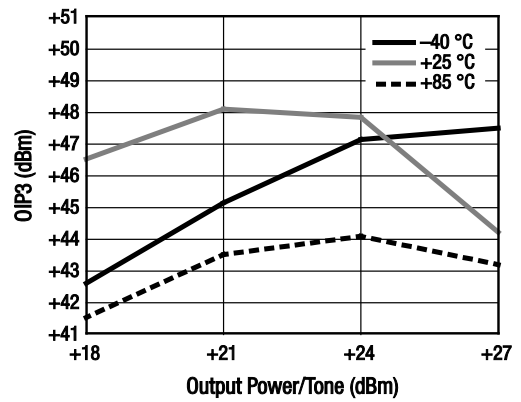


Figure 12. OIP3 vs Output Power/Tone Over Temperature ($\Delta f = 5$ MHz)

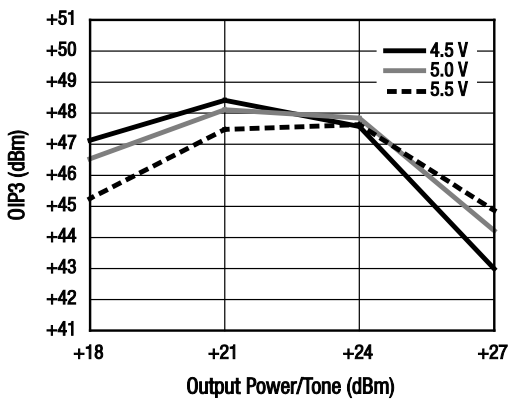


Figure 13. OIP3 vs Output Power/Tone Over Voltage ($\Delta f = 5$ MHz)

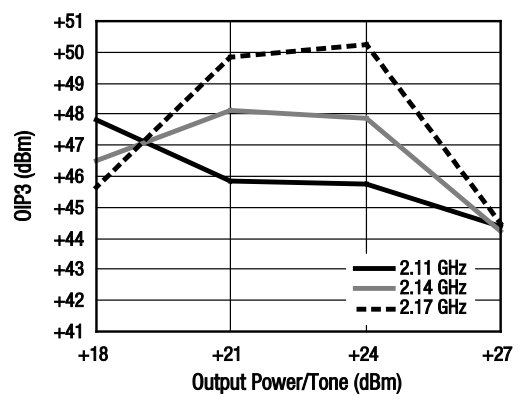


Figure 14. OIP3 vs Output Power/Tone Over Frequency ($\Delta f = 5$ MHz)

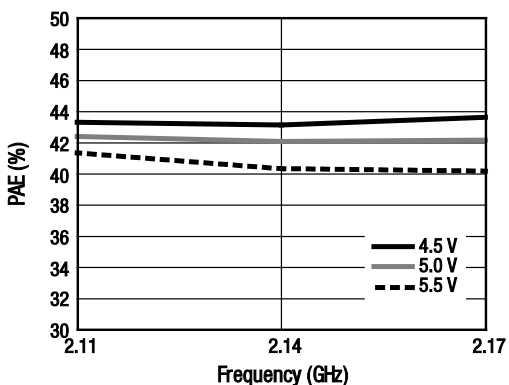


Figure 15. PAE vs Frequency Over Voltage

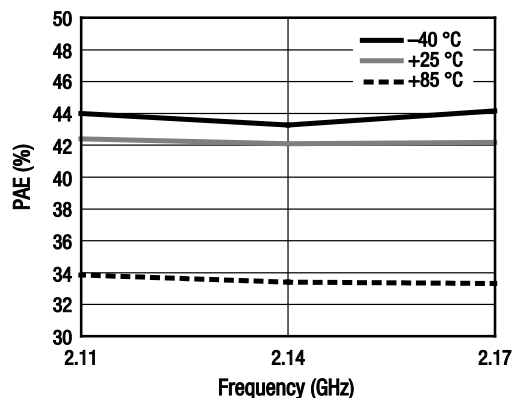


Figure 16. PAE vs Frequency Over Temperature

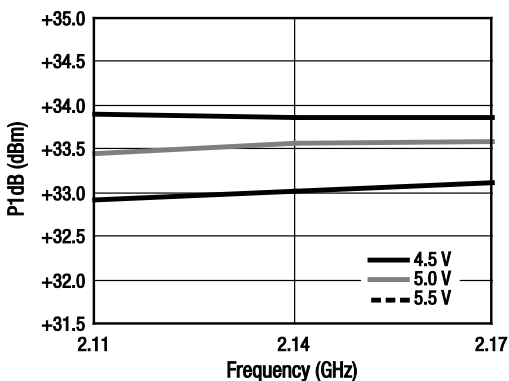


Figure 17. P1dB vs Frequency Over Voltage

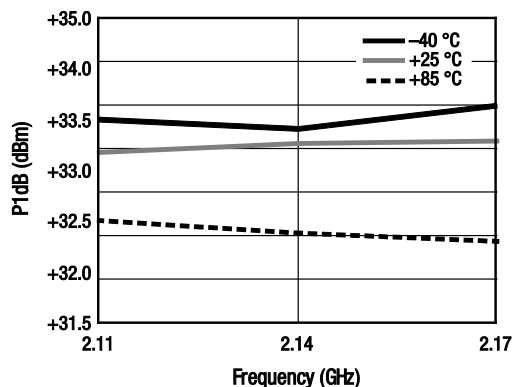


Figure 18. P1dB vs Frequency Over Temperature

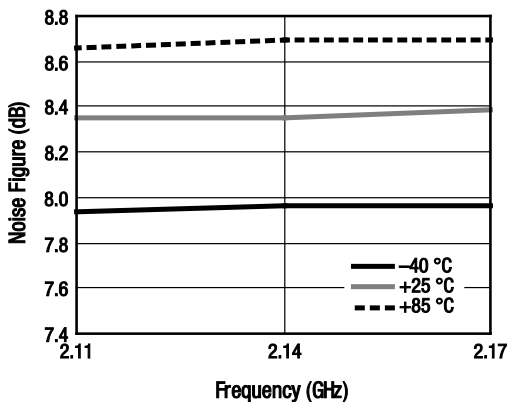


Figure 19. Noise Figure vs Frequency Over Temperature

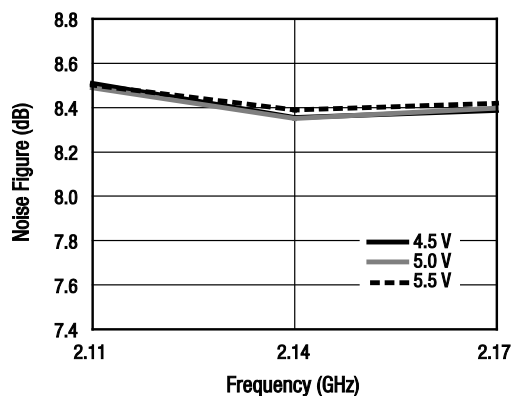


Figure 20. Noise Figure vs Frequency Over Voltage

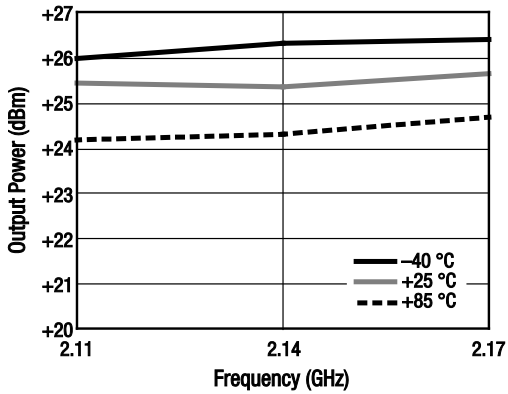


Figure 21. Output Power @ ACLR = -45 dBc vs Frequency Over Temperature

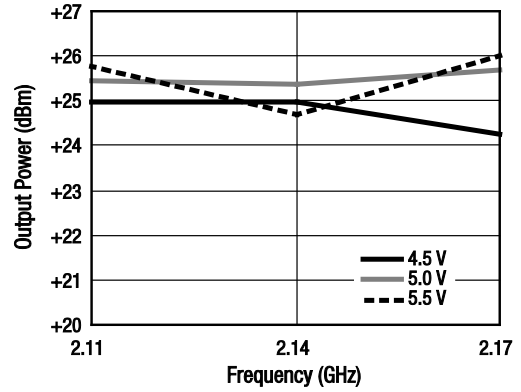


Figure 22. Output Power @ ACLR = -45 dBc vs Frequency Over Voltage

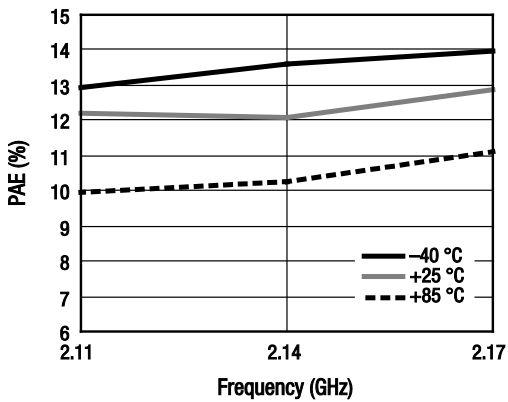


Figure 23. PAE @ ACLR = -45 dBc vs Frequency Over Temperature

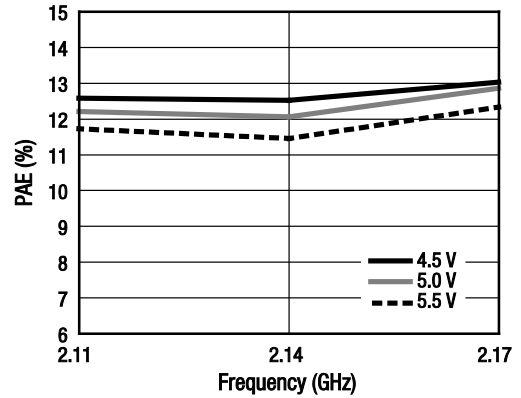


Figure 24. PAE @ ACLR = -45 dBc vs Frequency Over Voltage

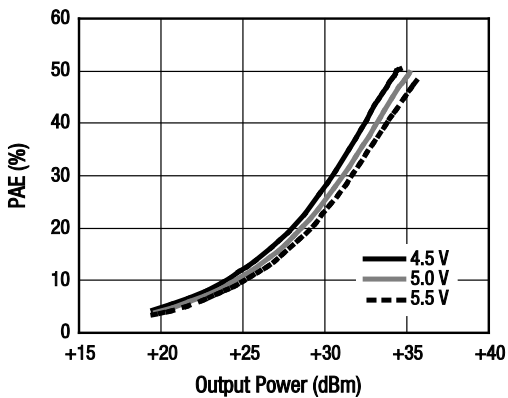


Figure 25. PAE vs Output Power Over Voltage

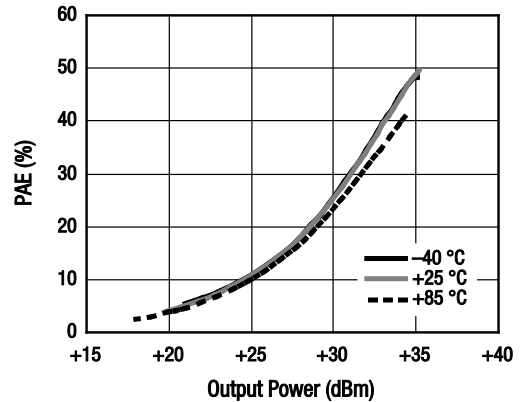


Figure 26. PAE vs Output Power Over Temperature

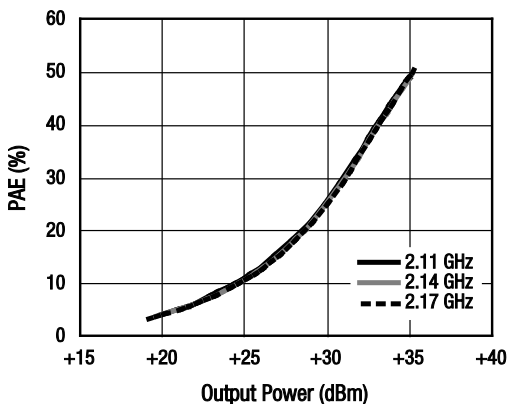


Figure 27. PAE vs Output Power Over Frequency

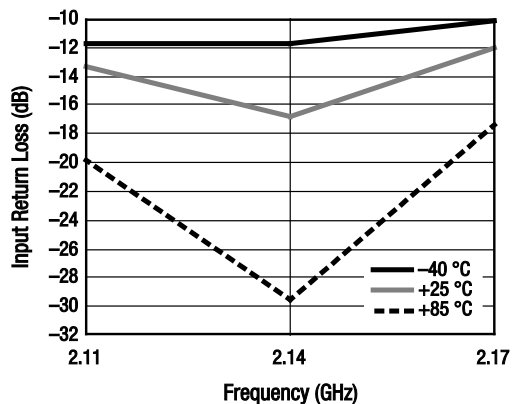


Figure 28. Input Return Loss vs Frequency Over Temperature

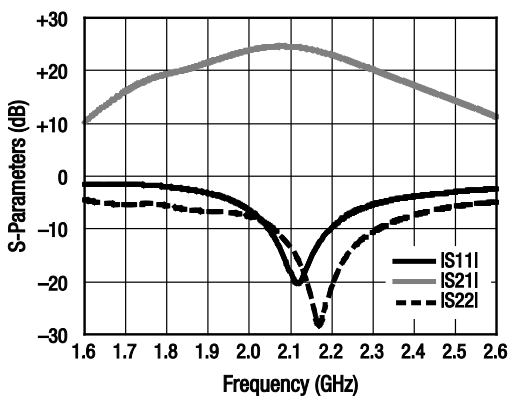


Figure 29. S-Parameters vs Frequency

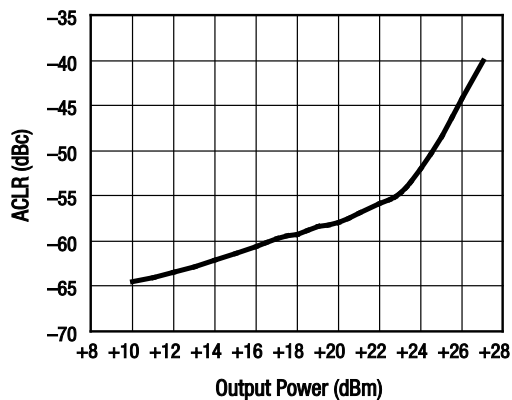


Figure 30. ACLR vs Output Power
(WCDMA 3GPP, 64 DPCH, $f = 2140$ MHz)

Evaluation Board Description

The SKY65120-21 Evaluation Board is used to test the performance of the SKY65120-21 PA. An Evaluation Board schematic diagram is provided in Figure 31. Table 5 provides the Bill of Materials (BOM) list for Evaluation Board components.

An assembly drawing for the Evaluation Board is shown in Figure 32. An Evaluation Board layer detail drawing is shown in Figure 33. Layer detail physical characteristics are noted in Figure 34.

Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

1. Paths to ground should be made as short as possible.
2. The ground pad of the SKY65120-21 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Since the circuit board acts as the heat sink, it must shunt as much heat as possible from the device. Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board. Multiple vias to the grounding layer are required.

NOTE: A poor connection between the slug and ground increases junction temperature (T_J), which reduces the lifetime of the device.

Evaluation Board Test Procedure

- Step 1: Connect RF test equipment to the input/output SMA connectors.
- Step 2: Connect DC ground.
- Step 3: Connect all VDD, VREG, and VC_BIAS lines to a +5 V supply. Verify that the I_{CCQ} current is approximately 447 mA.
- Step 4: Apply RF signal data at -20 dBm and observe that the output level is approximately +4.6 dBm or that the gain of the device is approximately 24.6 dB.

NOTE: It is important to adjust the VCC1 and VCC2 voltage sources so that +5 V is measured at the board. High collector currents drop the collector voltage significantly if long leads are used. Adjust the bias voltage to compensate.

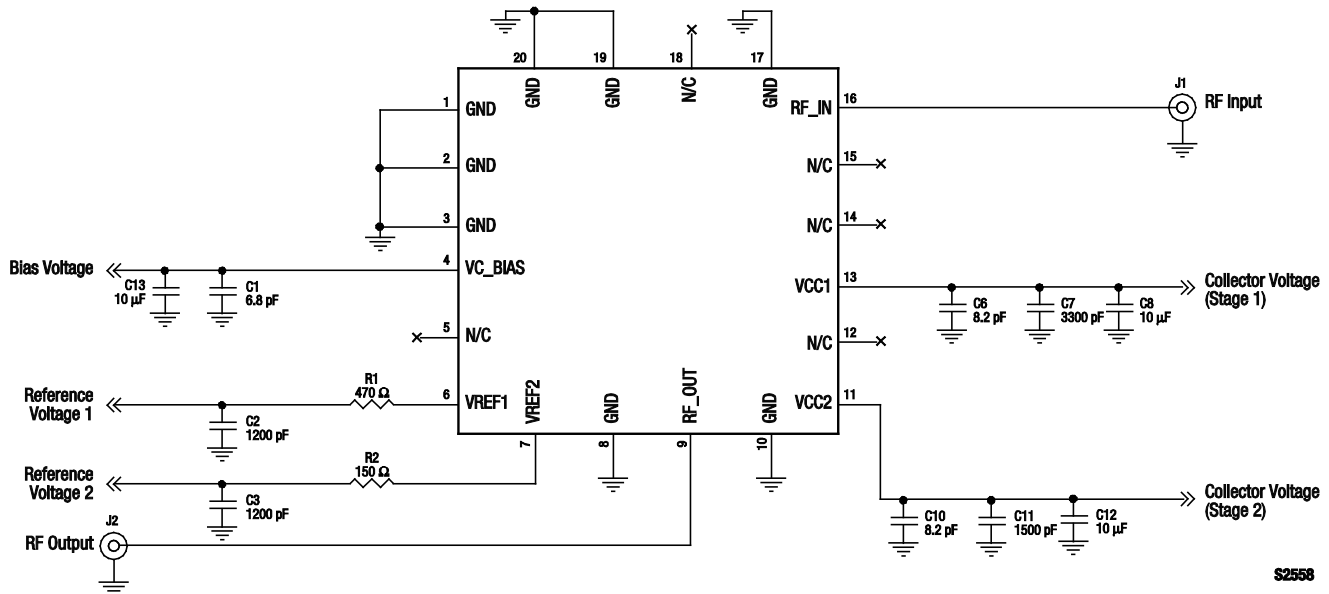
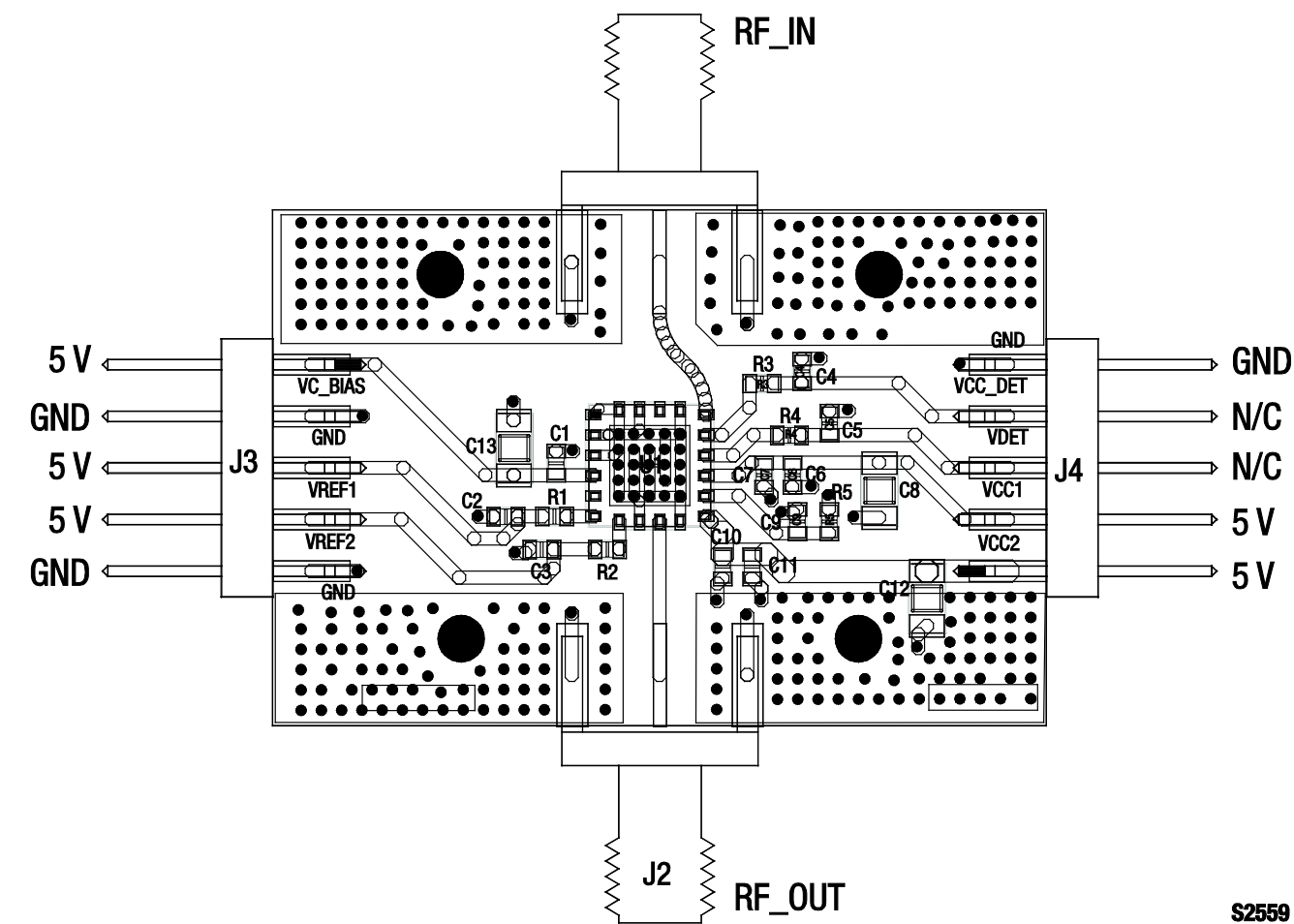


Figure 31. SKY65120-21 Evaluation Board Schematic

Table 5. SKY65120-21 Evaluation Board Bill of Materials (BOM)

Component	Value	Size	Product #	Manufacturer	Manufacturer's Part #	Characteristics
C1	6.8 pF	0603	5404R23-045	Murata	GRM1885C1H6R8CD01J	COG, 50 V, ±0.25 pF
C2, C3	1200 pF	0603	SK204-000-002	Murata	GRM1887U1H122J	U2J, 50 V, ±5 %
C6, C10	8.2 pF	0603	5404R23-046	Murata	GRM1885C1H6R8CZ01D	COG, 50 V, ±0.25 pF
C7	3300 pF	0603	5404R28-015	Murata	GRM188R71H332KD01J	X7R, 50 V, ±10 %
C8, C12, C13	10 µF	1206	5404R91-005	TDK	C3216X5R0J106KT	X5R, 6 V, ±10 %
C11	1500 pF	0603	5404R24-015	AVX	06031C152MATMA	X7R, 100 V, ±20 %
R1	470 Ω	0603	5424R20-041	Rohm	MCR03EZHUJ470	50 V, 0.063 W, ±5 %
R2	150 Ω	0603	5424R19-114	Rohm	MCR03EZHUJ150	50 V, 0.063 W, ±1 %

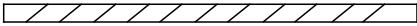



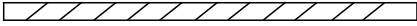

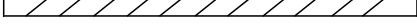


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Figure 32. Evaluation Board Assembly Drawing

*** TBD ***

Figure 33. Evaluation Board Layer Detail

Cross Section	Name	Thickness (mils)	Material	ϵ_r
	L1	1.4	Cu, 1 oz.	—
	Lam1	12	Rogers 4003-12	3.38
	L2	1.4	Cu, 1 oz.	—
	Lam2	4	FR4-4	4.35
	L3	1.4	Cu, 1 oz.	—
	Lam3	12	FR4-12	4.35
	L4	1.4	Cu, 1 oz.	—

8573

Figure 34. Layer Detail Physical Characteristics

Application Circuit Notes

Center Ground. It is extremely important to sufficiently ground the bottom ground pad of the device for both thermal and stability reasons. Multiple small vias are acceptable and will work well under the device if solder migration is an issue.

GND (pins 1, 2, 3, 8, 10, 17, 19, and 20). Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via that the layout allows. Multiple small vias are acceptable and will work well under the device if solder migration is an issue.

N/C (pins 5, 12, 14, 15, and 18). These pins are open and may or may not be connected to ground.

VC_BIAS (pin 4). The bias supply voltage for stages 1 and 2, typically set to +5 V.

VREF1 (pin 6). Bias reference voltage for amplifier stage 1. This signal should be operated over the same voltage range as VCC with a nominal voltage of +5 V.

VREF2 (pin 7). Bias reference voltage for amplifier stage 2. This signal should be operated over the same voltage range as VCC with a nominal voltage of +5 V.

RF_OUT (pin 9). Amplifier RF output pin ($Z_0 = 50 \Omega$). The module includes an onboard internal DC blocking capacitor. All impedance matching is provided internal to the module.

VCC2 (pin 11). Supply voltage for the output (final) stage collector bias (typically +5 V). To bypass VCC2, capacitors C10, C11, and C12 (see Figure 31) should be placed in the approximate location shown on the Evaluation Board, although exact placement is not critical.

VCC1 (pin 13). Supply voltage for the first stage collector bias (typically +5 V). To bypass VCC1, capacitors C6, C7, and C8 (see

Figure 31) should be placed in the approximate location shown on the Evaluation Board, although exact placement is not critical.

RF_IN (pin 16). Amplifier RF input pin ($Z_0 = 50 \Omega$). The module includes an onboard internal DC blocking capacitor. All impedance matching is provided internal to the module.

Package Dimensions

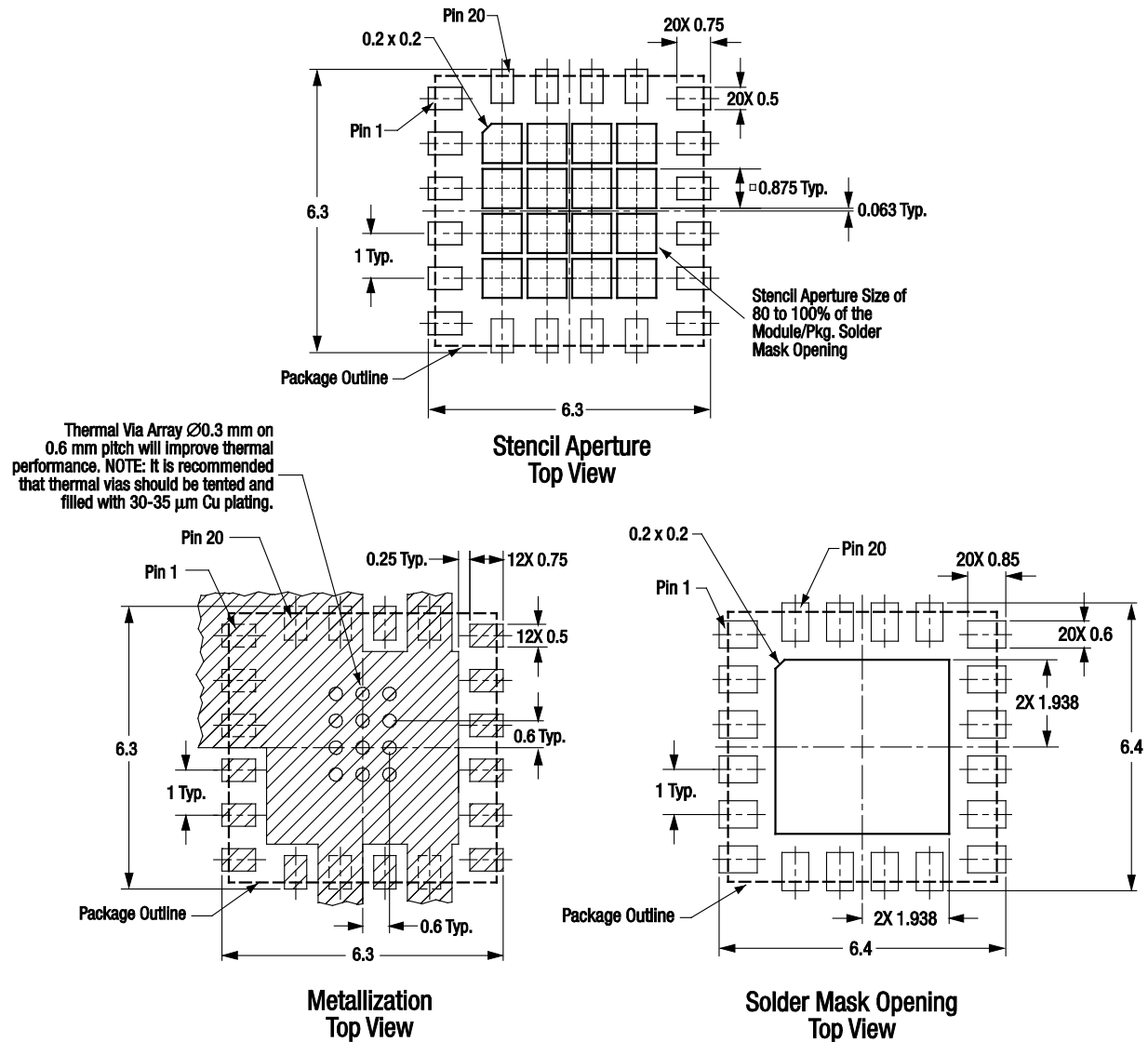
The PCB layout footprint for the SKY65152-11 is shown in Figure 35. Typical case markings are shown in Figure 36. Package dimensions for the 20-pin MCM are shown in Figure 37, and tape and reel dimensions are provided in Figure 38.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY65120-21 is rated to Moisture Sensitivity Level 3 (MSL3) at 250 °C. It can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, *PCB Design and SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.



All dimensions are in millimeters

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Figure 35. SKY65120-21 PCB Layout Footprint

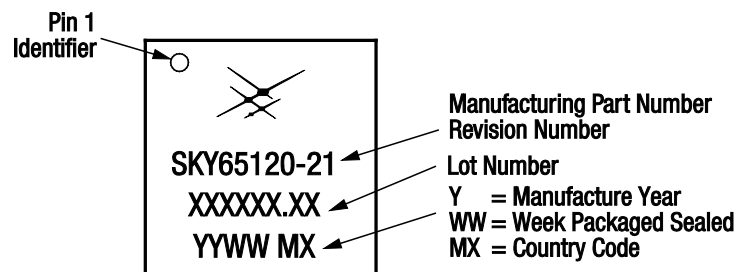


Figure 36. SKY65120-21 Typical Case Markings

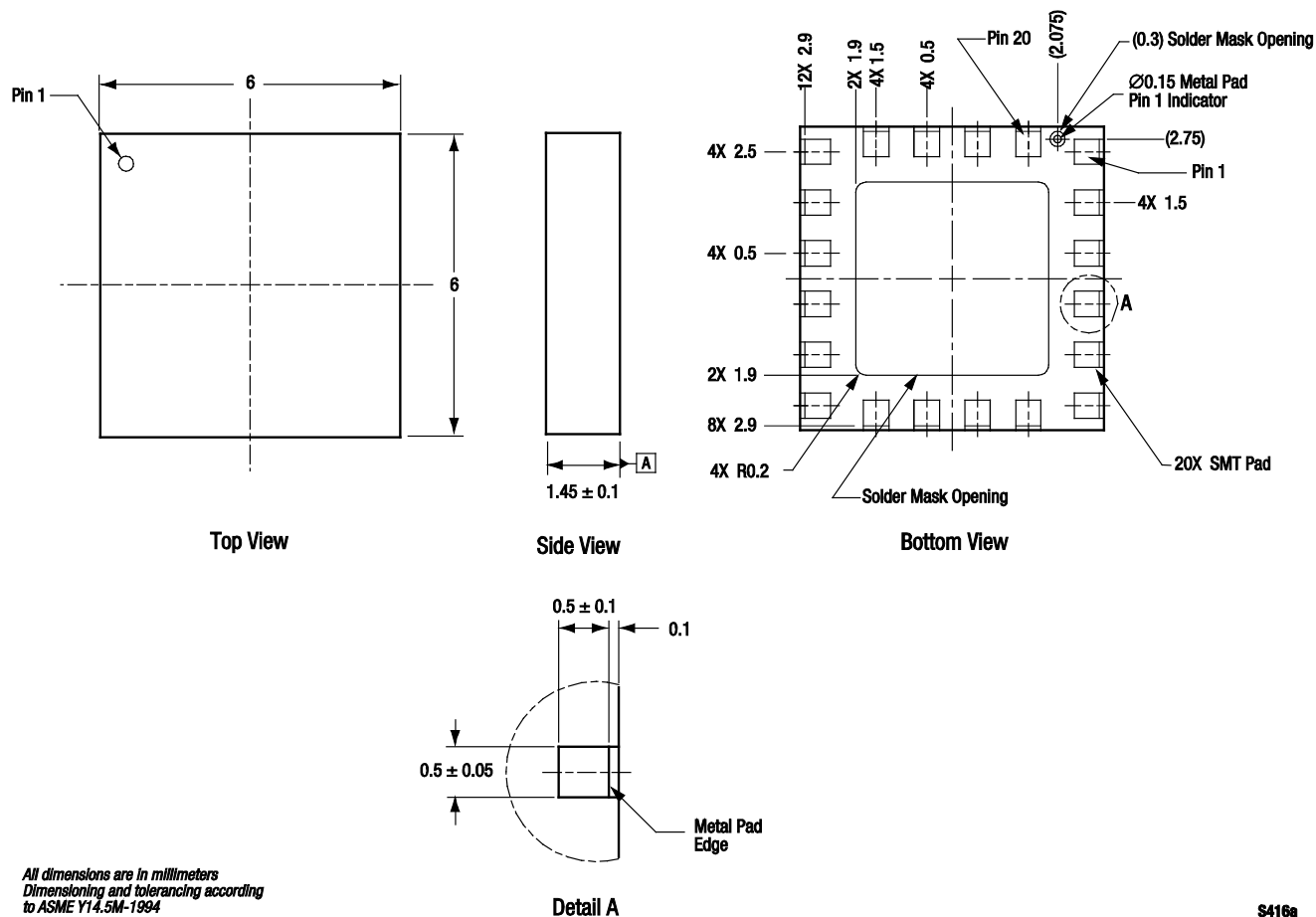
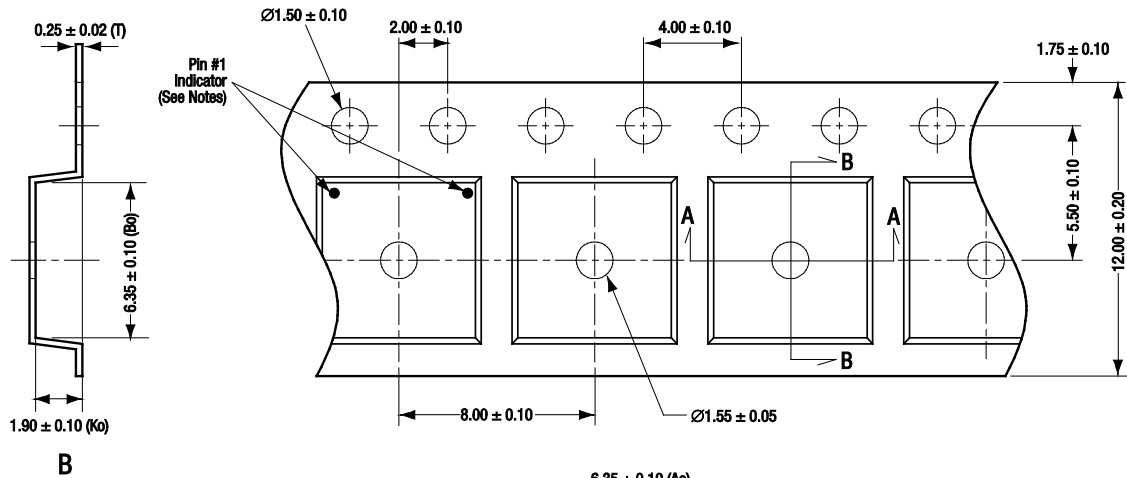


Figure 37. SKY65120-21 20-Pin MCM Package Dimensions



Notes:

1. Carrier tape: black conductive polystyrene
2. Cover tape material: transparent conductive PSA
3. Cover tape size: 9.3 mm width
4. All dimensions are in millimeters
5. Ao and Bo measurement point is 0.3 mm from bottom pocket
5. Pin 1 orientation is in top left corner for the following Skyworks products:

SKY65205-11

SKY65208-11

SKY65215-11

For all other 6 x 6 mm MCM/RFLGA products, pin 1 orientation is in top right corner.

\$1786

Figure 38. SKY65120-21 20-Pin MCM Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY65120-21 Power Amplifier	SKY65120-21	TW16-D190-001

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