

LTM8001

36V_{IN}, 5A μ Module Regulator with 5-Output Configurable LDO Array

DESCRIPTION

Demo circuit 1818A features the LTM8001 μ Module regulator that includes a 5A switching regulator and an array of five 1.1A low noise LDOs. DC1818A is configured so the switching regulator provides an output that also powers the LDOs. The LDOs in turn provide three outputs – one from a single LDO and two outputs each formed by paralleling two LDOs together.

DC1818A supports changes to the LTM8001's user adjustable features including the output voltage of the switching regulator, output voltage of each of the five LDOs, switching frequency, soft-start period and output current limit of the

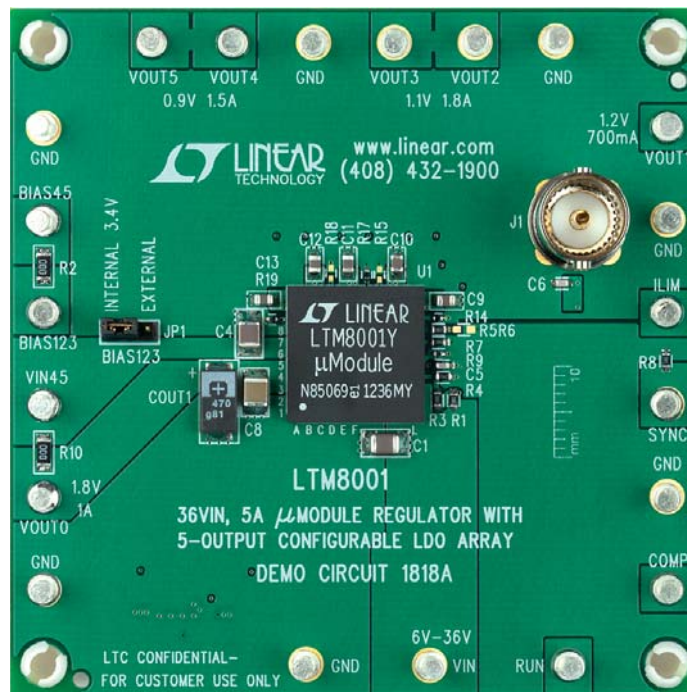
switching regulator simply by modifying the appropriate resistors or capacitor. DC1818A also supports all current sharing or independent operation options of the LDOs. DC1818A includes a BNC connector for noise measurement of the LDO for V_{OUT1}. An optional capacitor at C14 further reduces output noise.

The LTM8001 data sheet must be read in conjunction with this demo manual to properly use or modify DC1818A.

Design files for this circuit board are available at <http://www.linear.com/demo>

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BOARD PHOTO



PERFORMANCE SUMMARY

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Input Voltage, V_{IN}				6	V
Maximum Input Voltage, V_{IN}		36			V
Regulator Output Voltage, V_{OUT0}	$I_{OUT0} \leq 5A$, $I_{OUT1-5} = 0A$, $R9 = 19.6k$	1.72		1.84	V
Maximum Regulator Output Current, I_{OUT0}	$I_{LIM} = V_{REF}$, $I_{OUT1-5} = 0A$	5			A
LDO1 Output Voltage, V_{OUT1}	$1mA \leq I_{OUT1} \leq 700mA$, $R14 = 121k$	1.16		1.25	V
LDO2,3 Output Voltage, $V_{OUT2,3}$	$V_{OUT2} = V_{OUT3}$, $SET2 = SET3$, $2mA \leq I_{OUT2,3} \leq 1.8A$, $R17 = 54.9k$	1.04		1.13	V
LDO4,5 Output Voltage, $V_{OUT4,5}$	$V_{OUT4} = V_{OUT5}$, $SET4 = SET5$, $2mA \leq I_{OUT4,5} \leq 1.5A$, $R19 = 45.3k$	0.86		0.94	V
V_{OUT0} Efficiency	$V_{IN} = 12V$, $I_{OUT0} = 2.5A$, $I_{OUT1-5} = 0A$		84		%
Switching Frequency	$R7 = 118k$		350		kHz

QUICK START PROCEDURE

Demo circuit 1818A is an easy way to evaluate the performance of the LTM8001. Refer to Figure 1 for the proper measurement equipment setup and follow the procedure below:

NOTE: Do not hot-plug the V_{IN} terminal at high input voltages. The absolute maximum voltage on V_{IN} is 40V and hot-plugging a power supply through wire leads to the demonstration circuit can cause the voltage on the extremely low ESR ceramic input capacitor to ring to twice its DC value. In order to protect the LTM8001, an aluminum electrolytic capacitor with higher ESR is placed at the input terminals. This may protect against some, but not all, input transients due to a hot-plugged power supply. See Application Note 88 for more details.

1. Place JP1 for BIAS123 in the INTERNAL 3.4V position.

NOTE: DC1818A includes an LTM8020 regulator to provide 3.4V bias voltages to the LDOs. The 3.4V bias supply can be disconnected using jumper JP1 to allow an external bias supply.

2. Connect the power supply (with power off), loads, and meters as shown in Figure 1.
3. After all connections are made, turn on the input power and verify that V_{OUT0} is 1.8V and the output voltages for V_{OUT1} , $V_{OUT2,3}$, and $V_{OUT4,5}$ are 1.2V, 1.1V, and 0.9V respectively.

NOTE: If V_{OUT0} is too low, temporarily disconnect the loads to make sure that the loads are not set too high. If V_{OUT1} , $V_{OUT2,3}$ or $V_{OUT4,5}$ is too high, make sure the outputs are loaded by at least the LDO minimum load current of 1mA, 2mA and 2mA respectively.

4. Once the proper output voltages are established, adjust each load within its operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters.

QUICK START PROCEDURE

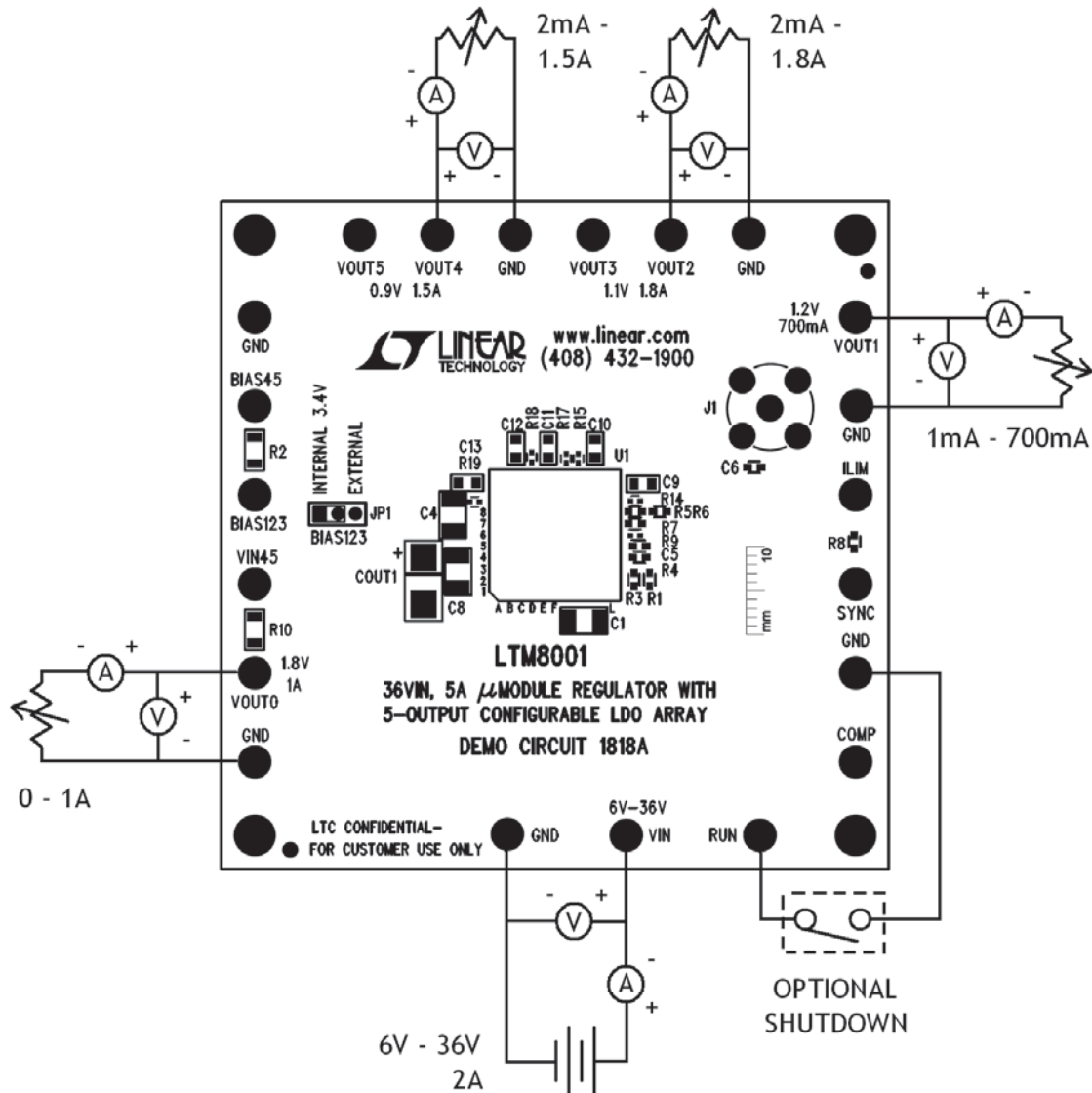


Figure 1. Proper Measurement Equipment Setup

QUICK START PROCEDURE

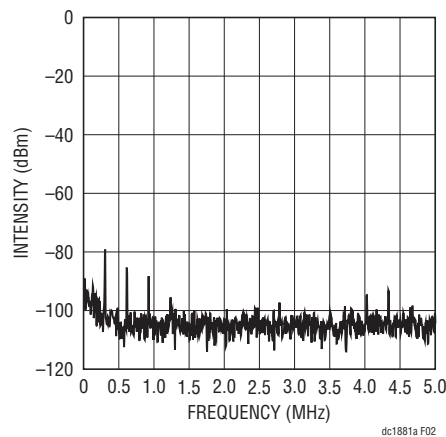


Figure 2. V_{OUT1} Noise Spectrum (V_{OUT1} = 1.2V at 700mA, C_{OUT1} = 22 μ F, C_{SET1} = 1nF, V_{IN} = 12V, V_{OUT0} = 1.8V Loaded to a Total Current of 5A)

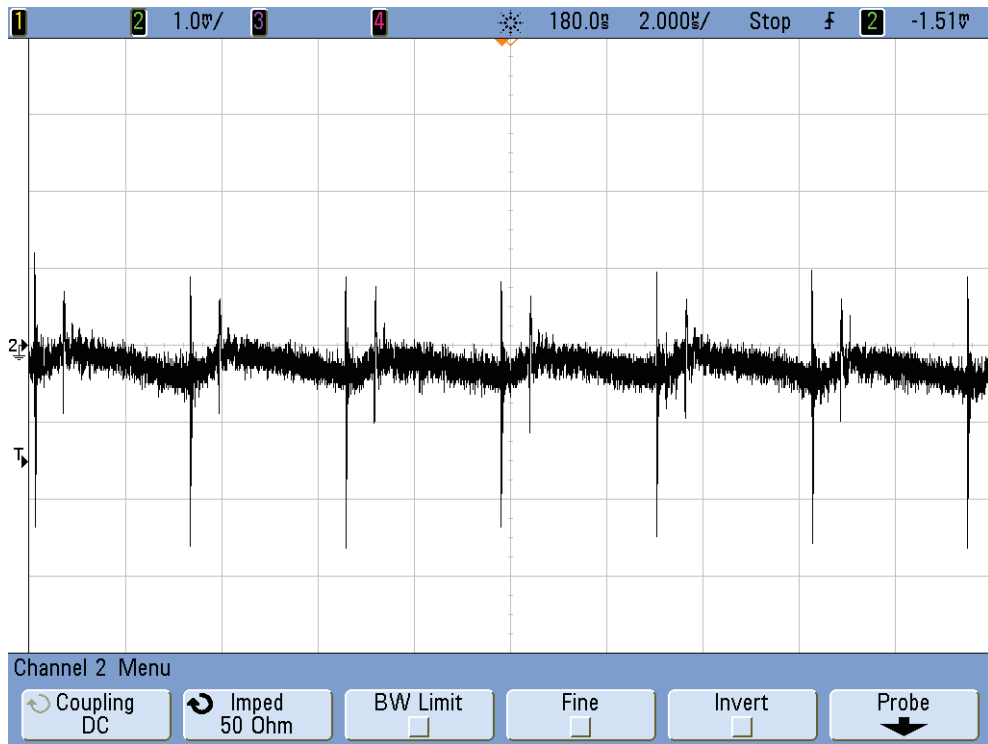
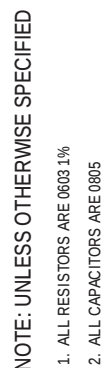


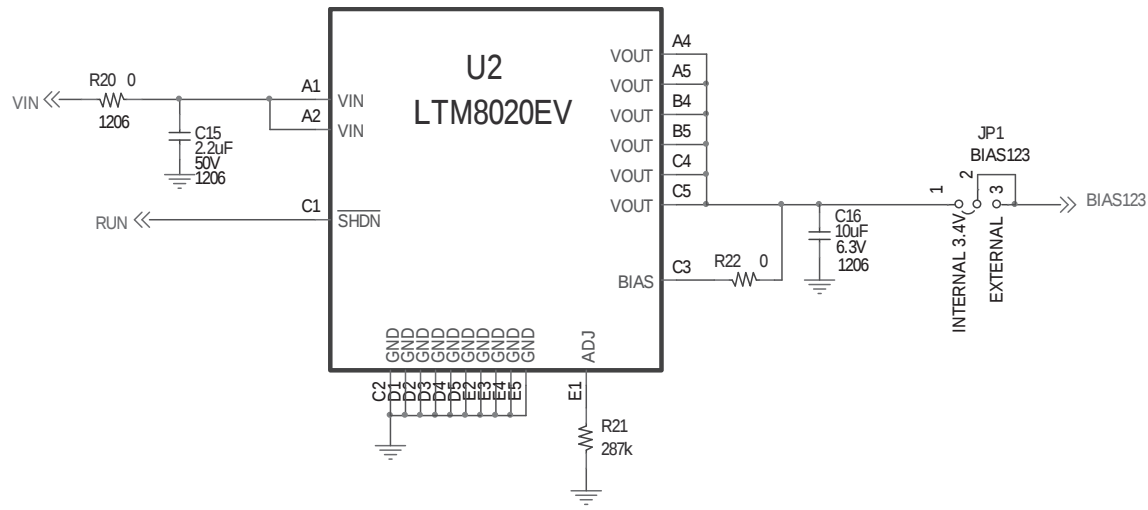
Figure 3. V_{OUT1} Ripple (V_{OUT1} = 1.2V at 700mA, C_{OUT1} = 22 μ F, C_{SET1} = 1nF, V_{IN} = 12V, V_{OUT0} = 1.8V Loaded to a Total Current of 5A, 100MHz BW)

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	COUT1	CAP., POSCAP, 470µF, 4V, D3L	SANYO, 4TPE470ML
2	1	C1	Cap., X5R, 10µF, 50V, 20% 1210	TAIYO YUDEN, UMK325BJ106M
3	1	C5	Cap., X7R, 1000pF, 50V, 20% 0603	AVX, 06035C102MAT2A
4	1	C8	Cap., X5R, 100µF, 6.3V, 20%, 1210	TAIYO YUDEN, JMK325ABJ107MM-T
5	5	C9-C13	Cap., X5R, 2.2µF, 10V, 10%, 0805	TAIYO YUDEN, LMK212BJ225KG-T
6	1	R7	RES., CHIP, 118k, 1%, 0603	VISHAY, CRCW0603118KFKEA
7	1	R9	RES., CHIP, 19.6k, 1%, 0402	VISHAY, CRCW040219K6FKED
8	1	R14	RES., CHIP, 121k, 1%, 0402	VISHAY, CRCW0402121KFKEA
9	1	R17	RES., CHIP, 54.9k, 1%, 0402	VISHAY, CRCW040254K9FKED
10	1	R19	RES., CHIP, 45.3k, 1%, 0402	VISHAY, CRCW040245K3FKED
11	1	U1	IC, LTM8001EY, BGA, 15mmX15mmX3.42mm	LINEAR TECH. LTM8001EY
Additional Demo Board Circuit Components				
1	0	CIN1	CAP., ALUM, 100µF, 50V	SUN ELECT, 50CE100LX
2	0	C2, C3	Cap., X5R, 1µF, 10V, 20% 0603	TAIYO YUDEN, LMK107BJ105MA-T
3	0	C4	Cap., X5R, 10µF, 50V, 20% 1210	TAIYO YUDEN, UMK325BJ106M
4	0	C6	Cap., X7R, 100pF, 25V, 10%, 0603	AVX, 06033C101KAT2A
5	0	C14	Cap., 0603	
6	0	C15	Cap., X5R, 2.2µF, 50V, 20%, 1206	TAIYO YUDEN, UMK316BJ225MD-T
7	0	C16	Cap., X5R, 10µF, 6.3V, 10%, 1206	TAIYO YUDEN, JMK316BJ106KL-T
8	0	R1	RES., CHIP, 121k, 1%, 0603	VISHAY, CRCW0603121KFKEA
9	0	R2, R10, R20	RES., CHIP, 0Ω, 1206	VISHAY, CRCW12060000Z0EA
10	0	R3	RES., CHIP, 107k, 1%, 0603	VISHAY, CRCW0603107KFKEA
11	0	R4	RES., CHIP, 174k, 1%, 0603	VISHAY, CRCW0603174KFKEA
12	0	R5	RES., CHIP, 100k, 5%, 0603	VISHAY, CRCW0603100KJNEA
13	0	R6, R11, R13	RES., CHIP, 0603	
14	0	R8, R12, R16, R22	RES., CHIP, 0Ω, 0603	VISHAY, CRCW06030000Z0EA
15	0	R15, R18	RES., CHIP, 0402	
16	0	R21	RES., CHIP, 287k, 1%, 0603	VISHAY, CRCW0603287KFKEA
17	0	U2	IC, LTM8020EV, LGA, 6.25mmx6.25x2.32mm	LINEAR TECH. LTM8020EV
Hardware: For Demo Board Only				
1	21	E1-E21	TESTPOINT, TURRET, 0.095"	MILL-MAX, 2501-2-00-80-00-00-07-0
2	1	JP1	Header, 3 Pins 2mm Ctrs.	SAMTEC, TMM-103-02-L-S
3	1	JP1	SHUNT	SAMTEC, 2SN-BK-G
4	1	J1	CONN, BNC, 5 PINS	CONNEX, 112404
5	4	MH1-MH4	STAND-OFF, NYLON 0.5" Tall	KEYSTONE, 8833 (SNAP ON)



SCHEMATIC DIAGRAM



DEMO MANUAL DC1818A

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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