

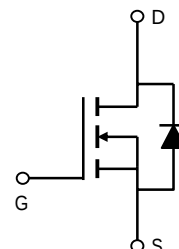
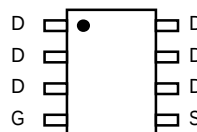
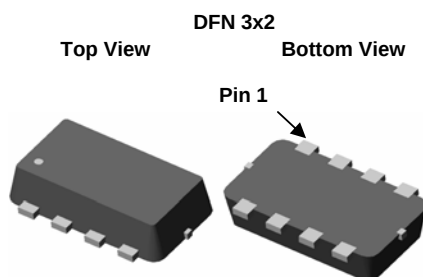
AON4420L
N-Channel Enhancement Mode Field Effect Transistor
General Description

The AON4420L combines advanced trench MOSFET technology with a small footprint package to provide low $R_{DS(ON)}$ per unit area. This device is ideal for load switch and high speed switching applications.

- RoHS Compliant
- Halogen Free

Features

$V_{DS} (V) = 30V$
 $I_D = 10A$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 19m\Omega$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 25m\Omega$ ($V_{GS} = 4.5V$)


Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Pulsed Drain Current ^C	I_{DM}	50	
Continuous Drain Current ^A	$T_A=25^\circ C$	10	A
	$T_A=70^\circ C$	8	
Power Dissipation ^A	$T_A=25^\circ C$	1.6	W
	$T_A=70^\circ C$	1	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	34	40	$^\circ C/W$
Maximum Junction-to-Ambient ^A		66	80	$^\circ C/W$
Maximum Junction-to-Lead ^B	$R_{\theta JL}$	20	25	$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D = 250μA, V _{GS} = 0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 30V, V _{GS} = 0V T _J = 55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1.4	1.9	2.5	V
I _{D(ON)}	On state drain current	V _{GS} = 10V, V _{DS} = 5V	50			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 10V, I _D = 10A T _J =125°C		16 27	20	mΩ
		V _{GS} = 4.5V, I _D = 8A		21	26	
g _{FS}	Forward Transconductance	V _{DS} = 5V, I _D = 10A		30		S
V _{SD}	Diode Forward Voltage	I _S = 1A, V _{GS} = 0V		0.75	1	V
I _S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz	440	550	660	pF
C _{oss}	Output Capacitance		80	110	140	pF
C _{rss}	Reverse Transfer Capacitance		35	55	80	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	2	4	6	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge (10V)	V _{GS} =10V, V _{DS} =15V, I _D =10A	8	9.8	12	nC
Q _g (4.5V)	Total Gate Charge (4.5V)		4	4.6	5.5	nC
Q _{gs}	Gate Source Charge		1.5	1.8	2.2	nC
Q _{gd}	Gate Drain Charge		1.3	2.2	3	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =1.5Ω, R _{GEN} =3Ω		5		ns
t _r	Turn-On Rise Time			3.2		ns
t _{D(off)}	Turn-Off DelayTime			24		ns
t _f	Turn-Off Fall Time			6		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =10A, dI/dt=300A/μs	8	11	14	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =10A, dI/dt=300A/μs	11	13	16	nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using t ≤ 300μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F: The current rating is based on the t ≤ 10s thermal resistance rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

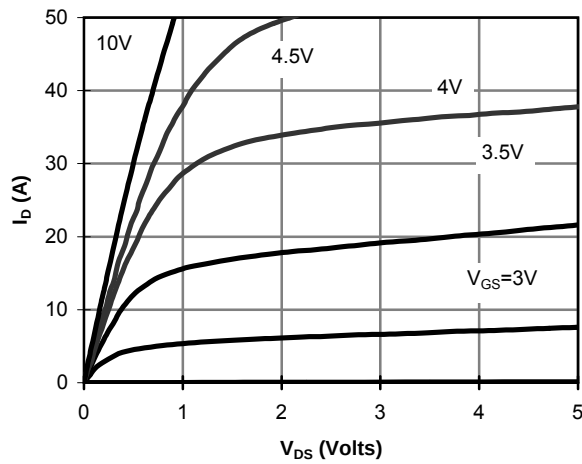


Figure 1: On-Region Characteristics

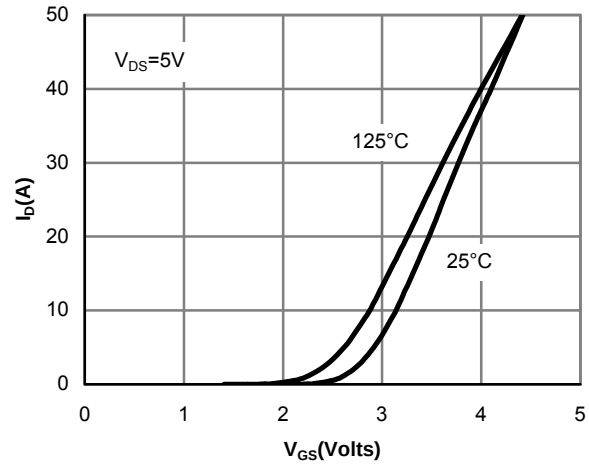


Figure 2: Transfer Characteristics

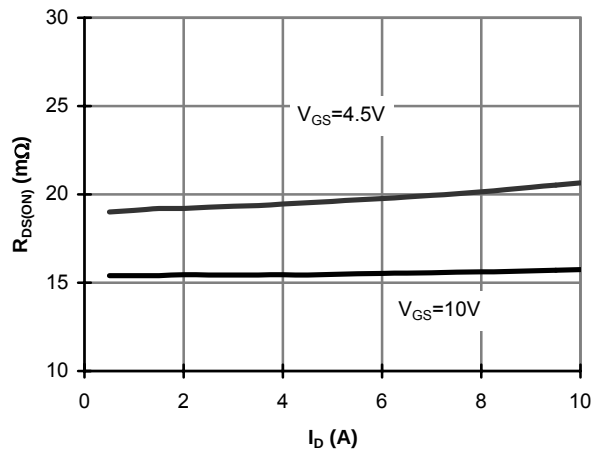


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

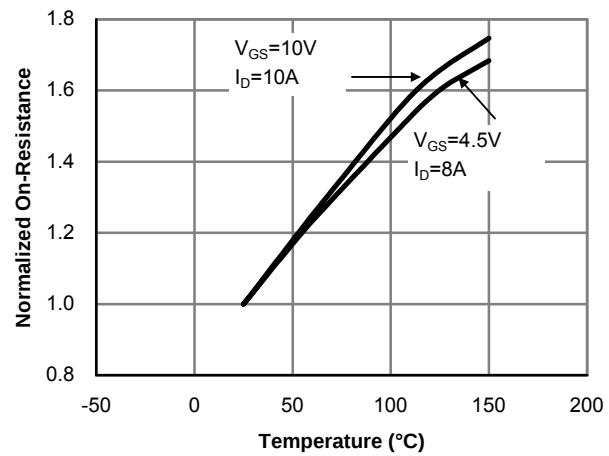


Figure 4: On-Resistance vs. Junction Temperature

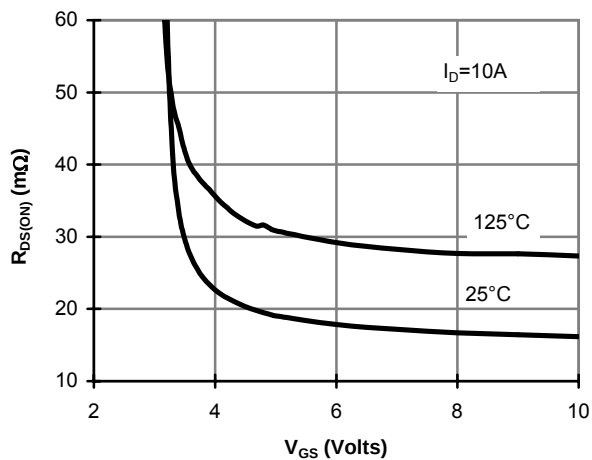


Figure 5: On-Resistance vs. Gate-Source Voltage

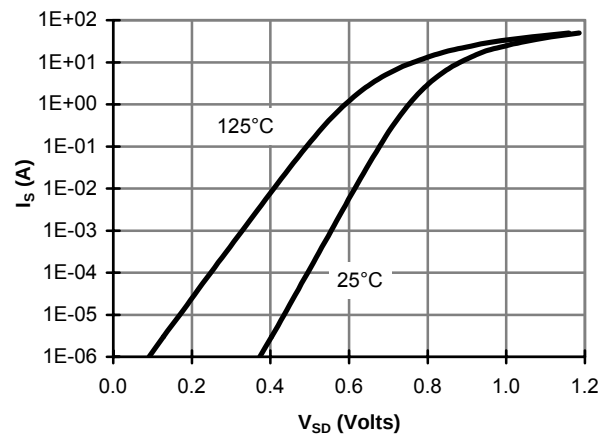


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

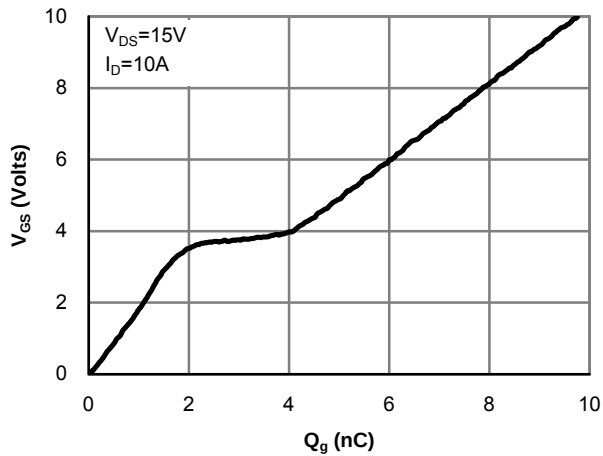


Figure 7: Gate-Charge Characteristics

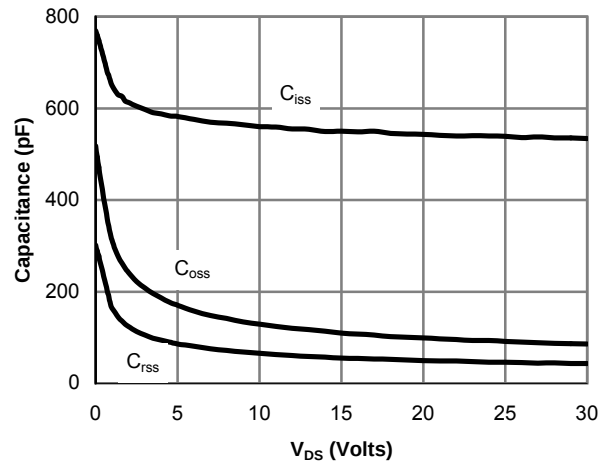


Figure 8: Capacitance Characteristics

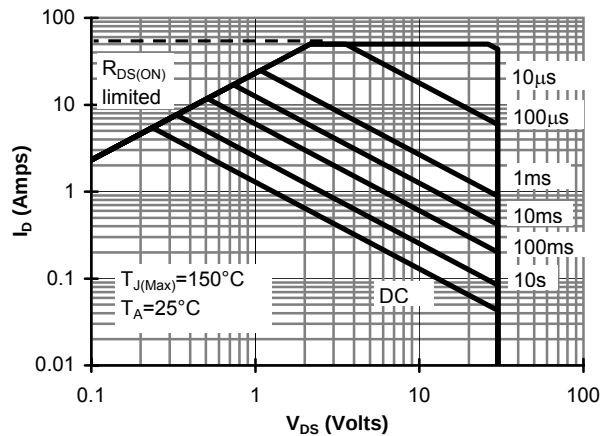


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

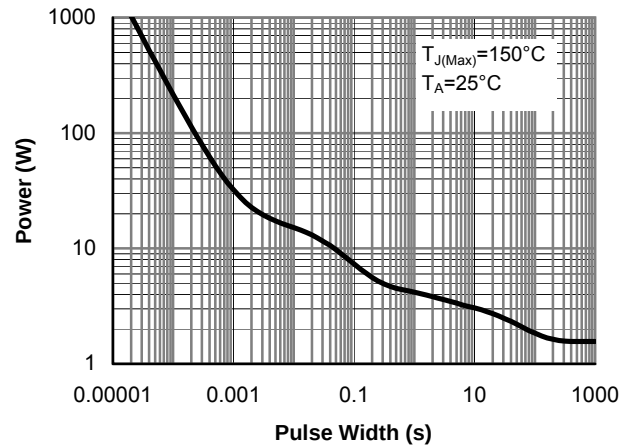


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

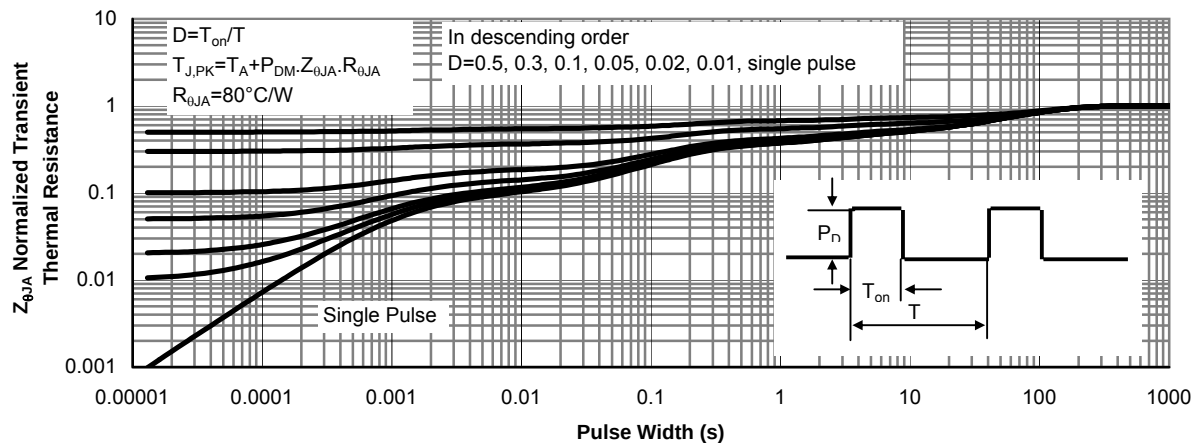
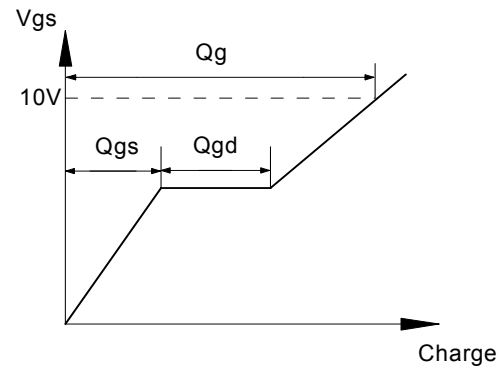
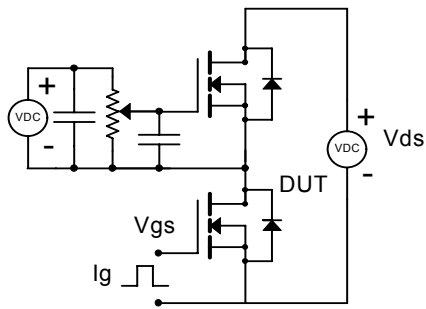
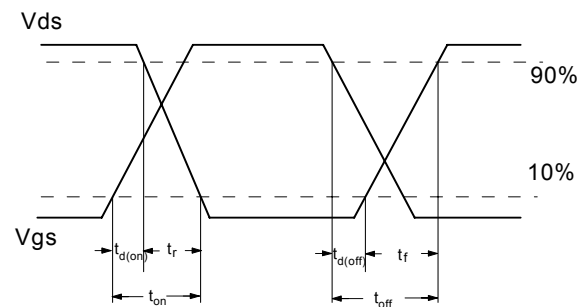
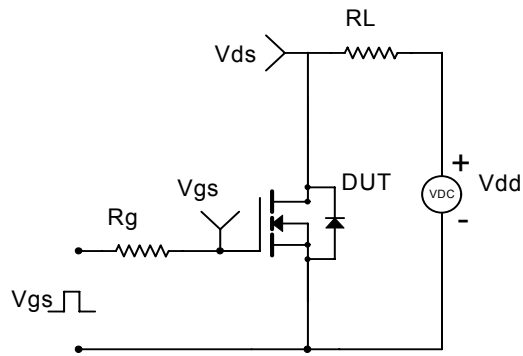


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

