0.13 g (typ.)

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# **TC4094BFN**

### TC4094B 8-Stage Shift-and-Store Bus-Register

TC4094B is a SHIFT and STORE REGISTER that consists of an 8-bit shift register and an 8-bit latch. The read data in the shift register can be taken in the latch through the asynchronous STROBE input; therefore, the data transfer mode can hold output. And, since the parallel outputs is of 3-state construction, it can be directly connected to the 8-bit busline.

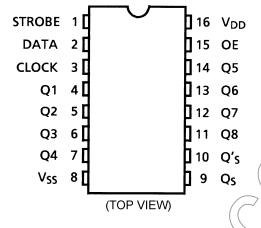
This register can be applied to Serial-to-parallel conversion, data receivers, etc.

# Note: xxxFN (JEDEC SOP) is not available in Japan. TC4094BFN SOL16-P-150-1.27

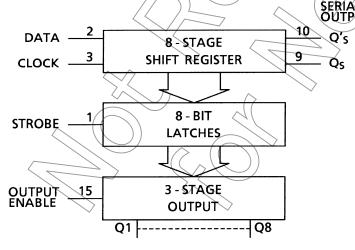
)Weight

SOL16-P-150-1.27

## Pin Assignment



### **Block Diagram**



PARALLEL OUTPUTS

2012-02-29

### **Truth Table**

CL	OE	ST	D		PO	SO		
CL	Ŏ.	5	D	Q1	Qn	Qs	Q's	
	Н	Н	L	L	Qn – 1	Q7	NC	
	Η	Η	Н	Н	Qn – 1	Q7	NC	
	Η	L	Х	NC	NC	Q7	NC	
	L	X	Х	HZ	HZ	Q7	NC	
$\Box$	Н	Χ	Х	NC	NC	NC	Qs	
$\supset$	L	Х	Х	HZ	HZ	NC	Qs	

CL = Clock X = Don't care

OE = Output eneble NC = No change

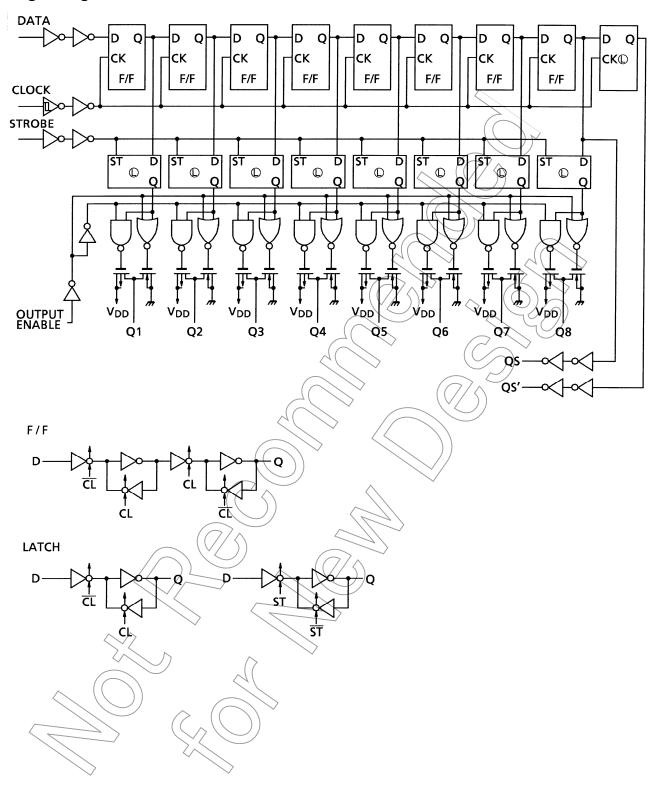
ST = Strobe HZ = High impedance

 $\mathsf{D} = \mathsf{Data}$ 

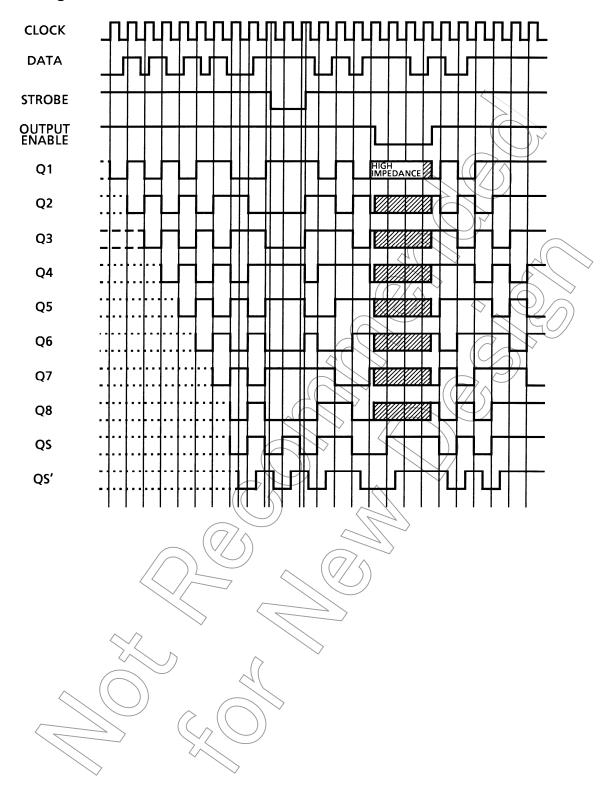
PO = Parallel outputs

SO = Serial outputs

### **Logic Diagram**



### **Timing Chart**



### **Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Rating	Unit
DC supply voltage	$V_{DD}$	$V_{SS}$ – 0.5 to $V_{SS}$ + 20	V
Input voltage	V <sub>IN</sub>	V <sub>SS</sub> – 0.5 to V <sub>DD</sub> + 0.5	V
Output voltage	V <sub>OUT</sub>	V <sub>SS</sub> – 0.5 to V <sub>DD</sub> + 0.5	< ∨
DC input current	I <sub>IN</sub>	±10	mA
Power dissipation	PD	180	MW
Operating temperature range	T <sub>opr</sub>	-40 to 85	ိုင္ပံ
Storage temperature range	T <sub>stg</sub>	-65 to 150	∕}¢

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

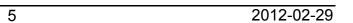
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

### Operating Ranges (V<sub>SS</sub> = 0 V) (Note)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
DC supply voltage	V <sub>DD</sub>	$\langle \langle \rangle \rangle$	3	_	18	V
Input voltage	VIN	-\//	0	_	$V_{DD}$	V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V<sub>DD</sub> or V<sub>SS</sub>.



# Static Electrical Characteristics ( $V_{SS} = 0 V$ )

01		Sym-	Test Condition		-40	)°C		25°C		85	°C				
Charac	teristics	bol		V <sub>DD</sub> (V)	Min	Max	Min	Тур.	Max	Min	Max	Unit			
						I <sub>OUT</sub>  < 1 μA	5	4.95	_	4.95	5.00	_	4.95	_	
High-level output voltage	$V_{OH}$		10	9.95	_	9.95	10.00∠	_	9.95	_	V				
9			$V_{IN} = V_{SS}, V_{DD}$	15	14.95	_	14.95	15.00		14.95	_				
			  I <sub>OUT</sub>   < 1 μA	5	_	0.05	_	0.00	0.05	\r	0.05				
Low-level voltage	output	$V_{OL}$	$V_{IN} = V_{SS}, V_{DD}$	10	_	0.05	_	0.00	0.05	/_	0.05	V			
J			VIN - VSS, VDD	15	-	0.05	<b>*</b>	0(00/	0,05	_	0.05				
			V <sub>OH</sub> = 4.6 V	5	-0.61	_	-0.51	_1.0		-0.42	_				
			V <sub>OH</sub> = 2.5 V	5	-2.50	_	-2.10	-4.0 <sub>N</sub>	· —	-1.70	_				
Output hig	h current	I <sub>OH</sub>	V <sub>OH</sub> = 9.5 V	10	-1.50	_	-1.30	-2.2	_	-1.10	_	mA			
			V <sub>OH</sub> = 13.5 V	15	-4.00	- <	3.40	9.0	_	2.80	7				
			$V_{IN} = V_{SS}, V_{DD}$								>				
			V <sub>OL</sub> = 0.4 V	5	0.61	(+//	0.51	1.2	+(	0.42	_	mA			
Output low	current	nt I <sub>OL</sub>	V <sub>OL</sub> = 0.5 V	10	1.50	7	1.30	3.2	4	(1.10)	) —				
Output low	Current		V <sub>OL</sub> = 1.5 V	15	4.00		3.40	12.0	<sub>2</sub>	2.80	_				
			$V_{IN} = V_{SS}, V_{DD}$		4					*					
		V <sub>IH</sub>	V <sub>OUT</sub> = 0.5 V, 4.5 V	5	3.5	>	3.5	2.75		3.5	_	V			
Input high	voltago		V <sub>OUT</sub> = 1.0 V, 9.0 V	10 (	7.0	_	7.0	5.50	) —	7.0	_				
input nign	voitage	VIH	V <sub>OUT</sub> = 1.5 V, 13.5 V <sub>⟨</sub>	J (5	11,0	-//	11.0	8.25	_	11.0	_	V			
			I <sub>OUT</sub>   < 1 μA		>										
			V <sub>OUT</sub> = 0.5 V, 4.5 V	5	_	1.5		2.25	1.5	_	1.5				
Input low v	voltage	V <sub>IL</sub>	V <sub>OUT</sub> = 1.0 V, 9.0 V	_10	_	3.0		4.50	3.0	_	3.0	V			
input low v	ollage	۷IL	$V_{OUT} = 1.5 V, 13.5 V$	15		4.0	_	6.75	4.0	_	4.0	V			
			I <sub>OUT</sub> 1 µA		~	1									
Input	"H" level	IIH	V <sub>IH</sub> = 18/V	18	//	9.1	_	10 <sup>-5</sup>	0.1	_	1.0	μΑ			
current	"L" level	YIL/	V <sub>IL</sub> = 0 V	18	(7)	<b>√</b> –0.1	_	$-10^{-5}$	-0.1	_	-1.0	μΑ			
3-state output	"H" level	TOH.	V <sub>out</sub> = 18 V	18		0.4	_	10 <sup>-4</sup>	0.4	_	12				
leakage current	"L" level	I <sub>DL</sub>	V <sub>out</sub> ≠ 0 V	18	2	-0.4	_	-10 <sup>-4</sup>	-0.4	_	-12	μΑ			
	$\sim$	>	V V V	5	· —	5	_	0.005	5	_	150				
Quiescent current	supply 📐	1DD/	$V_{IN} = V_{SS}, V_{DD}$	10	_	10	_	0.010	10	_	300	μА			
Junon			(Note)	15	_	20	_	0.015	20	_	600				

Note: All valid input combinations.

# Dynamic Electrical Characteristics (Ta = 25°C, $V_{SS}$ = 0 V, $C_L$ = 50 pF)

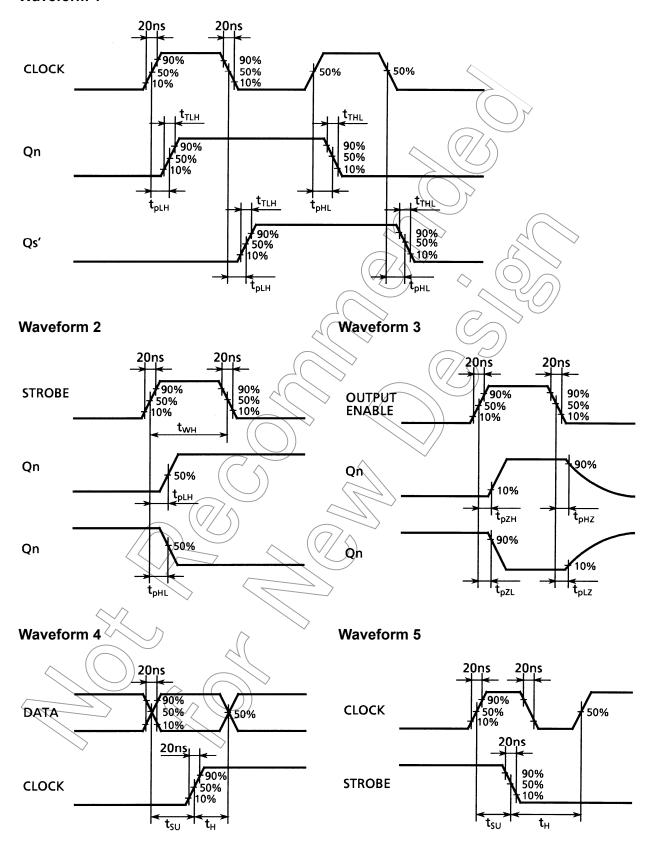
Characteristics	Symbol	Test Condition	V 00	Min	Тур.	Max	Unit
			V <sub>DD</sub> (V)		70	200	
Output transition time	tTLH		10		35	100	ns
(low to high)	TILM	_	15	_	30	80	113
			5		70	200	
Output transition time	t <sub>THL</sub>	_	10		35	100	ns
(high to low)	-1112		15	) <sub>A</sub>	30	80	
		<u></u>	5		150	600	
Propagation delay time	t <sub>pLH</sub>	_	10	_	75	250	ns
(CLOCK-Q <sub>S</sub> )	t <sub>pHL</sub>		15)	_	55	190	
			5	_	155	460	
Propagation delay time	t <sub>pLH</sub>	_ </td <td>10</td> <td>_ /</td> <td>75</td> <td>220</td> <td>ns</td>	10	_ /	75	220	ns
(CLOCK-Q <sub>S</sub> ')	t <sub>pHL</sub>		15		55	) 150	
			5 🛇	(	190	840	
Propagation delay time	t <sub>pLH</sub>	(F)	10	1	90	390	ns
(CLOCK-Q <sub>n</sub> )	t <sub>pHL</sub>		15 (		65	270	
			5	(2)	150	580	
Propagation delay time	t <sub>pLH</sub>		(10)/	\_	70	290	ns
(STROBE-Q <sub>n</sub> )	t <sub>pHL</sub>		15	) _	50	200	
			5	_	60	200	
Three state disable time	tPHZ	$R_{\Delta} = 1 \text{ k}\Omega$	) 1/0	_	35	100	ns
(OUTPUT ENABLE-Q <sub>n</sub> )	tpzh		15	_	30	80	
	6	$\wedge$	5	_	70	200	
Three state disable time	(tpLZ)	$R_L = 1 k\Omega$	10	_	40	100	ns
(OUTPUT ENABLE-Q <sub>n</sub> )	tpzL		15	_	35	80	
			5	_	45	200	
Min clock pulse width	t <sub>W</sub>	$((// \stackrel{\frown}{\rightarrow})$	10	_	20	100	ns
			15	_	15	80	
Min and a middle	(		5	_	40	200	
Min pulse width	t <sub>WH</sub>	_	10	_	20	80	ns
(STROBE)	$\wedge$	$\rightarrow$	15	_	15	70	
	4		5	1.25	6	_	
Max clock frequency	fcL	_	10	2.50	12	_	MHz
			15	3.00	16	_	
Min not up time			5	_	0	120	
Min set-up time	tsu	_	10	_	0	55	ns
(DATA-CLOCK)	$\vee$		15	_	0	35	
Min hold time			5	_	10	40	
Min hold time	t <sub>H</sub>	_	10	_	10	20	ns
(DATA-CLOCK)			15	_	5	15	
Min oot up time			5	_	90	200	
Min set-up time	tsu	_	10	_	40	100	ns
(CLOCK-STROBE)			15	_	30	80	

Characteristics	Symbol	Test Condition	V <sub>DD</sub> (V)	Min	Тур.	Max	Unit
Min hold time (CLOCK-STROBE)	tH	_	5 10 15	_ 		0 0 0	ns
Max clock input rise time Max clock input fall time	t <sub>rCL</sub>	_	5 〈 10 15		No limit		μs
Input capacitance	C <sub>IN</sub>	_	6		5	7.5	pF



### **Waveforms for Measurement of Dynamic Characteristics**

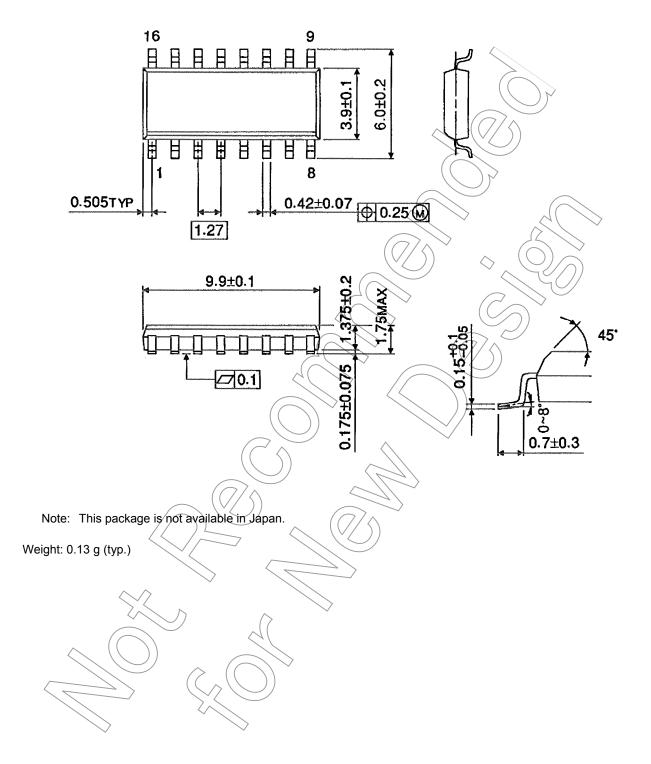
### Waveform 1



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### **Package Dimensions (Note)**

SOL16-P-150-1.27 Unit: mm



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