

FEATURES

- **reclocking of SMPTE 259M signals**
- **operational to 400 Mb/s**
- **adjustment free reclocker when used with the GS9000B or GS9000S decoder and GS9010A Automatic Tuning Sub-system**
- **28 pin PLCC packaging**
- **Pb-free and Green**

APPLICATIONS

- $4f_{SC}$, 4:2:2 and 360 Mb/s serial digital interfaces

ORDERING INFORMATION

Part Number	Package	Temperature	Pb-Free and Green
GS9015BCPJ	28 Pin PLCC	0°C to 70°C	No
GS9015BCTJ	23 Pin PLCC Tape	0°C to 70°C	No
GS90015BCPJE3	28 Pin PLCC	0°C to 70°C	Yes

DEVICE DESCRIPTION

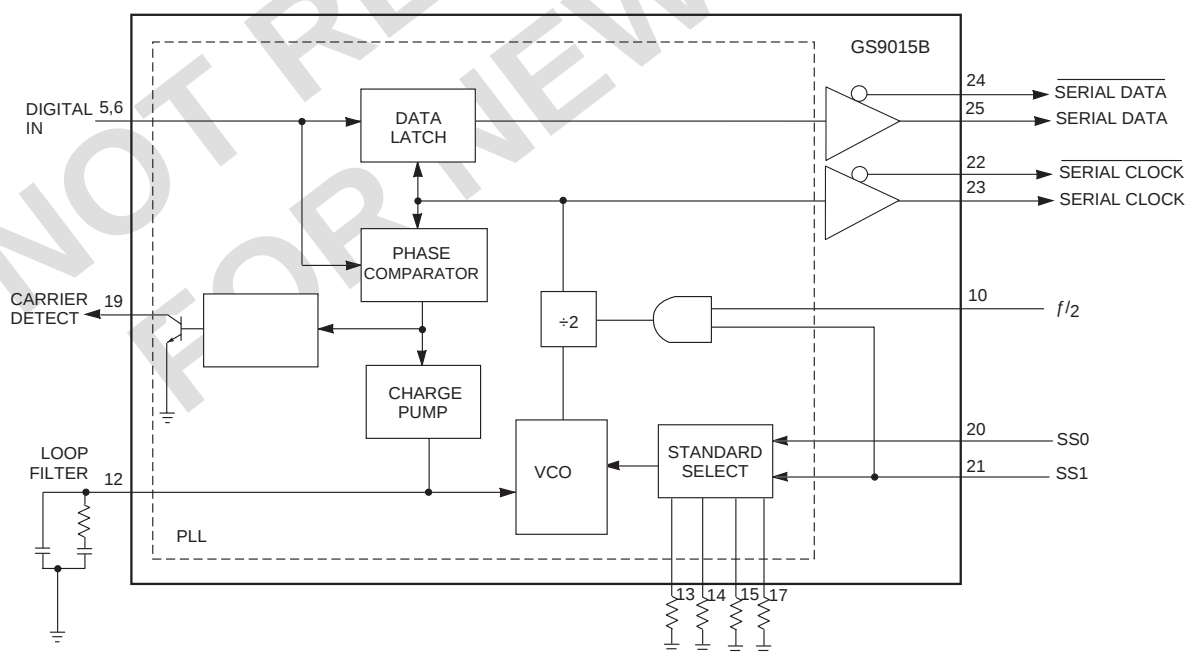
The GS9015B is a monolithic IC designed to receive SMPTE 259M serial digital video signals. This device performs the function of data and clock recovery. It interfaces directly with the **GENLINX™** GS9000B or GS9000S Decoder.

While there are no plans to discontinue the GS9015B, Gennum has developed a successor product with improved features and performance called the GS9035. The GS9035 is recommended for new designs.

The VCO centre frequencies are controlled by external resistors which can be selected by applying a two bit binary code to the Standards Select input pins. Alternatively, the GS9015B can be used with the GS9010A to form an adjustment free reclocker system.

The GS9015B is packaged in a 28 pin PLCC operating from a single +5 or -5 volt supply.

SPECIAL NOTE: R_{VCO1} and R_{VCO2} are functional over a reduced temperature range of $T_A=0^{\circ}\text{C}$ to 50°C . R_{VCO0} and R_{VCO3} are functional over the full temperature range of $T_A=0^{\circ}\text{C}$ to 70°C . This limitation does not affect operation with the GS9010A ATS.



FUNCTIONAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE/UNITS
Supply Voltage	5.5 V
Input Voltage Range (any input)	$V_{CC}+0.5$ to $V_{EE}-0.5$ V
DC Input Current (any one input)	5 mA
Power Dissipation	750 mW
Operating Temperature Range	$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$
Storage Temperature Range	$-65^{\circ}\text{C} \leq T_S \leq 150^{\circ}\text{C}$
Lead Temperature (soldering, 10 seconds)	260°C

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION



GS9015B RECLOCKER DC ELECTRICAL CHARACTERISTICS

$V_S = 5\text{V}$, $T_A = 0^{\circ}\text{C}$ to 70°C , $R_L = 100\Omega$ to $(V_{CC} - 2\text{V})$ unless otherwise shown.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_S	Operating Range	4.75	5.0	5.25	V	
Power Consumption	P_D		-	330	500	mW	
Supply Current (Total)	I_S		-	87	120	mA	see Figure11
Serial Data & Clock Output	- High - Low	V_{OH} V_{OL}	$T_A = 25^{\circ}\text{C}$	-1.025 -1.9	- -1.6	V	with respect to V_{CC}
Logic Inputs (1, 10, 20, 21)	- High - Low	$V_{IH\text{ MIN}}$ $V_{IL\text{ MAX}}$		+2.0 -	- +0.8	V	with respect to V_{EE}
Carrier Detect Output Voltage	V_{CDL} V_{CDH}	$R_L = 10\text{ k}\Omega$ to V_{CC}	4.0	5.0	0.4 -	V	with respect to V_{EE} Open Collector - Active High

GS9015B RECLOCKER AC ELECTRICAL CHARACTERISTICS

$V_S = 5\text{V}$, $T_A = 0^{\circ}\text{C}$ to 70°C , $R_L = 100\Omega$ to $(V_{CC} - 2\text{V})$ unless otherwise shown.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Serial Data Bit Rate	BR_{SDO}	$T_A = 25^{\circ}\text{C}$	100	-	400	Mb/s	
Serial Clock Frequency	f_{SLK}	$T_A = 25^{\circ}\text{C}$	100	-	400	MHz	see Figure 9
Output Signal Swing	V_O	$T_A = 25^{\circ}\text{C}$	700	800	900	mV p-p	see Figure10
Serial Data to Serial Clock Synchronization	t_d	See Waveforms	-	-500	-	ps	Data lags Clock
Lock Times	t_{LOCK}	see note 1	-	-	10	μs	
Jitter	t_J	$T_A = 25^{\circ}\text{C}$, 270 Mb/s	-	± 100	-	ps p-p	see Figure12
Direct Digital Input Levels (5, 6)	V_{DDI}		200	-	2000	mVp-p	Differential Drive

NOTES: 1. Switching between two sources of the same data rate.

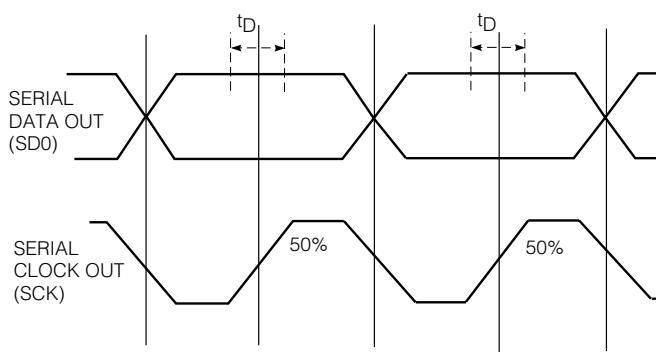


Fig.1 Waveforms

GS9015B Reclocking Receiver - Detailed Device Description

The GS9015B Reclocking Receiver is a bipolar integrated circuit containing circuitry necessary to re-clock and regenerate the NRZI serial data stream.

Packaged in a 28 pin PLCC, the receiver operates from a single five volt supply at data rates to 400 Mb/s. Typical power consumption is 330 mW. Typical output jitter is ± 100 ps at 270 Mb/s.

Serial Digital signals are applied to digital inputs DDI and $\overline{\text{DDI}}$ (pins 5,6).

Phase Locked Loop

The phase comparator itself compares the position of transitions in the incoming signal with the phase of the local oscillator (VCO). The error-correcting output signals are fed to the charge pump in the form of short pulses. The charge pump converts these pulses into a "charge packet" which is accurately proportional to the system phase error.

The charge packet is then integrated by the second-order loop filter to produce a control voltage for the VCO.

During periods when there are no transitions in the signal, the loop filter voltage is required to hold precisely at its last value so that the VCO does not drift significantly between corrections. Commutating diodes in the charge pump keep the output leakage current extremely low, minimizing VCO frequency drift.

The VCO is implemented using a current-controlled multivibrator, designed to deliver good stability, low phase noise and wide operating frequency capability. The frequency range is design-limited to $\pm 10\%$ about the oscillator centre frequency.

VCO Centre Frequency Selection

The centre frequency of the VCO is set by one of four external current reference resistors (RVCO0-RVCO3) connected to pins 13,14,15 or 17. These are selected by two logic inputs SS0 and SS1 (pins 20, 21) through a 2:4 decoder according to the following truth table.

SS1	SS0	Resistor Selected
0	0	RVCO0 (13)
0	1	RVCO1 (14)
1	0	RVCO2 (15)
1	1	RVCO3 (17)

As an alternative, the GS9010A Automatic Tuning Sub-system and the GS9000B or GS9000S Decoder may be used in conjunction with the GS9015B to obtain adjustment free and automatic standard select operation (see Figure17).

With the VCO operating at twice the clock frequency, a clock phase which is centred on the eye of the locked signal is used to latch the incoming data, thus maximising immunity to jitter-induced errors. The alternate phase is used to latch the output re-clocked data SDO and $\overline{\text{SDO}}$ (pins 25, 24). The true and inverse clock signals themselves are available from the SCO and $\overline{\text{SCO}}$ pins 23 and 22.

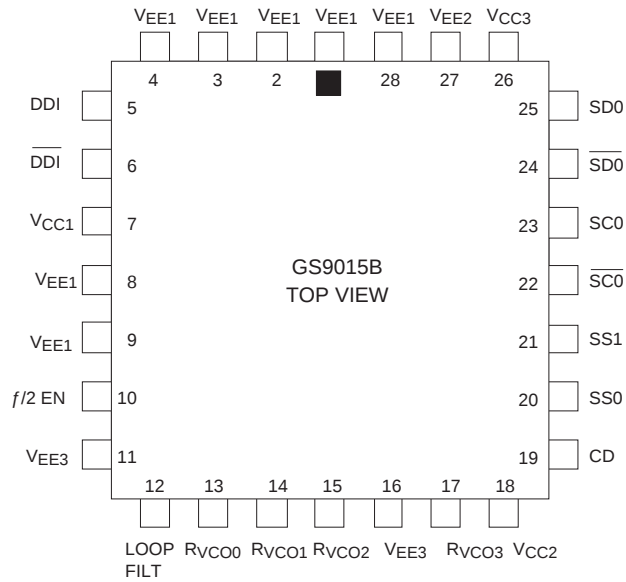


Fig. 2 GS9015B Pin Connections

GS9015B PIN DESCRIPTIONS

PIN NO.	SYMBOL	TYPE	DESCRIPTION
1	V_{EE1}		Power Supply. Most negative power supply connection.
2	V_{EE1}		Power Supply. Most negative power supply connection.
3	V_{EE1}		Power Supply. Most negative power supply connection.
4	V_{EE1}		Power Supply. Most negative power supply connection.
5,6	DDI/ $\overline{\text{DDI}}$	Input	Direct Data Inputs (true and inverse). Pseudo-ECL, differential serial data inputs. They may be directly driven from true ECL drivers when $V_{EE} = -5\text{V}$ and $V_{CC} = 0\text{V}$.
7	V_{CC1}		Power Supply. Most positive power supply connection. (Phase Detector, Carrier Detect).
8, 9	V_{EE1}		Power Supply. Most negative power supply connection.
10	$f/2\text{ EN}$	Input	$f/2$ Enable-TTL compatible input used to enable the divide by 2 function.
11	V_{EE3}		Power Supply. Most negative power supply connection. (VCO, MUX, Standard Select)
12	LOOP FILTER		Loop Filter. Node for connecting the loop filter components.
13	R_{VCO0}	Input	VCO Resistor 0. Analog current input used to set the centre frequency of the VCO when the two Standard Select bits (pins 20 and 21) are set LOW. A resistor is connected from this pin to V_{EE} .
14	R_{VCO1}	Input	VCO Resistor 1. Analog current input used to set the centre frequency of the VCO when Standard Select bit 0 (pin 20) is set HIGH and bit 1 (pin 21) is set LOW. A resistor is connected from this pin to V_{EE} .
15	R_{VCO2}	Input	VCO Resistor 2. Analog current input used to set the centre frequency of the VCO when Standard Select bit 0 (pin 20) is set LOW and bit 1 (pin 21) is set HIGH. A resistor is connected from this pin to V_{EE} .
16	V_{EE3}		Power Supply. Most negative power supply connection.
17	R_{VCO3}	Input	VCO Resistor 3. Analog current input used to set the centre frequency of the VCO when the two Standard Select bits (pins 20 and 21) are set HIGH. A resistor is connected from this pin to V_{EE} .

PIN NO	SYMBOL	TYPE	DESCRIPTION
18	V_{CC2}		Power Supply. Most positive power supply connection. (VCO, MUX, Standard Select).
19	CD	Output	Carrier Detect. Open collector output which goes HIGH when a signal is present at either the Serial Data inputs or the Direct Digital inputs. This output is used in conjunction with the GS9000B or GS9000S in the Automatic Standards Select Mode to disable the 2 bit standard select counter. This pin should see a low AC impedance (e.g. 1nF to AC Gnd)
20,21	SS0, SS1	Inputs	Standard Select Inputs. TTL inputs to the 2:4 multiplexer used to select one of four VCO centre frequency setting resistors (R_{VCO0} - R_{VCO3}). When both SS0 and SS1 are LOW, R_{VCO0} is selected. When SS0 is HIGH and SS1 is LOW, R_{VCO1} is selected. When SS0 is LOW and SS1 is HIGH, R_{VCO2} is selected and when both SS0 and SS1 are HIGH, R_{VCO3} is selected. These pins should see a low AC impedance (e.g. 1nF to AC Gnd)
22,23	$\overline{SCO}/SCO$	Outputs	Serial Clock Outputs (inverse and true). Pseudo-ECL differential outputs of the extracted serial clock. These outputs require a 390 Ω pull-down resistors to V_{EE} .
24,25	$\overline{SDO}/SDO$	Outputs	Serial Data Outputs (inverse and true). Pseudo-ECL differential outputs of the regenerated serial data. These outputs require a 390 Ω pull-down resistors to V_{EE} .
26	V_{CC3}		Power Supply. Most positive power supply connection. (ECL Outputs).
27	V_{EE2}		Power Supply. Most negative power supply connection. (Phase Detector, Carrier Detect)
28	V_{EE1}		Power Supply. Most negative power supply connection.

INPUT / OUTPUT CIRCUITS

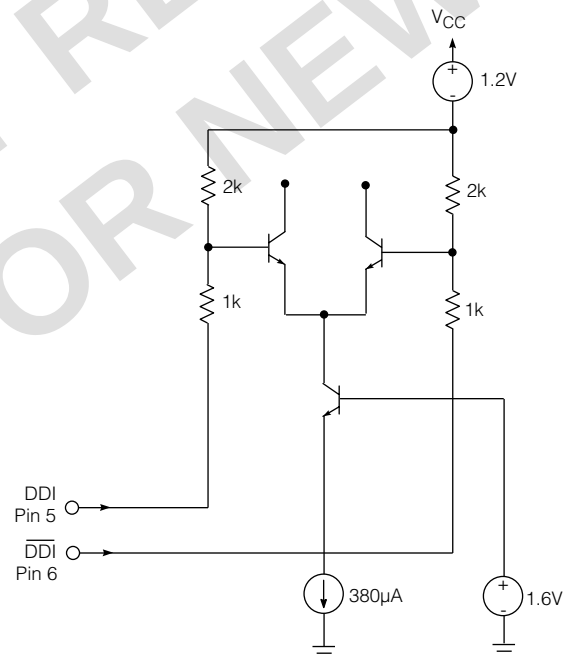


Fig. 3 Pins 1, 5 and 6

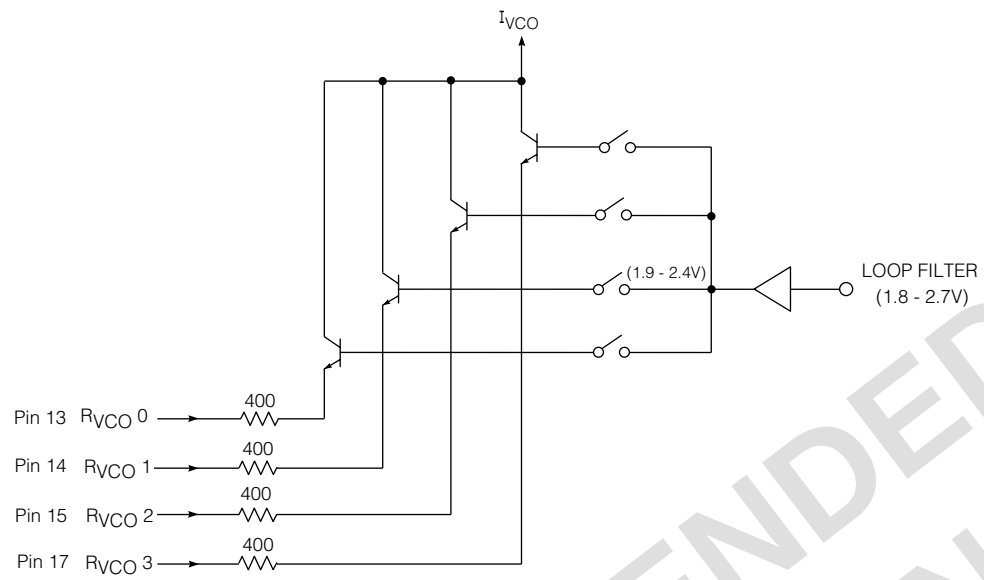


Fig. 4 Pins 13, 14, 15 and 17

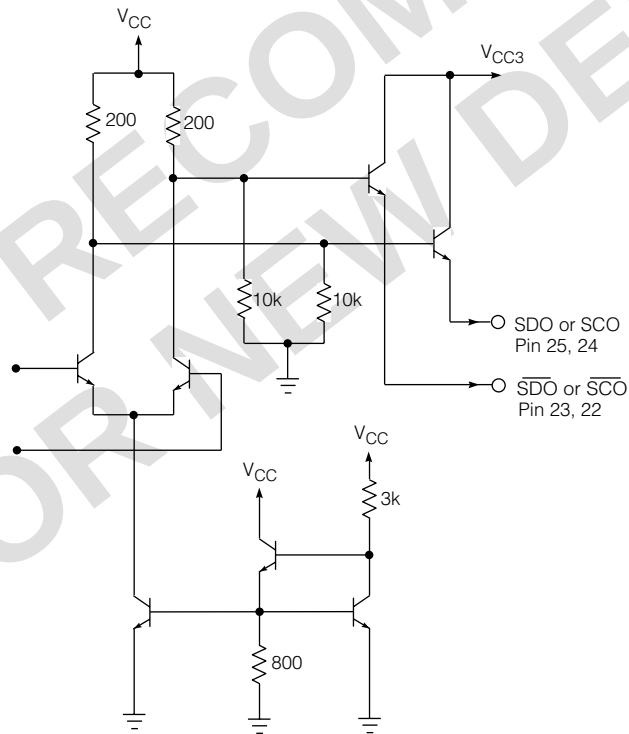


Fig. 5 Pins 25, 24, 23 and 22

INPUT / OUTPUT CIRCUITS cont.

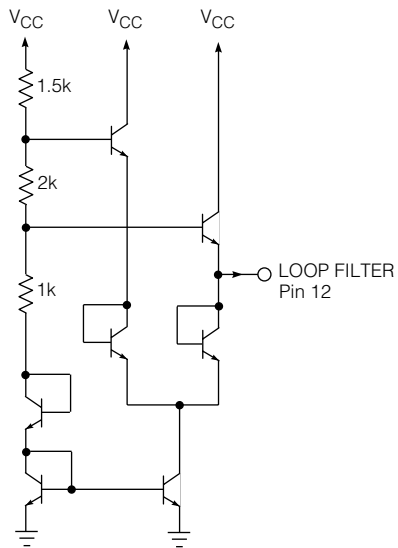


Fig. 6 Pin 12

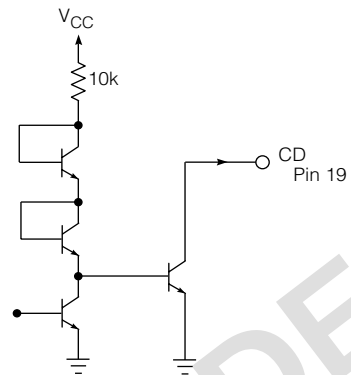


Fig. 7 Pin 19

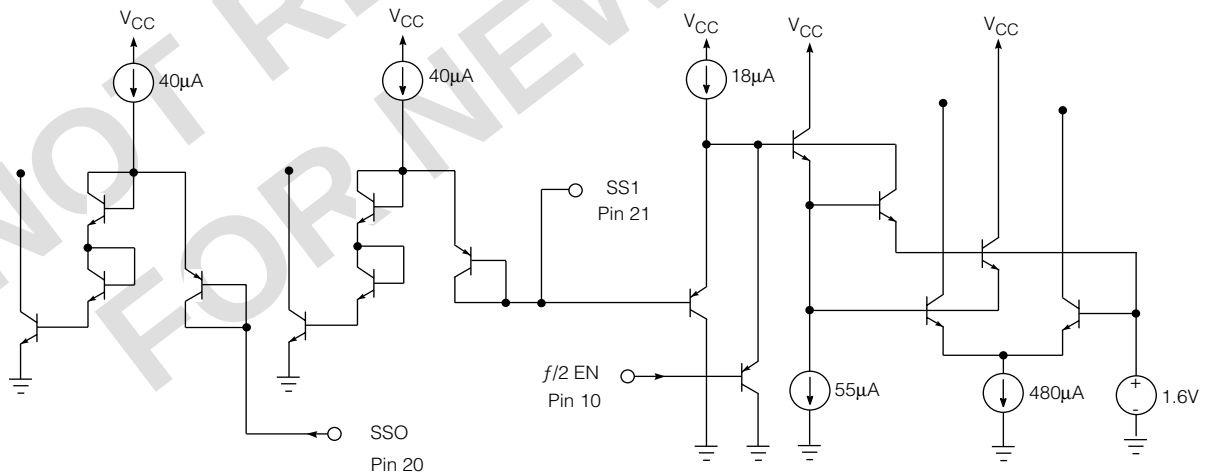


Fig. 8 Pins 20, 21 and 10

TYPICAL PERFORMANCE CURVES

($V_S = 5V$, $T_A = 25^\circ C$ unless otherwise shown)

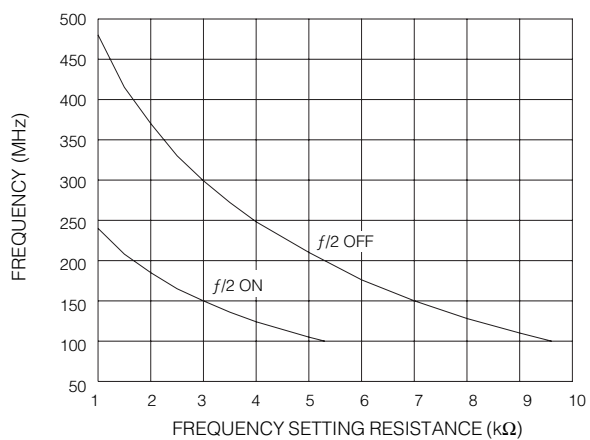


Fig. 9 Clock Frequency

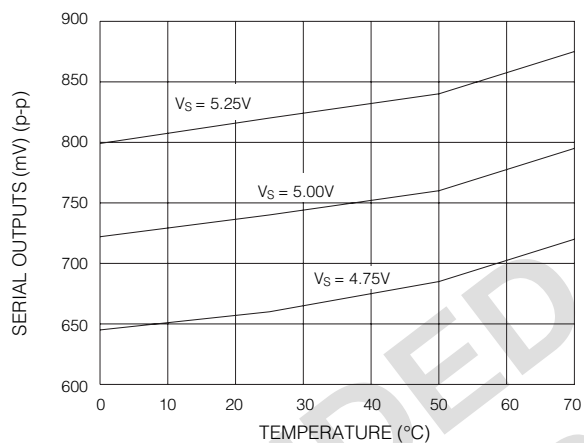


Fig. 10 Serial Outputs

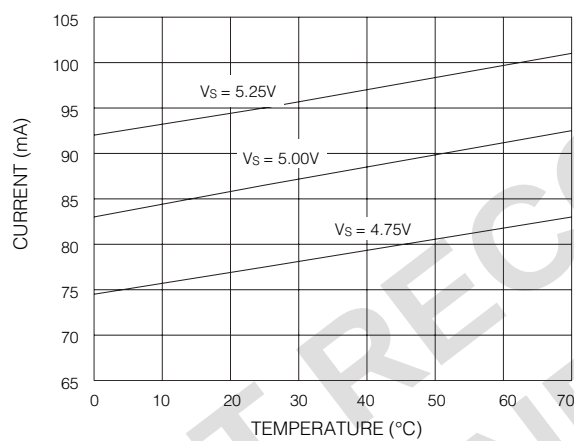


Fig. 11 Supply Current



The loop voltage can be conveniently measured across the 10 nF capacitor in the loop filter. Tuning procedures are described in the Temperature Compensation Section (page 11). The fixed value frequency setting resistors should be placed close to the corresponding pins on the GS9015B.

The SS0, SS1, and CD pins should see a low AC impedance. This is particularly important when driving the SS0, SS1 pins with external logic. The use of 1nF decoupling capacitors at these pins ensures this.

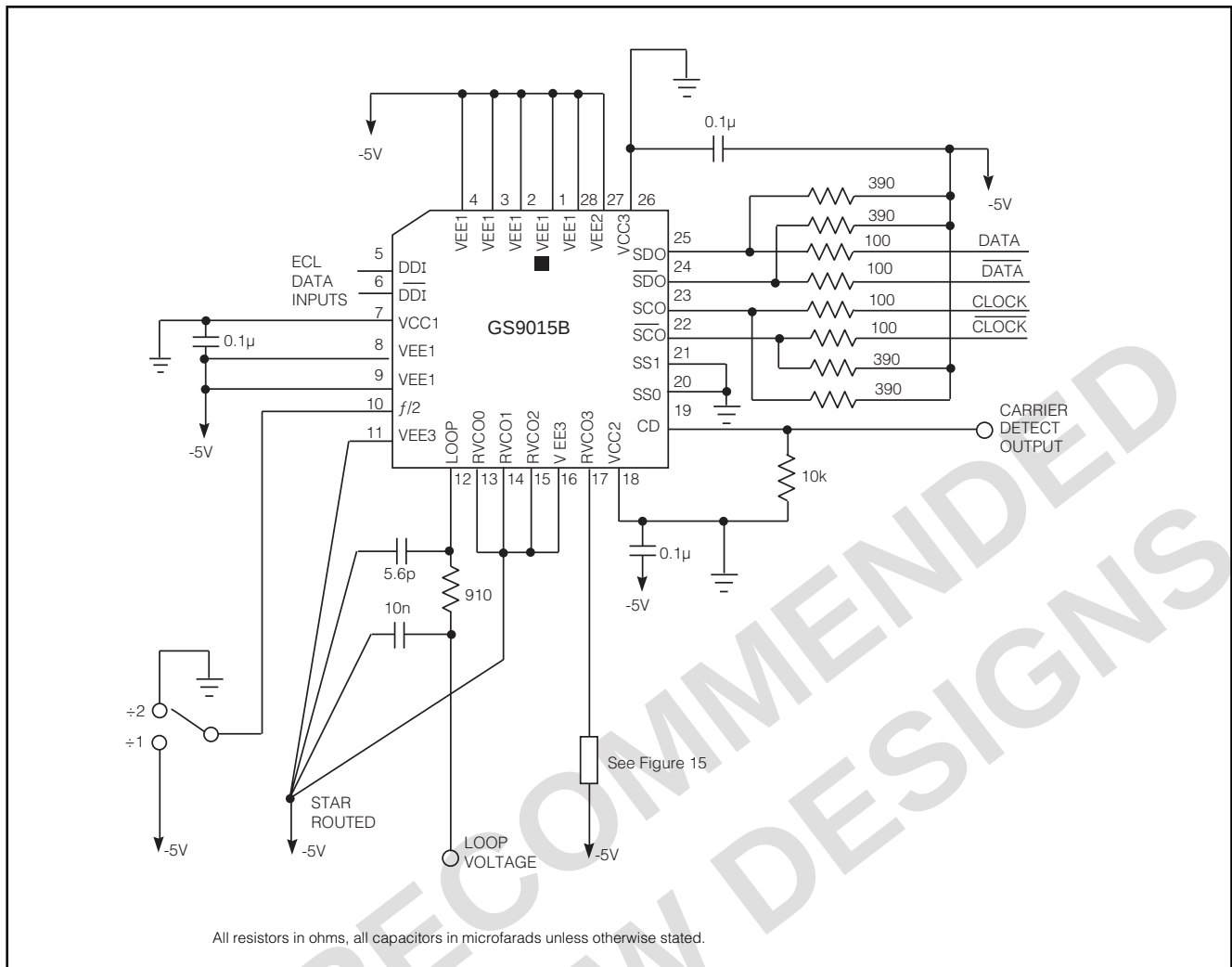


Fig. 13 GS9015B Typical Test Circuit Using -5V Supply

VCO Frequency Setting Resistors

There are two modes of VCO operation available in the GS9015B depending on the state of the $\div 2$ block. The $\div 2$ block is enabled according to: $\div 2 \text{ ENABLE} = f/2 \cdot \text{SS1}$. When the $f/2$ ENABLE (pin 10) is LOW, any of the four VCO frequency setting resistors, RVCO0 through RVCO3, (pins 13, 14, 15 and 17) may be used for any data rate from 100 Mb/s to 400 Mb/s. For example, for 143 Mb/s data rate, the value of the total RVCO resistance is approximately 6k8 and for 270 Mb/s operation, the value is approximately 3k5. The 5k potentiometers will then tune the desired data rate near their mid-points.

Jitter performance at the lower data rates (143, 177 Mb/s) is improved by operating the VCO at twice the normal frequency. This is accomplished by enabling the divide by two block in the PLL section of the GS9015B.

When $f/2$ (Pin 10) is HIGH, two of the RVCO pins are assigned to data rates below 200 Mb/s and two are assigned to data rates over 200 Mb/s. The selection is dependent upon the level of STANDARD SELECT BIT, SS1 (pin 21). When SS1 is LOW, RVCO0 and RVCO1 (pins 13 and 14) are used for the higher data rates. When SS1 is HIGH, the VCO frequency is now twice the bit rate and its frequency is set by RVCO2 and RVCO3 (pins 15 and 17).

For 143 Mb/s and 270 Mb/s operation, (the VCO is at 286 MHz and 270 MHz respectively) the total resistance required is approximately the same for both data rates. This also applies for 177 Mb/s and 360 Mb/s operation (the VCO is tuned to 354 MHz and 360 MHz respectively). This means that one potentiometer may be used for each frequency pair with only a small variation of the fixed resistor value. This halves the number of adjustments required.

Temperature Compensation

Figure 14 shows the connections for the frequency setting resistors for the various data rates. The compensation shown for 360 Mb/s and 177 Mb/s with Divide by 2 ON, is useful to a maximum ambient temperature of 50°C. If the Divide by 2 function is not enabled by the $f/2$ ENABLE input, no compensation is needed for the 143 Mb/s and 177 Mb/s data rates. The resistor connections are shown in Figure 15. In both cases, the 0.1µF capacitor that bypasses the potentiometer should be star routed to VEE3.

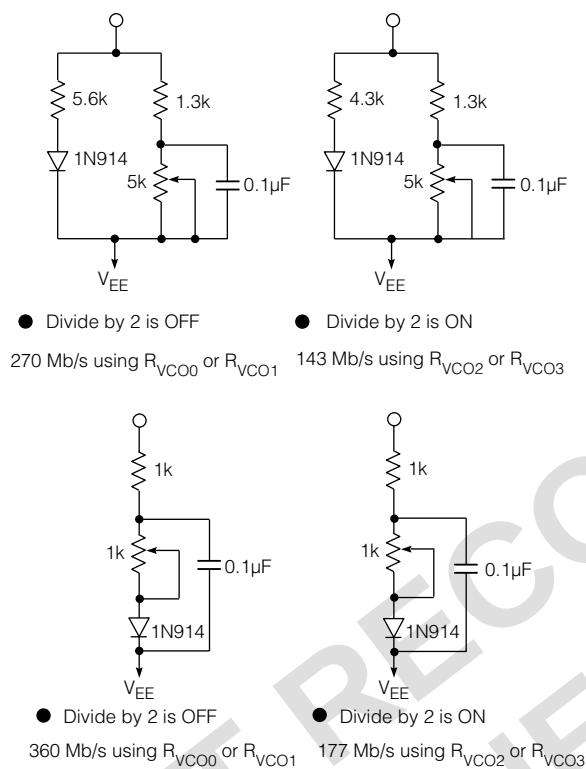
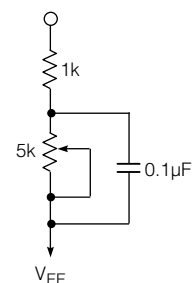


Fig. 14 Frequency Setting Resistor Values
& Temperature Compensation

Temperature Compensation Procedure

In order to correctly set the VCO frequency so that the PLL will always re-acquire lock over the full temperature range, the following procedure should be used. The circuit should be powered on for at least one minute prior to starting this procedure.

Monitor the loop filter voltage at the junction of the loop filter resistor and 10 nF loop filter capacitor (LOOP FILTER TEST POINT). Using the appropriate network shown above, the VCO frequency is set by first tuning the potentiometer so that the PLL loses lock at the low end (lowest loop filter voltage). The loop filter voltage is then slowly increased by adjusting the potentiometer to determine the error free low limit of the capture range. Error free operation is determined by using a suitable CRC or EDH measurement method to obtain a stable signal with no errors. Record the loop filter voltage at this point as V_{CL} . Now adjust the potentiometer so that the loop filter voltage is 250 mV above V_{CL} .



● Divide by 2 is OFF

143Mb/s and 177 Mb/s using any R_{VCO} pins

Fig. 15 Non - Temperature Compensated Resistor Values
for 143 Mb/s and 177 Mb/s

Loop Bandwidth

The loop bandwidth is dependant upon the internal PLL gain constants along with the loop filter components connected to pin 12. In addition, the impedance seen by the RVCO pin also influences the loop characteristics such that as the impedance drops, the loop gain increases.

Applications Circuit

Figure 16 shows an application of the GS9015B in an adjustment free, multi-standard serial to parallel convertor. This circuit uses the GS9010A Automatic Tuning Sub-system IC and a GS9000B or GS9000S Decoder IC.

The GS9010A ATS eliminates the need to manually set or externally temperature compensate the Receiver or Reclocker VCO. The GS9010A can also determine whether the incoming data stream is 4fsc NTSC, 4fsc PAL or component 4:2:2.

The GS9010A includes a ramp generator/oscillator which repeatedly sweeps the Reclocker VCO frequency over a set range until the system is correctly locked. An automatic fine tuning (AFT) loop maintains the Reclocker VCO control voltage at it's centre point through continuous, long term adjustments of the VCO centre frequency.

During normal operation, the GS9000B or GS9000S Decoder provides continuous HSYNC pulses which disable the ramp/oscillator of the GS9010A. This maintains the correct Reclocker VCO frequency. When an interruption to the incoming data stream is detected by the Reclocker, the Carrier Detect goes LOW and opens the AFT loop in order to maintain the correct VCO frequency for a period of at least 2 seconds. This allows the Reclocker to rapidly relink when the signal is re-established.

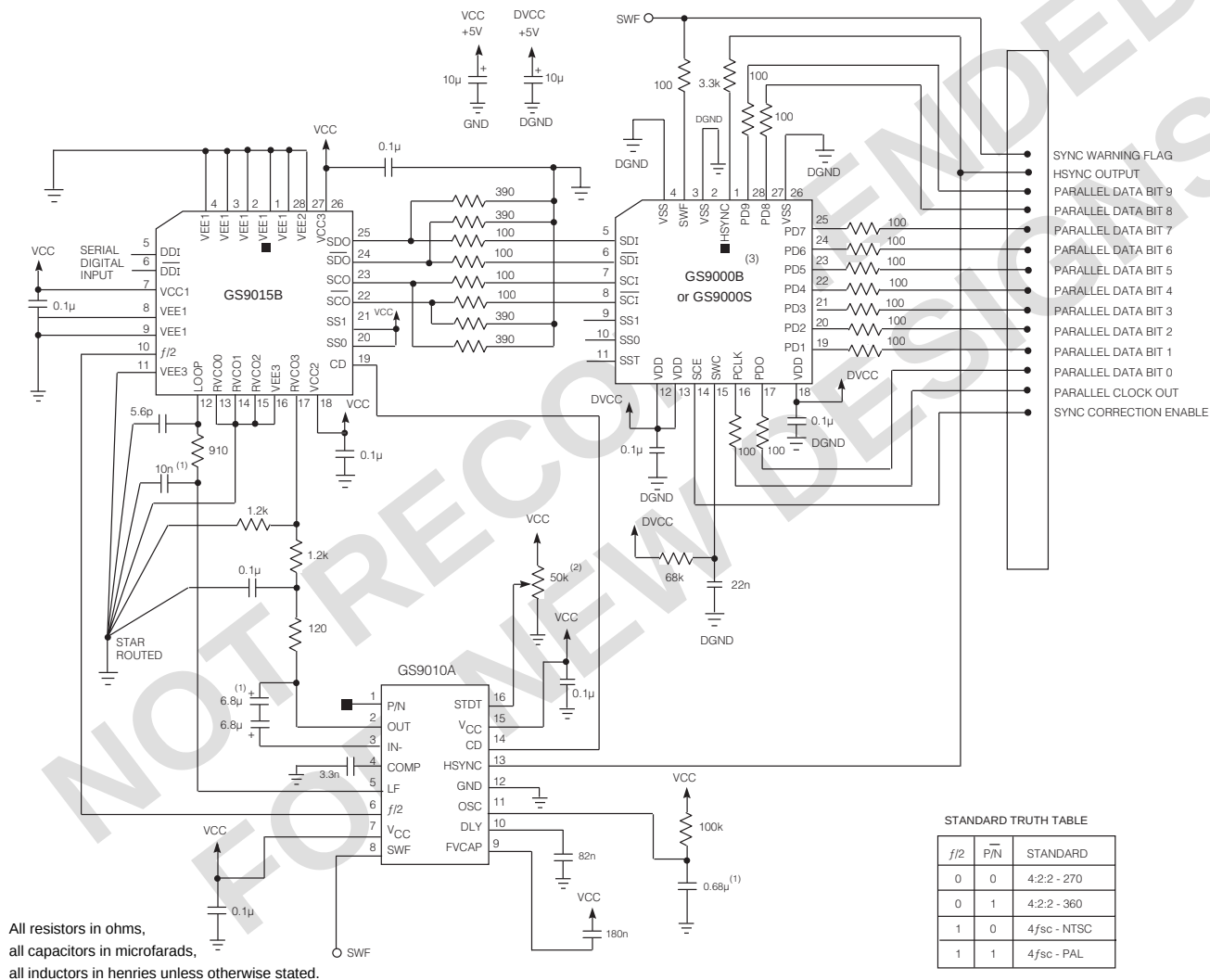
Application Note - PCB Layout

Special attention must be paid to component layout when designing high performance serial digital receivers. For background information on high speed circuit and layout design concepts, refer to Document No. 521-32-00, "Optimizing Circuit and Layout Design of the GS90005A/15A". A recommended PCB layout can be found in the Gennum Application Note "EB9010B Deserializer Evaluation Board"

The use of a star grounding technique is required for the loop filter components of the GS9005B/15B.

Controlled impedance PCB traces should be used for the differential clock and data interconnection between the GS9005B and the GS9000B or GS9000S. These differential traces must not pass over any ground plane discontinuities. A slot antenna is formed when a microstrip trace runs across a break in the ground plane.

The series resistors at the parallel data output of the GS9000B or GS9000S are used to slow down the fast rise/fall time of the GS9000B or GS9000S outputs. These resistors should be placed as close as possible to the GS9000B or GS9000S output pins.



(1) To reduce board space, the two anti-series 6.8 μ F capacitors (connected across pins 2 and 3 of the GS9010A) may be replaced with a 1.0 μ F non-polarized capacitor provided that:

- (a) the 0.68 μ F capacitor connected to the OSC pin (11) of the GS9010A is replaced with a 0.33 μ F capacitor and
- (b) the GS9005B/15B Loop Filter Capacitor is 10 nF.

(2) Remove this potentiometer if P/N function is not required, and ground pin 16 of the GS9010A.

(3) The GS9000B will operate to a maximum frequency of 370 Mbps. The GS9000S will operate to a maximum of 300 Mbps.

Fig. 16 Typical Application Circuit

NOT RECOMMENDED
FOR NEW DESIGNS

DOCUMENT IDENTIFICATION: DATA SHEET

The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

REVISION NOTES:

New document.
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GENNUM CORPORATION

MAILING ADDRESS:

P.O. Box 489, Str. A, Burlington, Ontario, Canada L7R 3Y3
Tel. +1 (905) 632-2996 Fax +1 (905) 632-2814

SHIPPING ADDRESS:

970 Fraser Drive, Burlington, Ontario, Canada L7L 5P5

GENNUM JAPAN CORPORATION

Shinjuku Green Tower Building 27F 6-14-1, Nishi Shinjuku Shinjuku-ku,
Tokyo 160-0023 Japan Tel: +81 (03) 3349-5501 Fax: +81 (03) 3349-5505

GENNUM UK LIMITED

Centaur House, Ancells Business Park, Ancells Road, Fleet, Hampshire, UK GU13 8UJ
Tel. +44 (1252) 761 039 Fax +44 (1252) 761 114

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