MIC4609

600V 3-Phase MOSFET/IGBT Driver

Features

- Gate Drive Supply Voltage up to 20V
- Overcurrent Protection with Programmable Restart Delay
- 1A Gate Drivers
- Dual (HI/LI) Inputs per Phase
- Fault Signal Asserts on Overcurrent and V_{DD} UVLO
- TTL Input Thresholds
- 300 ns Typical Input Filtering Time
- Shoot-Through Protection
- Low-Power Consumption
- Supply Undervoltage Protection
- -40°C to +125°C Junction Temperature Range

Typical Applications

- 3-Phase Motor Drive
- Field-Oriented Control (FOC)
- White Goods Appliances
- Brushless DC Fans

General Description

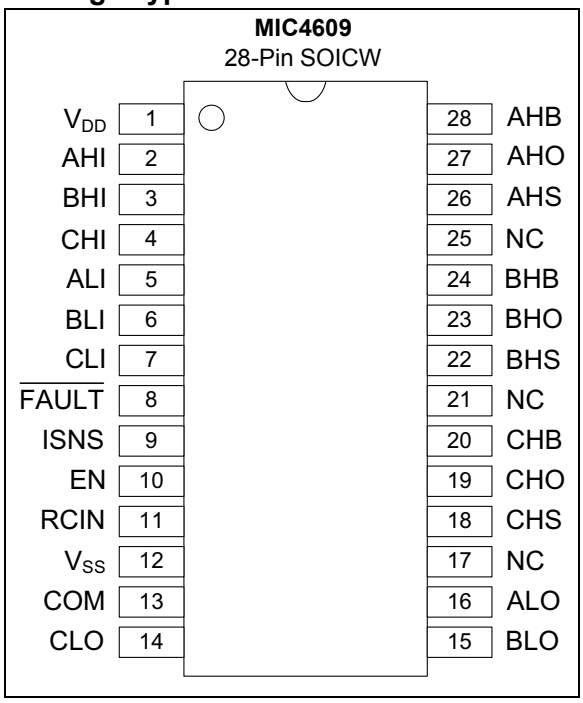
The MIC4609 is a 600V 3-phase MOSFET/IGBT driver. The MIC4609 features a 300 ns typical input filtering time to prevent unwanted pulses and a 550 ns of propagation delay. The MIC4609 has TTL input thresholds.

The robust operation of the MIC4609 ensures that the outputs are not affected by supply glitches, High Side (HS) ringing below ground, or HS slewing with high-speed voltage transitions. Undervoltage protection is provided on both the low-side and high-side drivers.

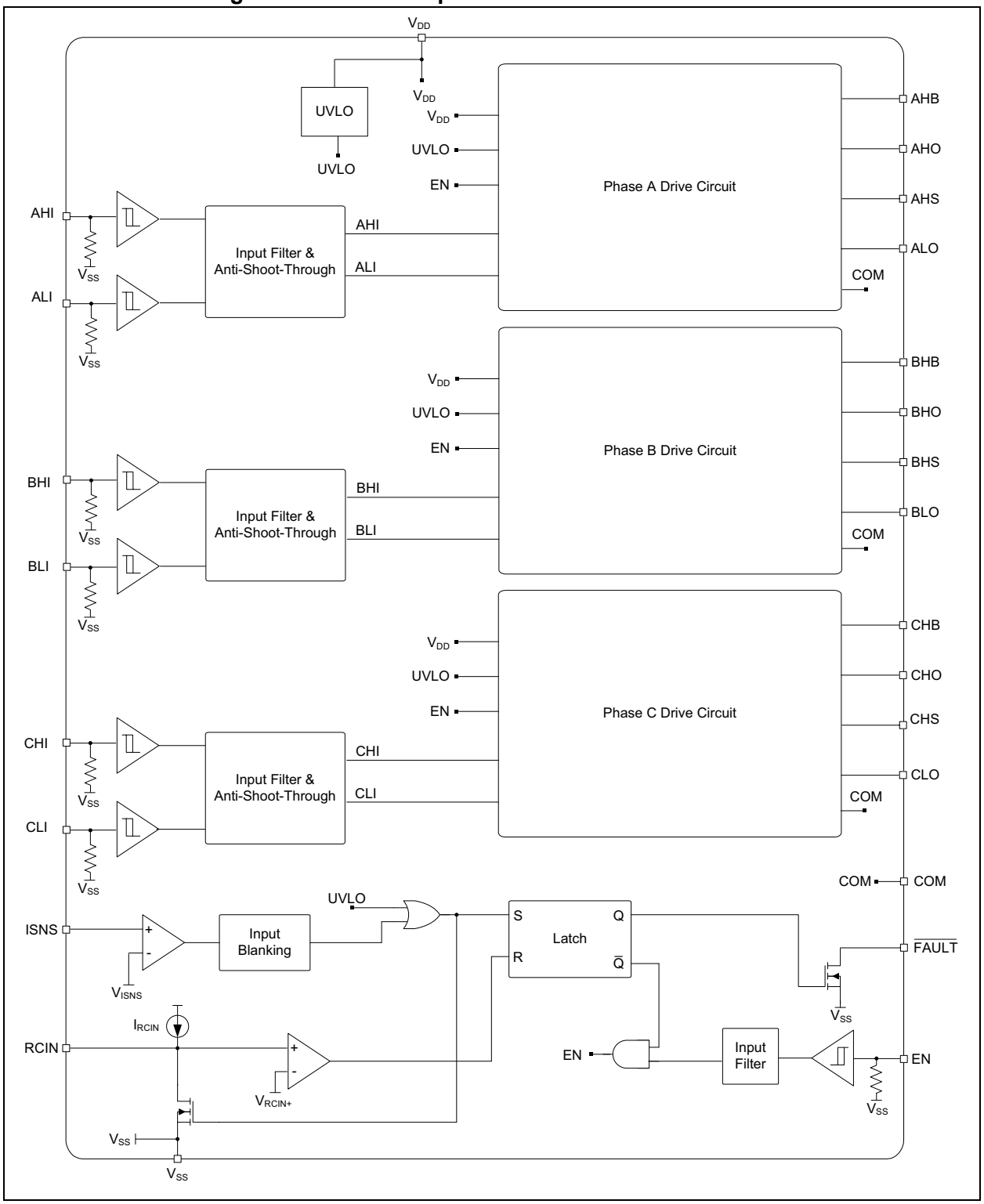
The MIC4609 is available in a 28-pin wide SOIC package. The MIC4609 has an operating junction temperature range of -40°C to +125°C.

Package Type

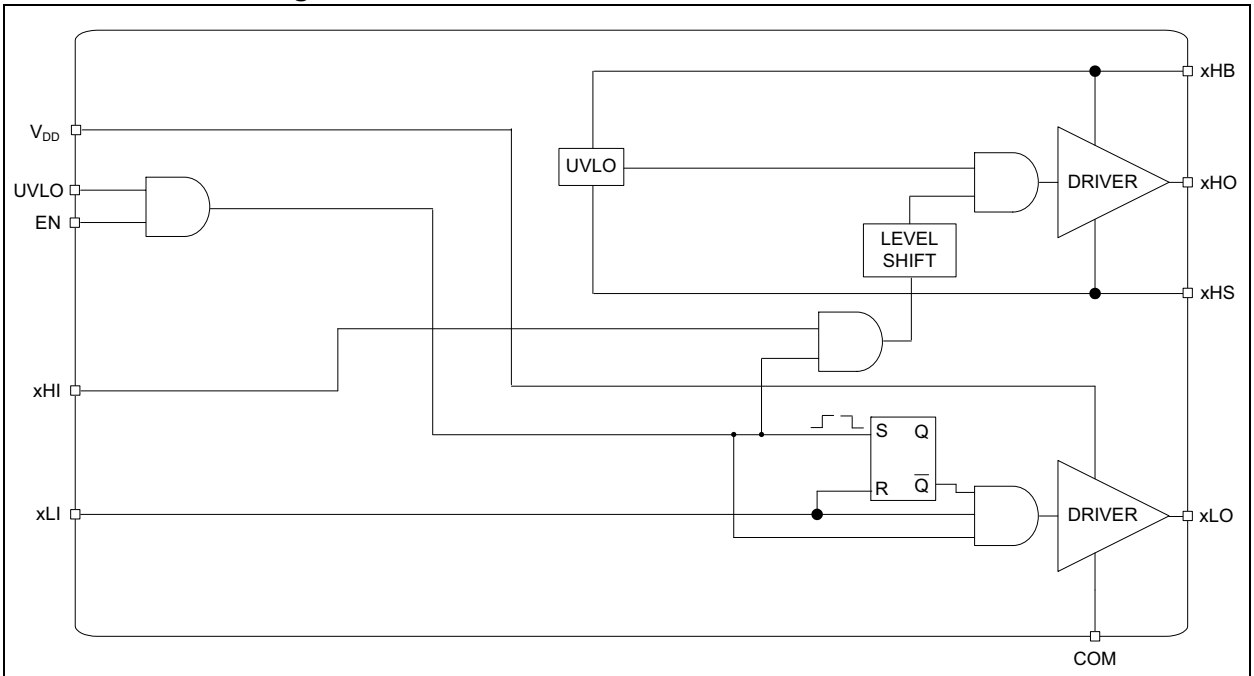
MIC4609
28-Pin SOICW



Functional Block Diagram MIC4609 – Top Level Circuit

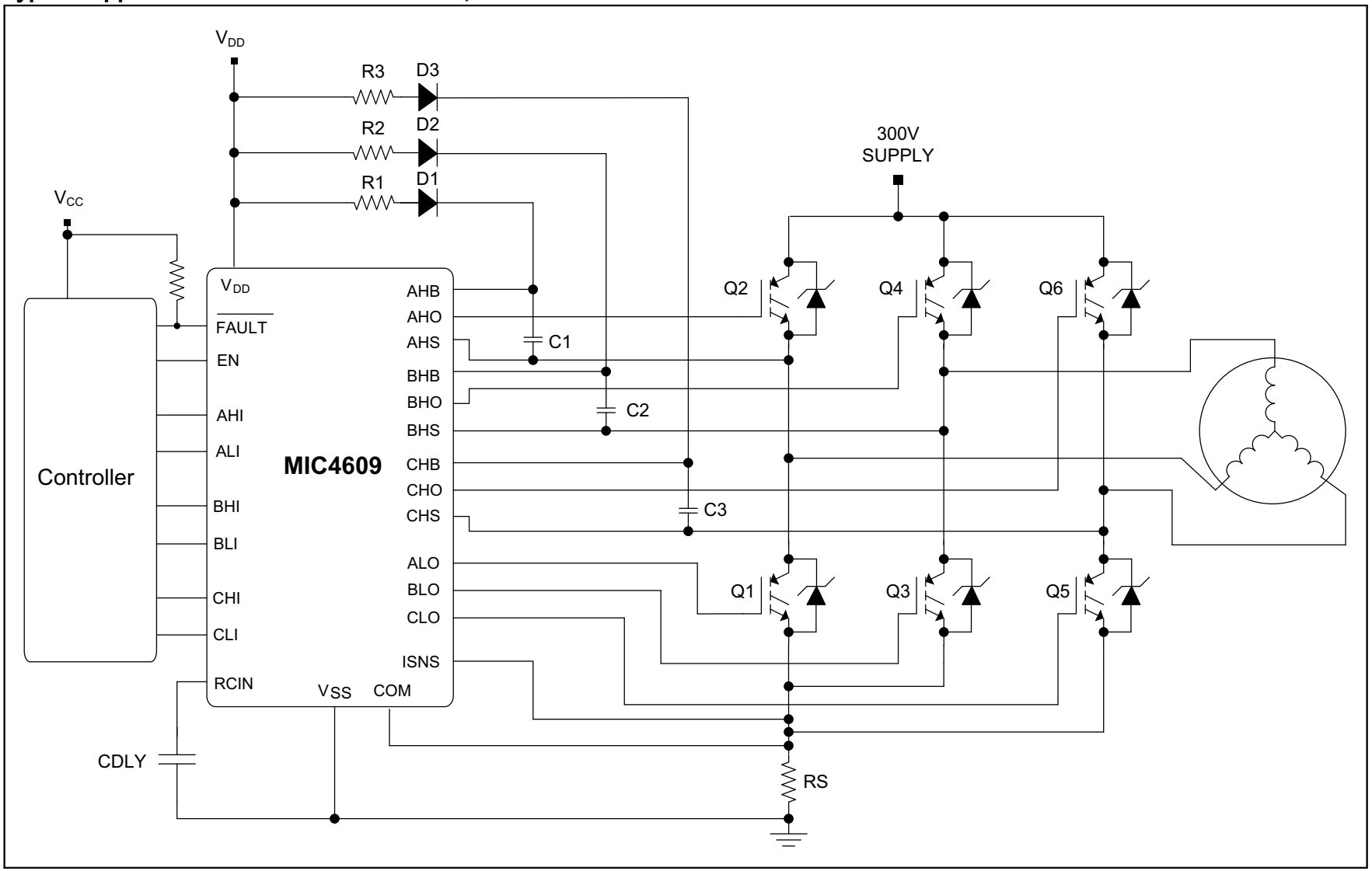


Functional Block Diagram MIC4609 – Phase x Drive Circuit



Note: The x in the suffix of a pin name designates any of the three phases, e.g., xHS refers to either AHS, BHS or CHS.

Typical Application Circuit MIC4609 – 300V, 3-Phase Motor Driver



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD}, V_{xHB} - V_{xHS}) ..... -0.3V to +25V
Input Voltages (V_{xLI}, V_{xHI}, V_{EN}) ..... -0.3V to V_{DD}
Voltage on LO (V_{xLO}) ..... -0.3V to V_{DD}
Voltage on HO (V_{xHO}) ..... V_{HS} - 0.3V to V_{HB}
Voltage on HS ..... -5V to +630V
Voltage on HB ..... +655V
Storage Temperature ..... -60°C to +150°C
ESD Rating
HBM 2kV
CDM ..... 1.5 kV

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Operating Ratings (1)

Supply Voltage (V_{DD}) ..... +10V to +20V
Voltage on xHS (continuous) ..... -1V to +600V
Voltage on xHS (repetitive transient) ..... -5V to +600V
HS Slew Rate 50V/ns
Voltage on xHB ..... V_{xHS} + 10V to V_{xHS} + 20V
and/or ..... V_{DD} - 1V to V_{DD} + 600V
Junction Temperature (T_J) ..... -40°C to +125°C
Junction Thermal Resistance (θ_{JA}) ..... -40°C to +125°C
SOIC Wide 28LD ..... 53°C/W

Note 1: The device is not guaranteed to function outside its operating rating.

AC/DC ELECTRICAL CHARACTERISTICS (Note 1, 2)

Electrical Specifications: Unless otherwise indicated, V_{DD} = V_{xHB} = 20V, V_{EN} = 5V, V_{SS} = V_{xHS} = 0V; No load on xLO or xHO, T_A = +25°C. **Bold** values indicate -40°C ≤ T_J ≤ +125°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Current						
V_{DD} Quiescent Current	I_{DD}	—	150	**250**	µA	xLI = xHI = 0V
V_{DD} Shutdown Current	I_{DDSH}	—	0.1	**10**	µA	EN = 0V with HS = floating or ground
V_{DD} Operating Current	I_{DDO}	—	240	**350**	µA	f = 20 kHz
Total xHB Quiescent Current	I_{xHB}	—	81	**180**	µA	xLI = xHI = 0V or xLI = 0V and xHI = 5V
Total xHB Operating Current	I_{xHBO}	—	600	**1500**	µA	f = 20 kHz
High-Side Leakage Current	I_{LxHB}	—	1	**10**	µA	V_{xHB} = V_{xHS} = 600V
Input (TTL: xLI, xHI, EN)						
Low-Level Input Voltage	V_{IL}	—	—	**0.8**	V	
High-Level Input Voltage	V_{IH}	**2.2**	—	—	V	
Input Voltage Hysteresis	V_{HYS}	—	0.2	—	V	
Input Pull-Down Resistance	R_I	**100**	370	**500**	kΩ	For xLI and xHI only (**Note 3**)
Undervoltage Protection						
V_{DD} Falling Threshold	V_{DDR}	**7**	8	**9**	V	
V_{DD} Threshold Hysteresis	V_{DDH}	—	0.5	—	V	
xHB Falling Threshold	V_{xHBR}	**7**	8	**9**	V	
xHB Threshold Hysteresis	V_{xHBH}	—	0.5	—	V	

Note 1: Specification for packaged product only.
2: The x in the suffix of a pin name designates any of the three phases, e.g., xHS refers to either AHS, BHS or CHS.
3: Enable resistance is typical only and is not production tested.

AC/DC ELECTRICAL CHARACTERISTICS (CONTINUED) (Note 1, 2)

Electrical Specifications: Unless otherwise indicated, V_{DD} = V_{xHB} = 20V, V_{EN} = 5V, V_{SS} = V_{xHS} = 0V; No load on xLO or xHO, T_A = +25°C. **Bold** values indicate -40°C ≤ T_J ≤ +125°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Overcurrent Protection						
Rising Overcurrent Threshold	V_{ISNS+}	420	520	650	mV	
ISNS Pin Blanking Time	t_{ISNS_BLK}	270	370	470	ns	
ISNS-to-Gate Propagation Delay	t_{ISNS_PROP}	400	650	900	ns	
Fault Circuit						
$\overline{\text{Fault}}$ Pin Output Low Voltage	V_{OLF}	—	—	**0.8**	V	V_{ISNS} = 1V, I_{FAULT} = 1 mA
Rising VCIN Pin Threshold	V_{RCIN+}	—	5	—	V	
VCIN Hysteresis	V_{RCIN_HYS}	—	0.6	—	V	
RCIN Pin Current Source	I_{RCIN}	3	5	7	µA	V_{RCIN} = 0V
Fault Clear Time	t_{FCL}	0.5	1	2	ms	C_{RCIN} = 1nF
LO Gate Driver						
Low-Level Output Voltage	V_{xOLL}	—	0.5	**0.9**	V	I_{xLO} = 50 mA
High-Level Output Voltage	V_{xOHL}	—	0.6	**0.9**	V	I_{xLO} = -50 mA V_{xOHL} = V_{DD} - V_{xLO}
Peak Sink Current	I_{xOHL}	—	1	—	A	V_{xLO} = 0V
Peak Source Current	I_{xOLL}	—	1	—	A	V_{xLO} = 20V
HO Gate Driver						
Low-Level Output Voltage	V_{xOLH}	—	0.5	**0.9**	V	I_{xHO} = 50 mA
High-Level Output Voltage	V_{xOHH}	—	0.6	**0.9**	V	I_{xHO} = -50 mA V_{xOHH} = V_{xHB} - V_{xHO}
Peak Sink Current	I_{xOHH}	—	1	—	A	V_{xHO} = 0V
Peak Source Current	I_{xOLH}	—	1	—	A	V_{xHO} = 20V
Switching Specifications						
Turn-On Propagation Delay	t_{ON}	300	600	700	ns	C_L = 1 nF
Turn-Off Propagation Delay	t_{OFF}	300	550	700	ns	C_L = 1 nF
Turn-On Rise Time	t_R	—	20	60	ns	C_L = 1 nF
Turn-Off Fall Time	t_F	—	20	60	ns	C_L = 1 nF
Input Filtering Time	t_{FLTR}	200	300	480	ns	xLI, xHI, EN
Dead Time	t_D	200	300	450	ns	C_L = 1 nF
Delay Matching	t_{DLYM}	—	50	—	ns	C_L = 1 nF
EN-to-Gate Shutdown Delay	t_{EN_OFF}	450	650	750	ns	C_L = 1 nF
Output Pulse Width Matching	t_{PWN}	—	50	—	ns	t_{PW} > 1 µs C_L = 1 nF

Note 1: Specification for packaged product only.

2: The x in the suffix of a pin name designates any of the three phases, e.g., xHS refers to either AHS, BHS or CHS.

3: Enable resistance is typical only and is not production tested.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply with 10V ≤ V_{DD} ≤ 20V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range (**Note 1**)	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_S	-60	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 28LD SOICW	θ_{JA}	—	53	—	°C/W	

Note 1: Operation in this range must not cause T_J to exceed Maximum Junction Temperature (+125°C).

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C with 10V ≤ V_{DD} ≤ 20V.

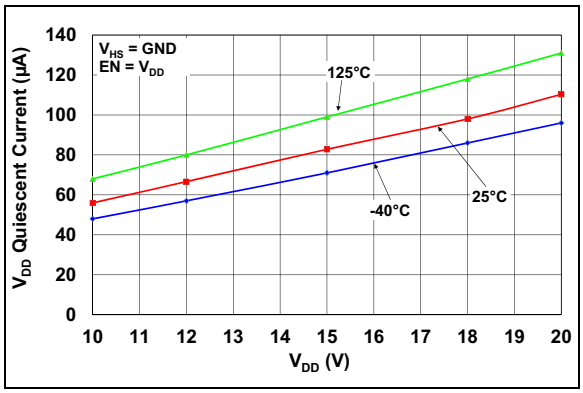


FIGURE 2-1: *V_{DD} Quiescent Current vs. V_{DD} Voltage.*

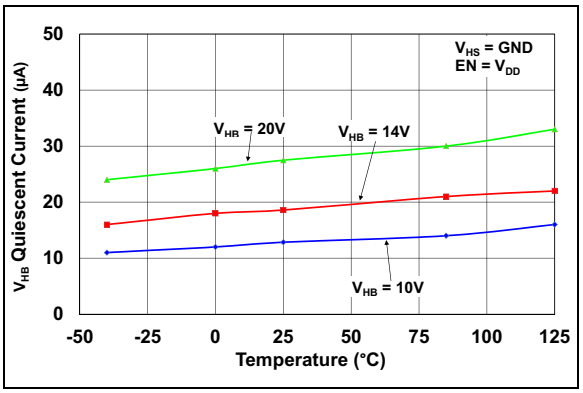


FIGURE 2-4: *V_{HB} Quiescent Current vs. Temperature.*

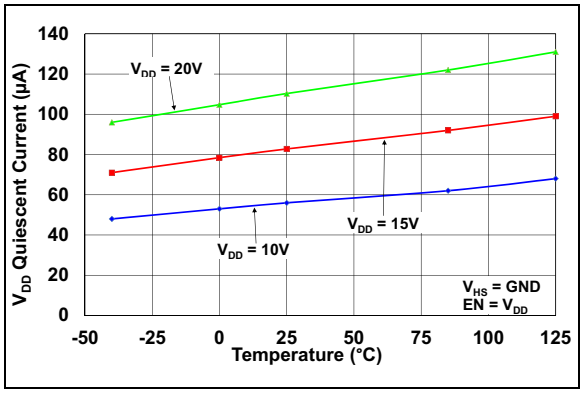


FIGURE 2-2: *V_{DD} Quiescent Current vs. Temperature.*

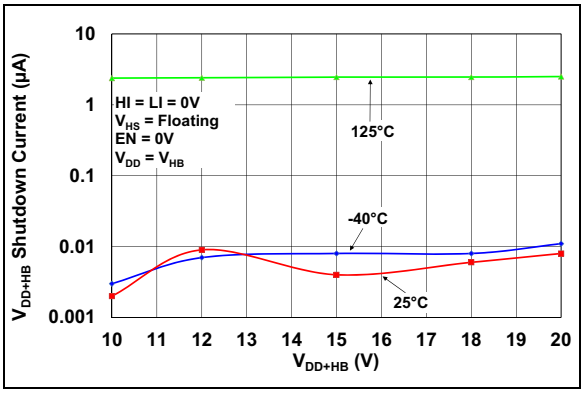


FIGURE 2-5: *V_{DD+HB} Shutdown Current vs. Voltage.*

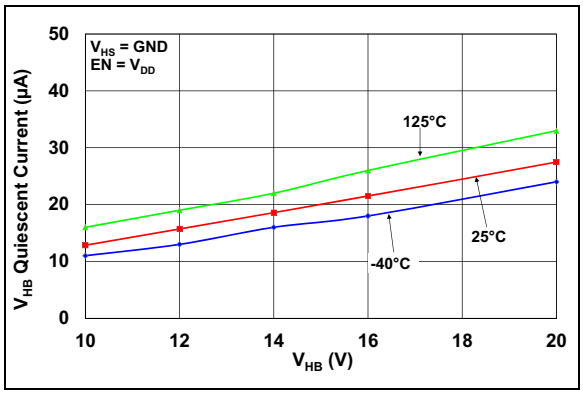


FIGURE 2-3: *V_{HB} Quiescent Current vs. V_{HB} Voltage.*

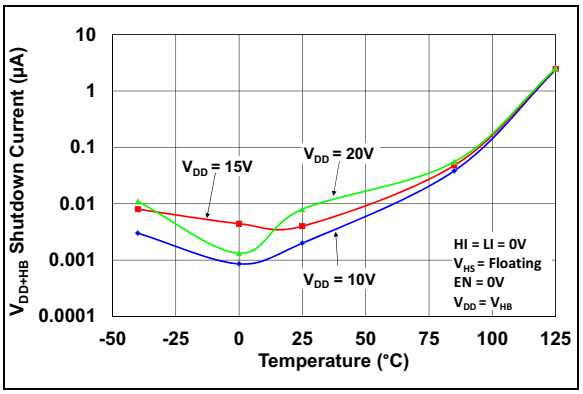


FIGURE 2-6: *V_{DD+HB} Shutdown Current vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C with 10V ≤ V_{DD} ≤ 20V.

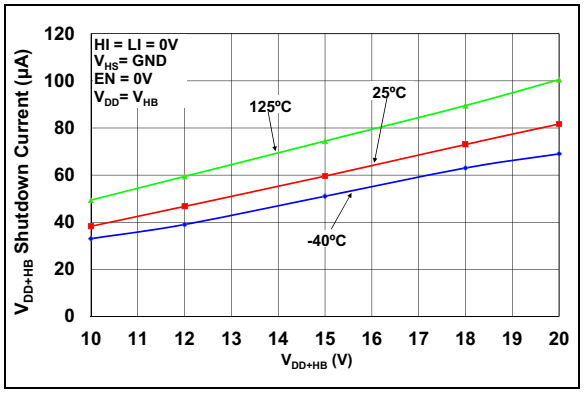


FIGURE 2-7: *V_{DD+HB} Shutdown Current vs. Voltage.*

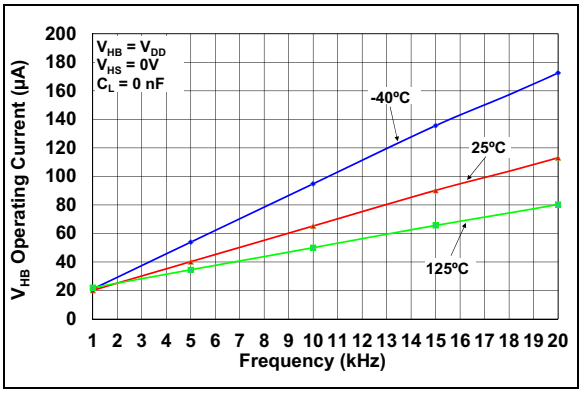


FIGURE 2-10: *V_{HB} Operating Current vs. Frequency – One Phase.*

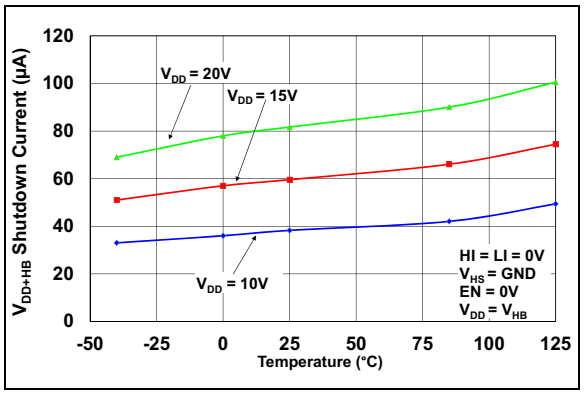


FIGURE 2-8: *V_{DD+HB} Shutdown Current vs. Temperature.*

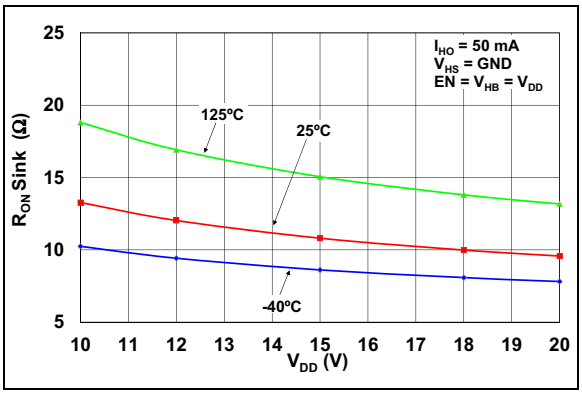


FIGURE 2-11: *HO Output Sink ON-Resistance vs. V_{DD}.*

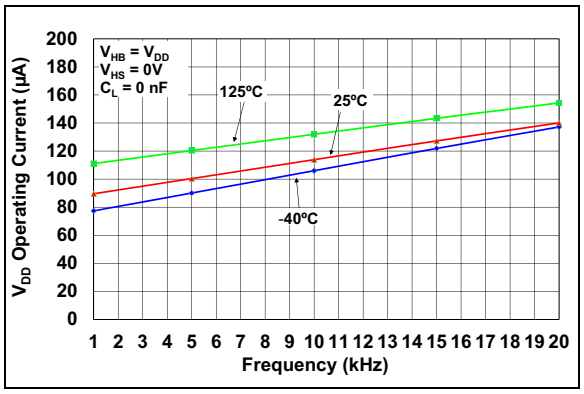


FIGURE 2-9: *V_{DD} Operating Current vs. Frequency.*

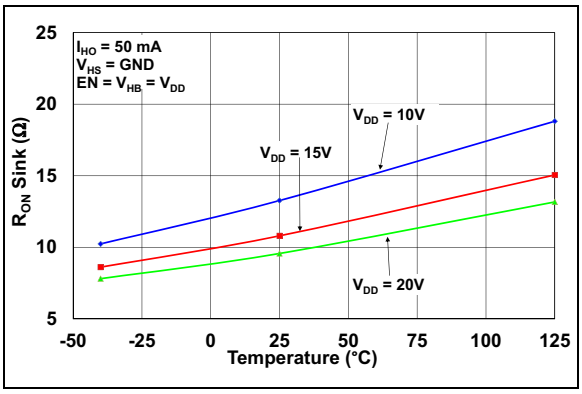


FIGURE 2-12: *HO Output Sink ON-Resistance vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C with 10V ≤ V_{DD} ≤ 20V.

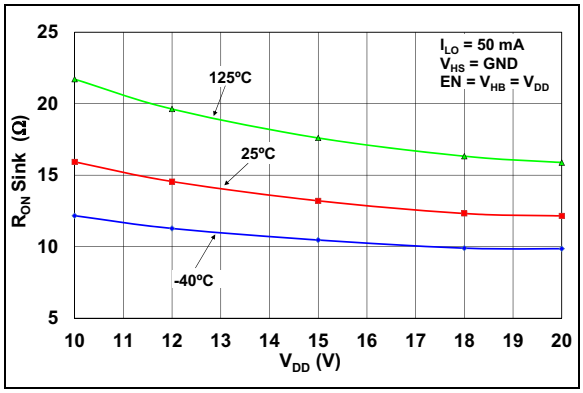


FIGURE 2-13: *LO Output Sink ON-Resistance vs. V_{DD}.*

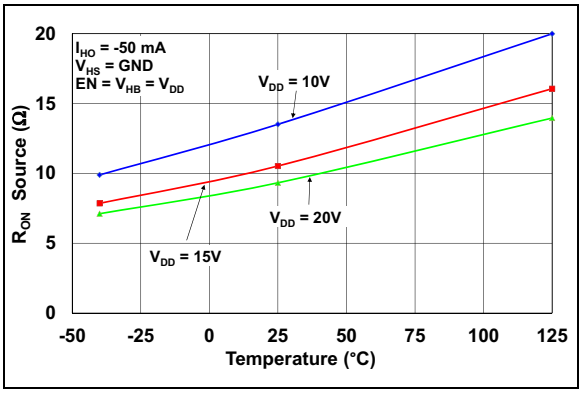


FIGURE 2-16: *HO Output Source ON-Resistance vs. Temperature.*

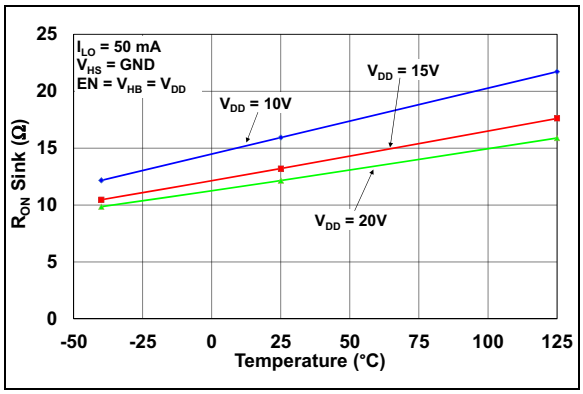


FIGURE 2-14: *LO Output Sink ON-Resistance vs. Temperature.*

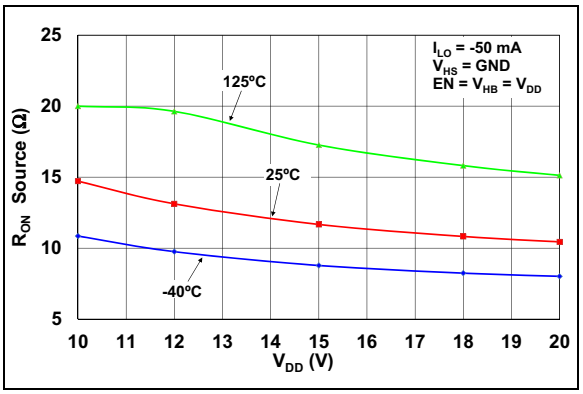


FIGURE 2-17: *LO Output Source ON-Resistance vs. V_{DD}.*

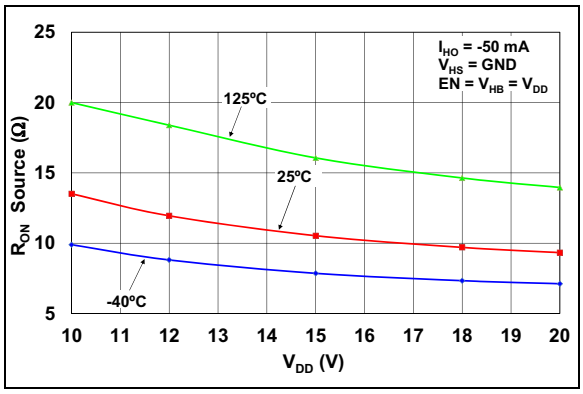


FIGURE 2-15: *HO Output Source ON-Resistance vs. V_{DD}.*

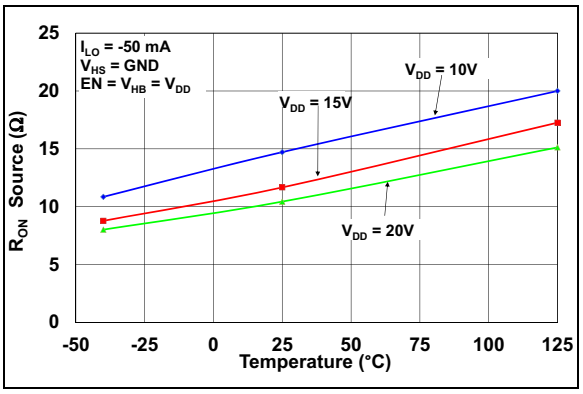


FIGURE 2-18: *LO Output Source ON-Resistance vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C with 10V ≤ V_{DD} ≤ 20V.

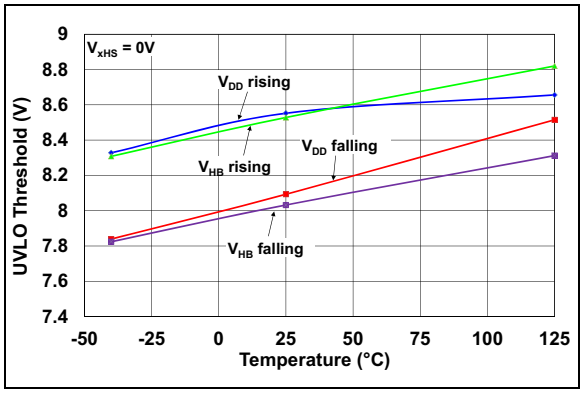


FIGURE 2-19: *V_{DD}/V_{HB} ULVO vs. Temperature.*

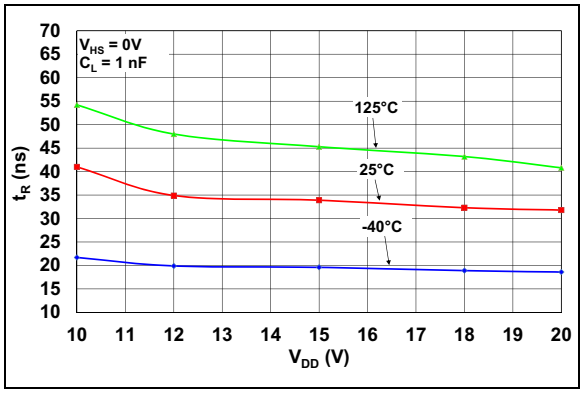


FIGURE 2-22: *HO Rise Time vs. V_{DD} Voltage.*

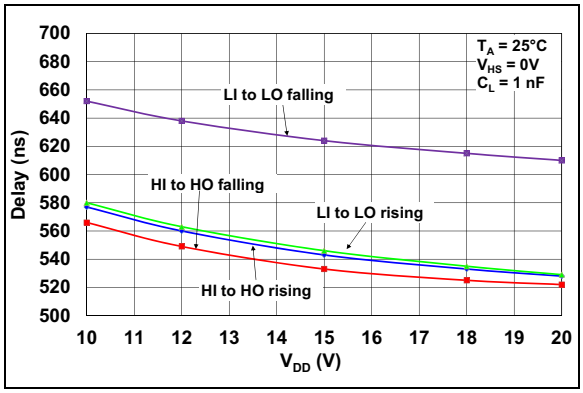


FIGURE 2-20: *Propagation Delay vs. V_{DD} Voltage.*

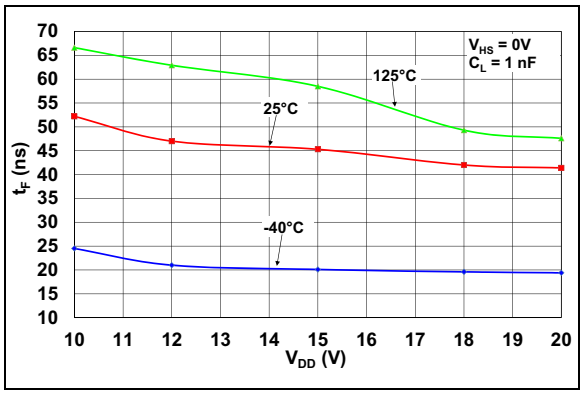


FIGURE 2-23: *HO Fall Time vs. V_{DD} Voltage.*

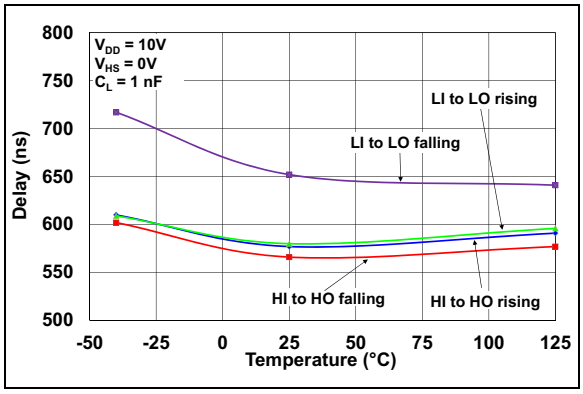


FIGURE 2-21: *Propagation Delay vs. Temperature.*

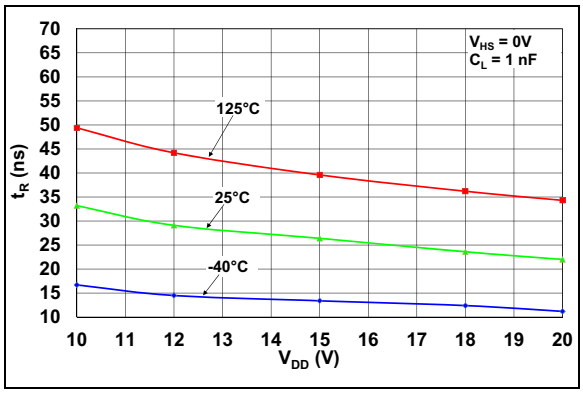


FIGURE 2-24: *LO Rise Time vs. V_{DD} Voltage.*

Note: Unless otherwise indicated, T_A = +25°C with 10V ≤ V_{DD} ≤ 20V.

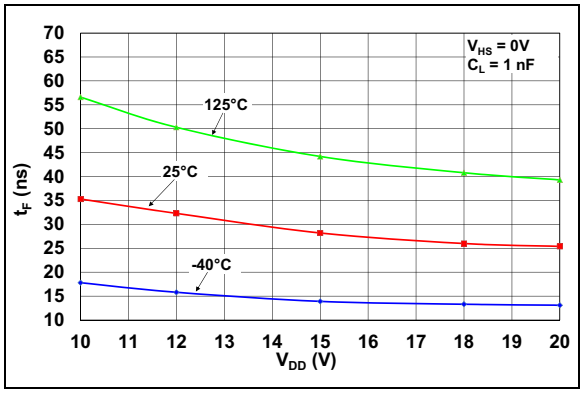


FIGURE 2-25: *LO Fall Time vs. V_{DD} Voltage.*

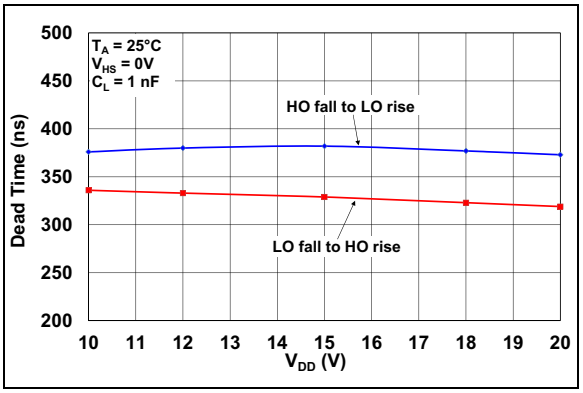


FIGURE 2-28: *Dead Time vs. V_{DD} Voltage.*

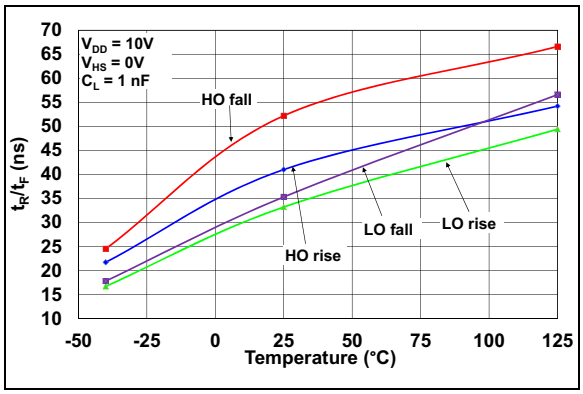


FIGURE 2-26: *Rise/Fall Time vs. Temperature (V_{DD} = 10V).*

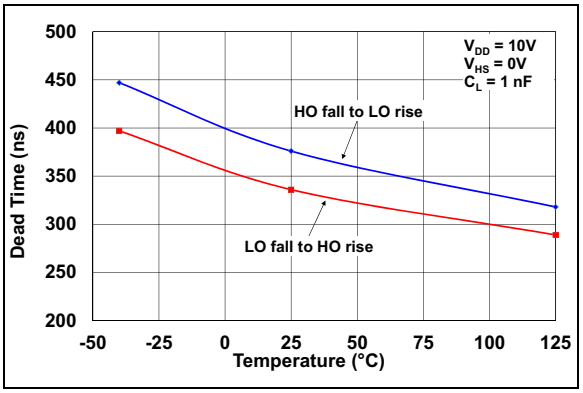


FIGURE 2-29: *Dead Time vs. Temperature (V_{DD} = 10V).*

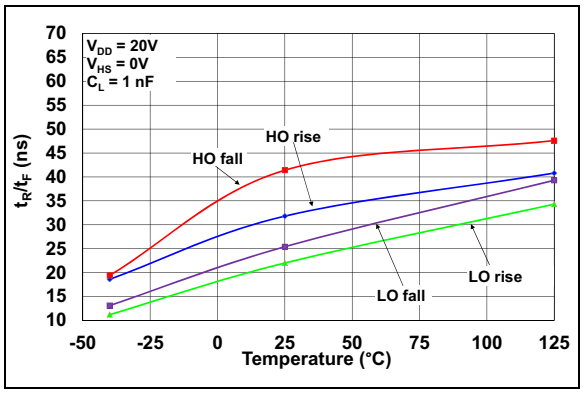


FIGURE 2-27: *Rise/Fall Time vs. Temperature (V_{DD} = 20V).*

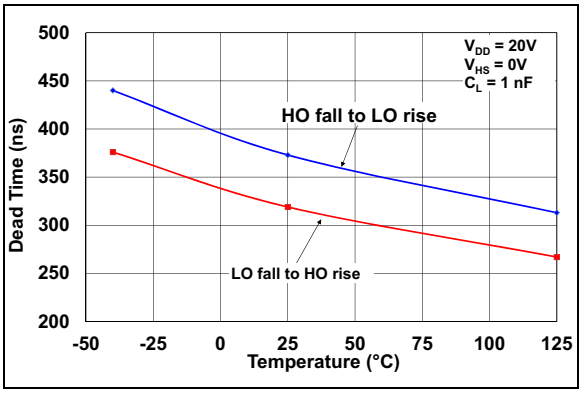


FIGURE 2-30: *Dead Time vs. Temperature (V_{DD} = 20V).*

Note: Unless otherwise indicated, T_A = +25°C with 10V ≤ V_{DD} ≤ 20V.

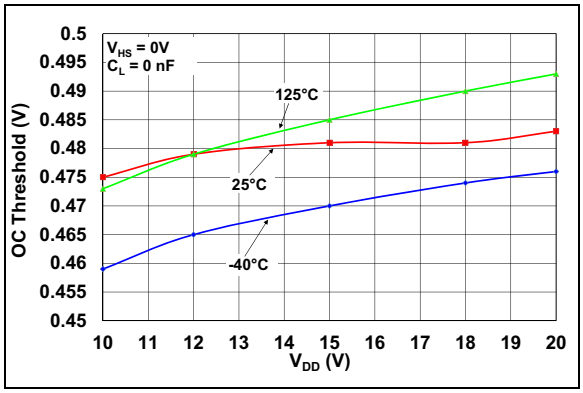


FIGURE 2-31: *Overcurrent Threshold vs. V_{DD} Voltage.*

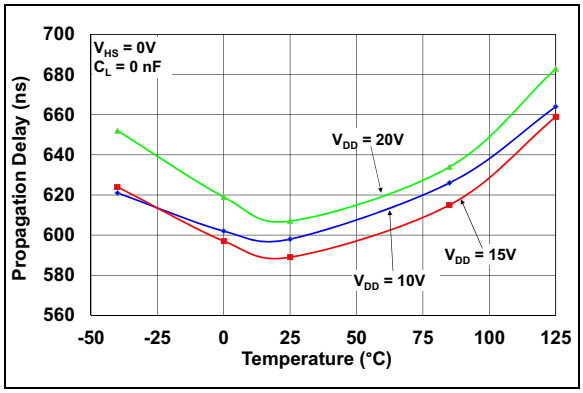


FIGURE 2-34: *Overcurrent Propagation Delay vs. Temperature.*

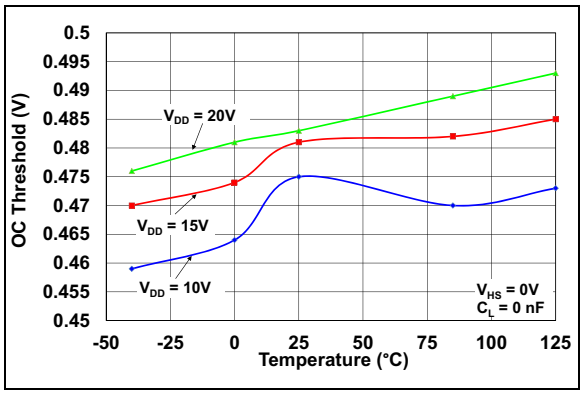


FIGURE 2-32: *Overcurrent Threshold vs. Temperature.*

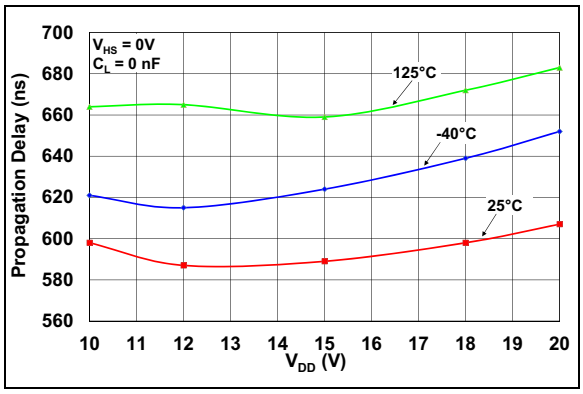


FIGURE 2-33: *Overcurrent Propagation Delay vs. V_{DD} Voltage.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

SOICW-28LD	Symbol	I/O	Description
1	V_{DD}	Power	Input Supply for Gate Drivers Decouple this pin to V_{SS} with a > 2.2 µF capacitor. Connect anode of bootstrap diodes to this pin.
2	AHI	IN	A-Phase High-Side Drive Input
3	BHI	IN	B-Phase High-Side Drive Input
4	CHI	IN	C-Phase High-Side Drive Input
5	ALI	IN	A-Phase Low-Side Drive Input
6	BLI	IN	B-Phase Low-Side Drive Input
7	CLI	IN	C-Phase Low-Side Drive Input
8	$\overline{FAULT}$	OUT	Fault Output Open drain asserts low to indicate Overcurrent or V_{DD} Undervoltage condition.
9	ISNS	IN	Current Sense Input for Overcurrent Shutdown
10	EN	IN	Enable Input Logic high on the Enable pin results in normal operation. Logic low forces the device to enter Shutdown mode.
11	RCIN	OUT	Overcurrent Fault Clear Delay Pin Connect to an external capacitor to set the fault clear delay.
12	V_{SS}	GND	Logic Ground Pin
13	COM	—	Low-Side Driver Return Pin
14	CLO	OUT	C-Phase Low-Side Drive Output Connect to the gate of the external low-side power MOSFET or IGBT.
15	BLO	OUT	B-Phase Low-Side Drive Output Connect to the gate of the external low-side power MOSFET or IGBT.
16	ALO	OUT	A-Phase Low-Side Drive Output Connect to the gate of the external low-side power MOSFET or IGBT.
17, 21, 25	NC	—	No Connect
18	CHS	—	C-Phase High-Side Drive Return Connection Connect to the emitter or source of the external high-side power device. Connect the bootstrap capacitor between this pin and the CHB pin.
19	CHO	OUT	C-Phase High-Side Drive Output Connect to the gate of the external high-side power MOSFET or IGBT.
20	CHB	Power	C-Phase High-Side Bootstrap Supply External bootstrap capacitor is required. Connect the bootstrap capacitor between this pin and CHS. Connect to the anode of the external bootstrap diode.
22	BHS	—	B-Phase High-Side Drive Return Connection Connect to the emitter or source of the external high-side power device. Connect the bootstrap capacitor between this pin and the BHB pin.
23	BHO	OUT	B-Phase High-Side Drive Output Connect to the gate of the external high-side power MOSFET or IGBT.

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

SOICW-28LD	Symbol	I/O	Description
24	BHB	Power	B-Phase High-Side Bootstrap Supply External bootstrap capacitor is required. Connect the bootstrap capacitor between this pin and BHS. Connect to the anode of the external bootstrap diode.
26	AHS	—	A-Phase High-Side Drive Return Connection Connect to the emitter or source of the external high-side power device. Connect the bootstrap capacitor between this pin and the AHB pin.
27	AHO	OUT	A-Phase High-Side Drive Output Connect to the gate of the external high-side power MOSFET or IGBT.
28	AHB	Power	A-Phase High-Side Bootstrap Supply External bootstrap capacitor is required. Connect the bootstrap capacitor between this pin and AHS. Connect to the anode of the external bootstrap diode.

4.0 FUNCTIONAL DESCRIPTION

The MIC4609 is a noninverting, 600V three-phase IGBT/MOSFET driver designed to independently drive six IGBTs or MOSFETs in a three-phase bridge. The MIC4609 offers a wide 10V-to-20V V_{DD} operating supply range with six independent inputs (TTL or 3.3V CMOS compatible).

The driver is comprised of six input buffers with hysteresis, four independent UVLO circuits (three high-side monitoring the HB voltage and one low-side monitoring the V_{DD} voltage), and six output drivers. The high-side output drivers utilize a high-speed level-shifting circuit that is referenced to the HS pin. An overcurrent protection circuit turns off all outputs during an overcurrent fault.

4.1 UVLO Protection

The UVLO circuits force the driver's outputs low until the supply voltage exceeds the UVLO threshold. Hysteresis in the UVLO circuits prevents system noise and finite circuit impedance from causing chatter during turn-on.

The UVLO circuits are illustrated in the functional block diagrams. The low-side UVLO circuit, Functional Block Diagram MIC4609 – Phase x Drive Circuit, monitors the voltage between the V_{DD} and V_{SS} pins. The circuit keeps all the drivers off when V_{DD} is less than the UVLO threshold voltage.

The three high-side UVLO circuits, shown in Typical Application Circuit MIC4609 – 300V, 3-Phase Motor Driver, monitor the voltage between the xHB and xHS pins. The circuit keeps its respective high-side output off when V_{HB} - V_{HS} is less than the UVLO threshold voltage.

4.2 Startup and UVLO

The startup sequence is illustrated in Figure 4-1. As V_{DD} rises above an unspecified threshold, V_T, the internal circuitry becomes active, the $\overline{\text{FAULT}}$ pin asserts low and the UVLO circuitry begins to monitor V_{DD}. When the rising V_{DD} reaches the UVLO threshold, a current source begins charging the RCIN pin's external capacitor until it reaches the RCIN delay threshold. The output drivers are enabled once the RCIN threshold is reached and the EN pin is asserted high.

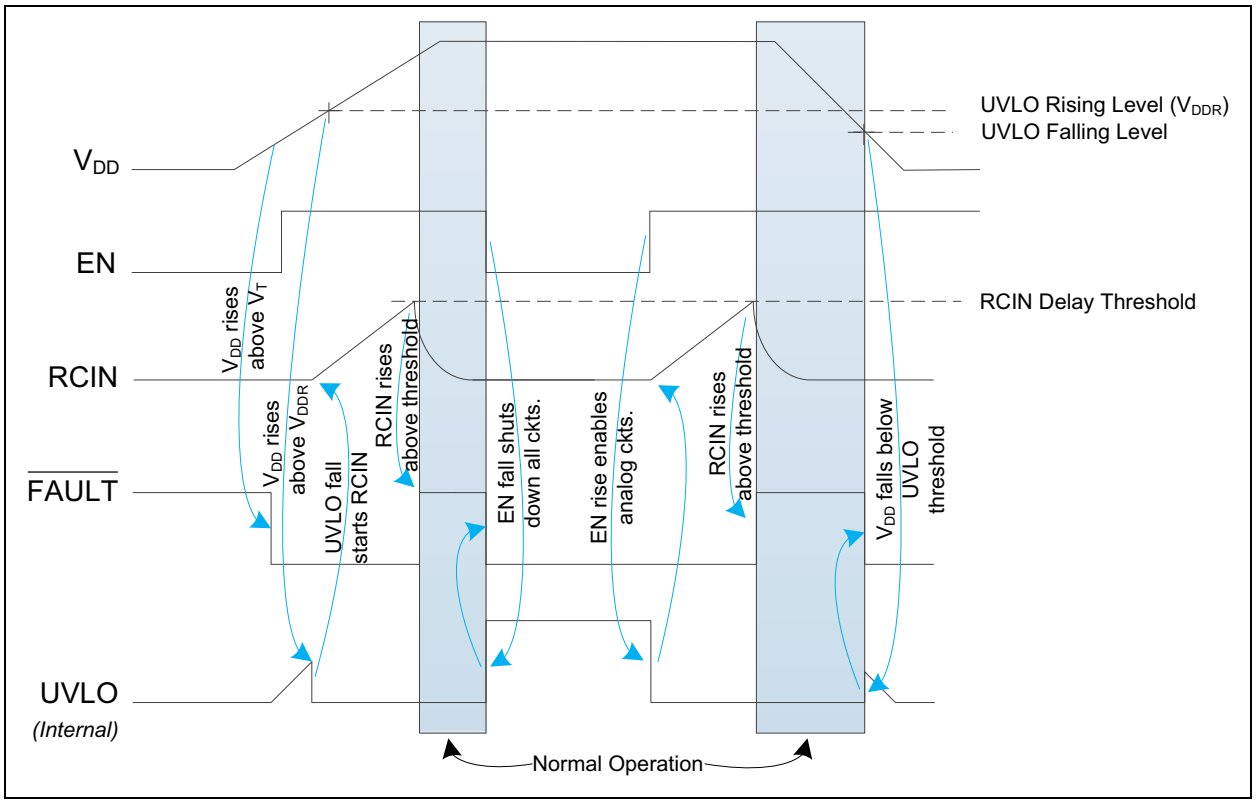


FIGURE 4-1: *Startup and Fault Timing Diagram.*

TABLE 4-1: OPERATIONAL TRUTH TABLE

				ULVO (1, 2)		Outputs (3, 4)	
Condition	**xHI**	**xLI**	**EN**	**HB ULVO**	**V_{DD} ULVO**	**xHO**	**xLO**
Disabled	X	X	L	X	X	L	L
V_{DD} ULVO	X	X	X	X	L	L	L
V_{HB} ULVO	X	L or H	H	L	H	L	L or H
Switching	H	H	⌐¬	H	H	L	L
	H	H	H	⌐¬	⌐¬	L	L
	L	H	H	H	H	L	H
	H	L	H	H	H	H	L
	L	L	H	H	H	L	L

Note 1: UVLO = H when V_{DD} > UVLO threshold

2: UVLO = L when V_{DD} < UVLO threshold

3: xHO and xLO remain low if both xHI and xLI are low when the V_{DD} rises above the UVLO threshold or when the EN pin is asserted high. Normal switching operation begins when one of the inputs changes state from L to H.

4: Anti-shoot-through circuit prevents a high on both outputs simultaneously.

4.3 Enable Inputs

There is one external Enable pin that controls all three phases. A logic high on the enable pin (EN) allows for startup of all phases and normal operation. Conversely, when a logic low is applied on the Enable pin, all phases turn off and the device enters a low current Shutdown mode. All outputs (xHO and xLO) are pulled low when EN is low. The EN pin is internally pulled down. Leaving the pin open disables the part.

4.4 Input Stage

The xHI and xLI pins are referenced to the COM pin and have a CMOS/TTL compatible input range. The input threshold voltage is independent of the V_{DD} supply. The input pin voltage must not exceed the V_{DD} pin voltage. The voltage state of the input signal(s) does not change the quiescent current draw of the driver. The input stage block diagram is shown in Figure 4-2.

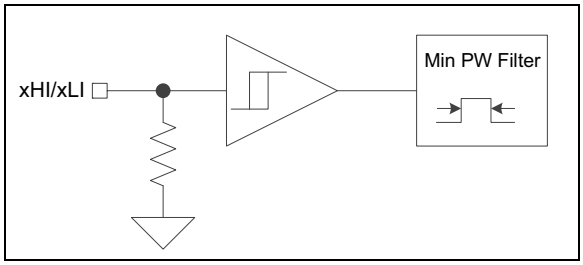


FIGURE 4-2: *Input Stage Block Diagram.*

An internal pull-down resistor is connected to the xHI and xLI pins. This pulls the driver output pins low if the inputs are disconnected or left floating. A small amount of hysteresis is programmed into the input to prevent false triggering of the output. In addition, each input has a minimum pulse-width filter for additional noise immunity protection. The input pulse width must exceed the t_{FLTR} time before the outputs will change state. Refer to the Electrical Characteristics table and Figure 4-3 for additional information.

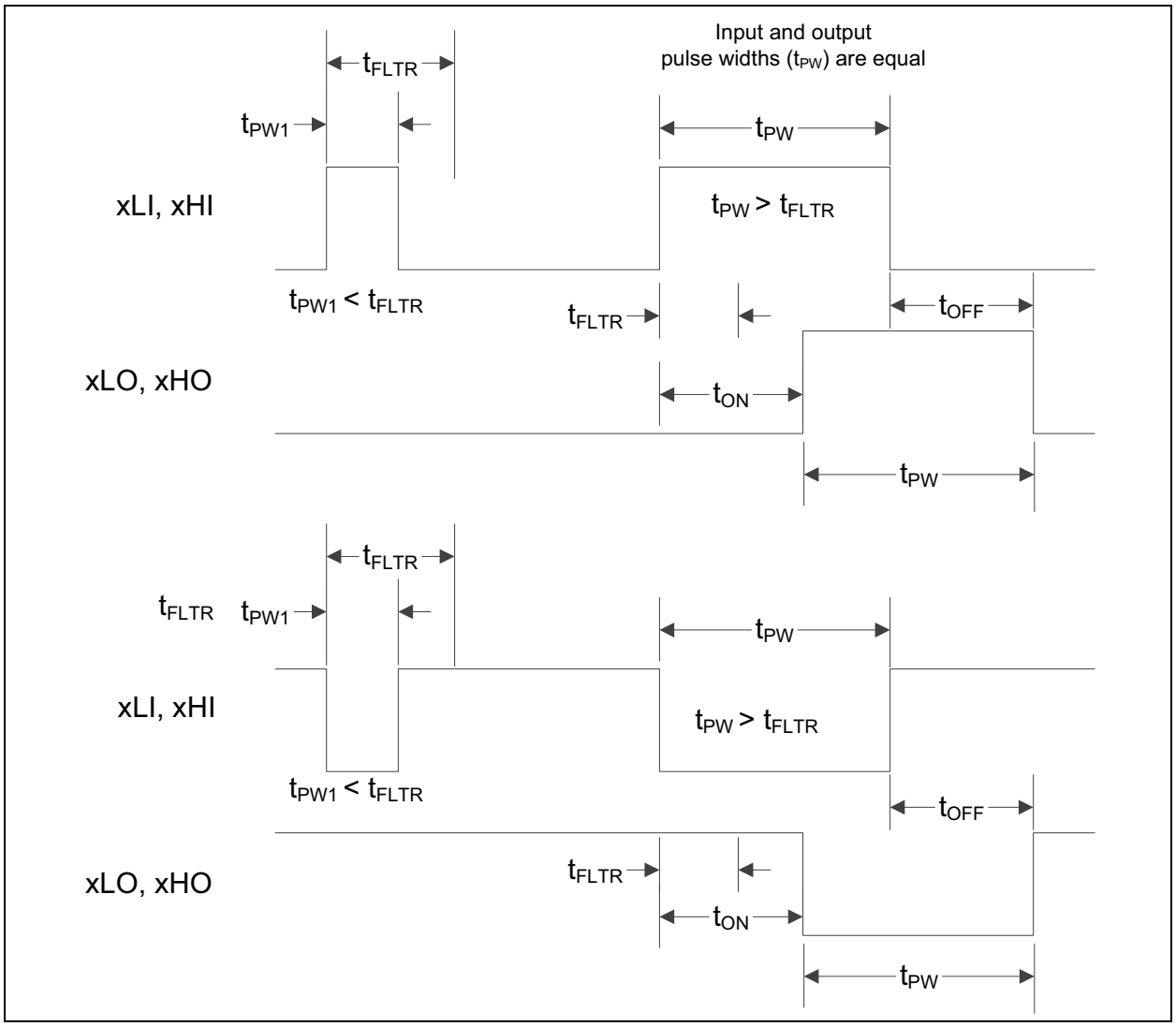


FIGURE 4-3: *Minimum Pulse-Width Diagram.*

4.5 Dead Time and Anti-Shoot-Through Protection

Shoot-through occurs when both the high and low-side IGBTs/MOSFETs of a particular phase are ON at the same time. The inputs of each phase use anti-shoot-through circuitry to prevent this condition from occurring. If both the HI and LI inputs of a phase go high, both outputs (HO and LO) of that phase go low.

In addition to anti-shoot-through circuitry, a fixed "dead-time" delay is added to the input-to-output propagation delay. This allows the IGBTs/MOSFETs in a particular phase to fully turn off before the other turns on.

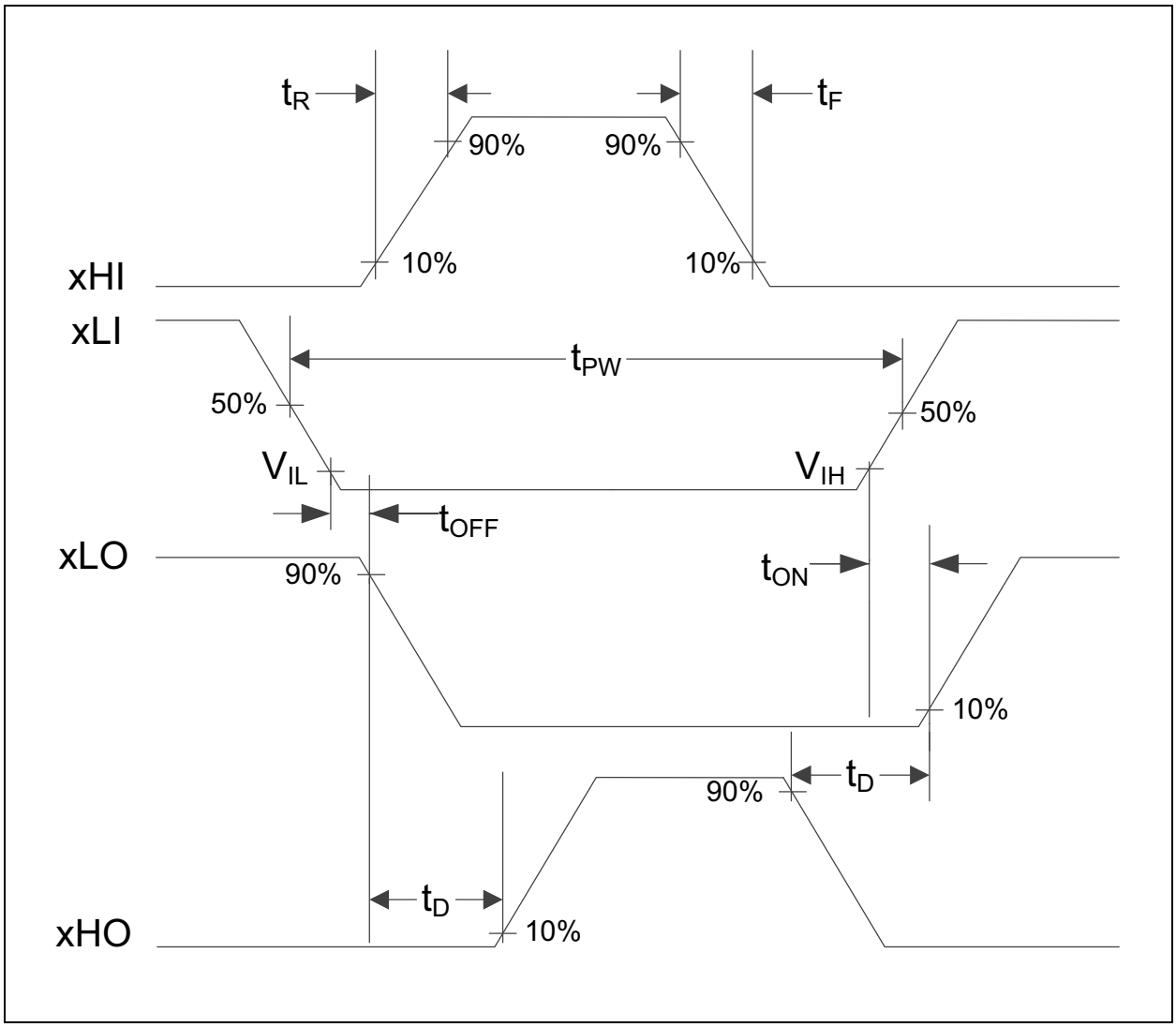


FIGURE 4-4: *Dead Time, Propagation Delay, and Rise/Fall-Time Diagram.*

4.6 Low-Side Driver Output Stage

The low-side driver, shown in Figure 4-5, is designed to drive an N-channel MOSFET or IGBT. The driver is referenced to the COM pin, which can be floating with respect to ground. The COM reference gives the gate drive currents a return path without having to flow through the current sense resistor.

Low driver impedances allow the external IGBT/MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low V_{CE} or R_{DSON} from the external power device.

When driving the external IGBT on, the driver's internal P-channel MOSFET is turned on and V_{DD} is applied to the gate of the external IGBT. To turn off the external IGBT, the driver's N-channel FET is turned on, which discharges the external IGBT's gate.

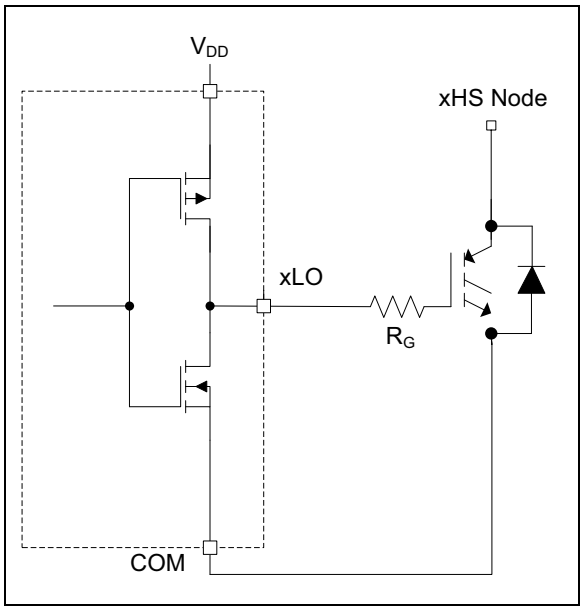


FIGURE 4-5: *Low-Side Driver Block Diagram.*

4.7 High-Side Driver and Bootstrap Circuit

The High-Side driver is designed to drive a floating N-channel FET or IGBT, whose source/emitter terminal is referenced to the HS pin. A simplified diagram of the high-side driver section is shown in Figure 4-6.

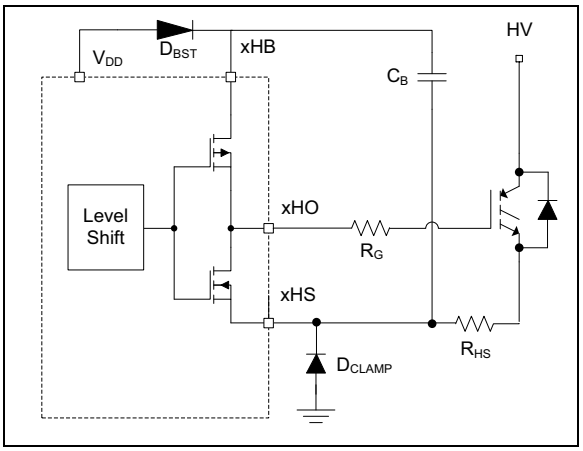


FIGURE 4-6: *High-Side Driver and Bootstrap Circuit Block Diagram.*

A low-power, high-speed, level-shifting circuit isolates the low-side (V_{SS} pin) referenced circuitry from the high-side (xHS pin) referenced driver. Power to the high-side driver and UVLO circuit is supplied by the bootstrap capacitor (C_B) while the voltage level of the xHS pin is shifted high.

The bootstrap circuit consists of an external diode, D_{BST}, and an external capacitor, C_B. In a typical application, such as the motor driver shown in Figure 4-7 (Phase A illustrated only), the AHS pin is at ground potential while the low-side MOSFET is ON. The internal diode charges capacitor C_B to $V_{DD} - V_F$ during this time (where V_F is the forward voltage drop of the internal diode). After the low-side MOSFET is turned off and the AHO pin turns on, the voltage across capacitor C_B is applied to the gate of the high-side external MOSFET. As the high-side MOSFET turns on, voltage on the AHS pin rises with the source of the high-side MOSFET until it reaches V_{DD}. As the AHS and AHB pins rise, the internal diode is reverse biased, preventing capacitor C_B from discharging. During this time, the high-side MOSFET is kept ON by the voltage across capacitor C_B.

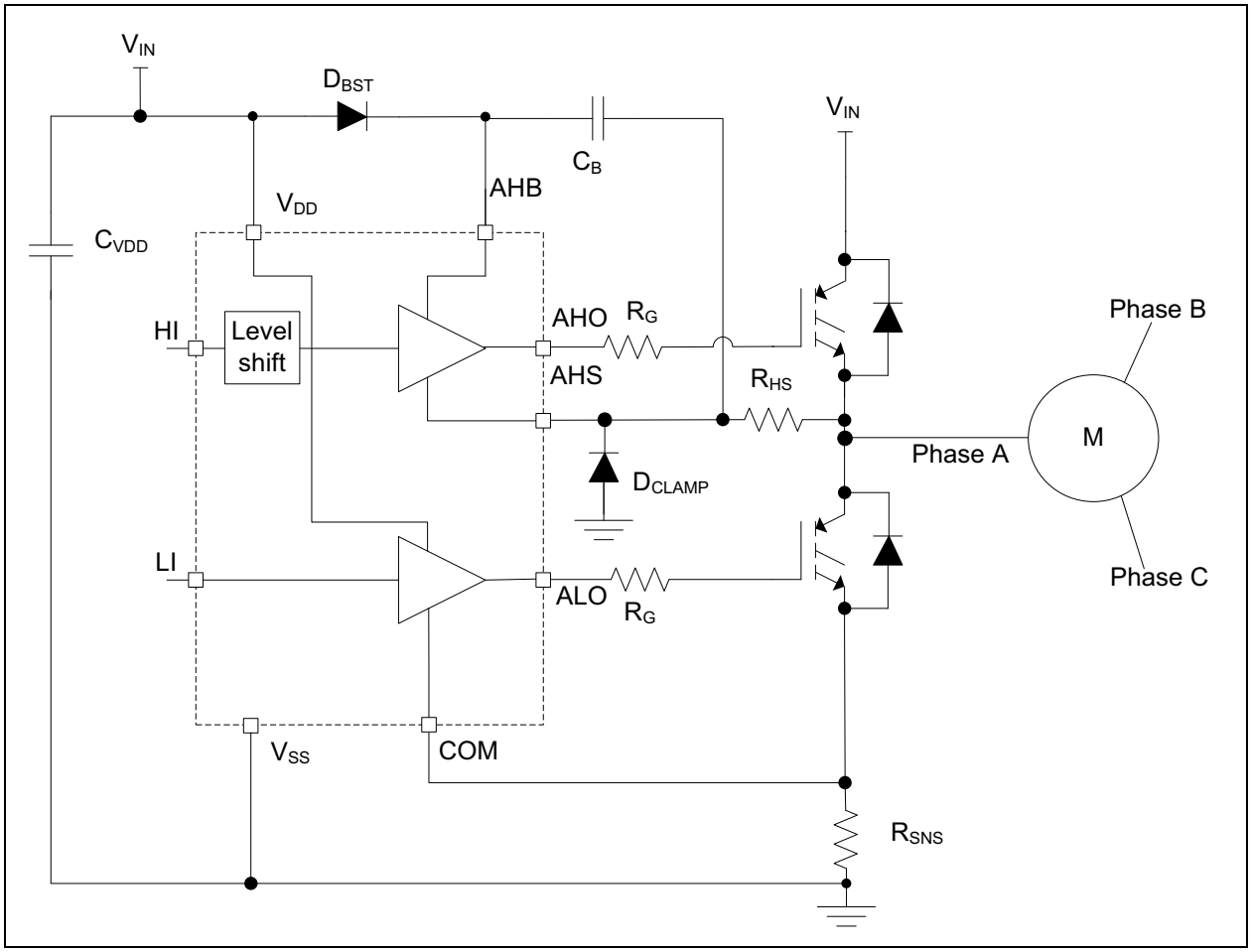


FIGURE 4-7: *MIC4609 Motor Driver Typical Application – Phase A.*

4.8 Overcurrent Protection Circuitry

The MIC4609 provides overcurrent protection for the 3-phase bridge. It consists of:

- a comparator that senses the voltage across a current-sense resistor
- a latch and timer that keep all gate drivers off during a fault
- an open-drain $\overline{\text{FAULT}}$ pin that pulls low during the fault.

Figure 4-8 illustrates the overcurrent protection sequence. When an overcurrent condition is detected, the $\overline{\text{FAULT}}$ pin is pulled low and a latch disables the gate drive outputs for a time determined by the RCIN pin capacitor. After the delay circuit times out, the latch is reset, the $\overline{\text{FAULT}}$ pin is deasserted to a high impedance state and the gate drive outputs are re-enabled.

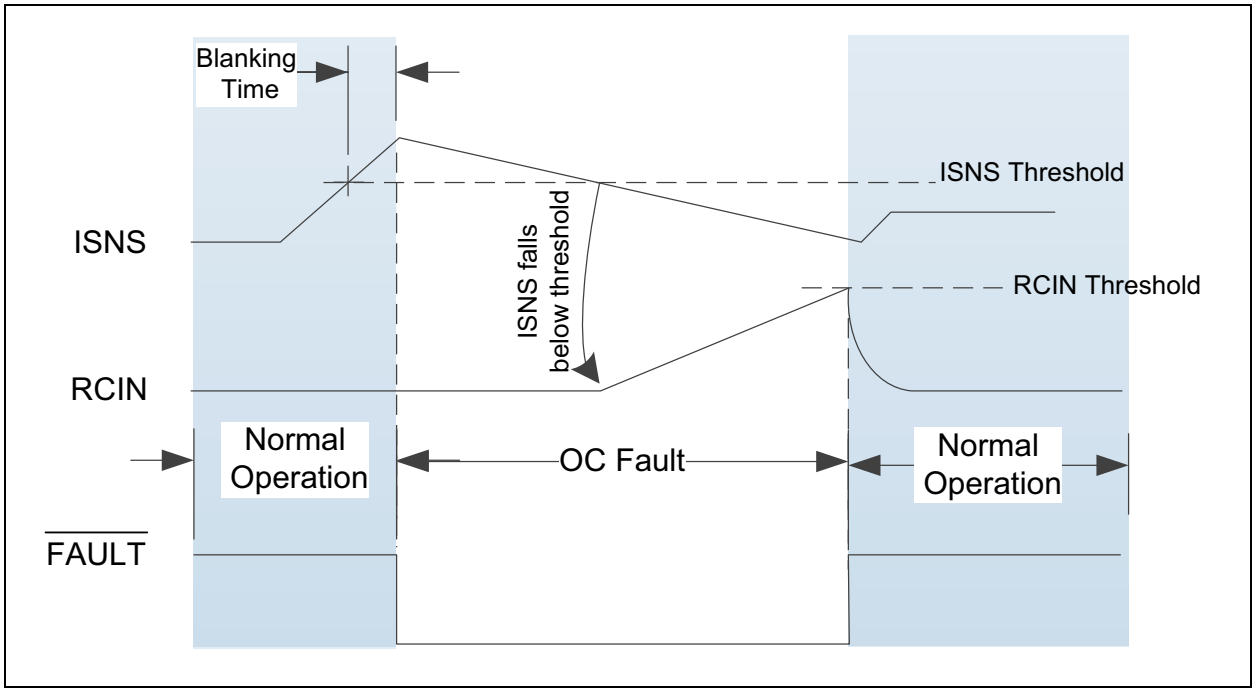


FIGURE 4-8: *Overcurrent Fault Sequence.*

4.8.1 ISNS

The ISNS pin may be used to monitor motor winding currents. The measurement is referenced to the V_{SS} pin and can sense the voltage across a low-side current sense resistor or it may be connected to a current sense transformer. The current sense resistor is typically connected between the source pins (MOSFET) or emitter pins (IGBT) of all three low-side switches and power ground.

If the peak voltage on the ISNS pin exceeds the V_{ISNS} threshold, it will cause all six outputs to latch off. A blanking circuit on the ISNS comparator output prevents noise from falsely tripping the overcurrent circuit. The ISNS pin is internally pulled down to V_{SS} but may be externally connected to V_{SS} ground for improved noise immunity if the overcurrent feature is not used.

4.8.2 RCIN

A capacitor connected to the RCIN pin determines the amount of time the gate drive outputs are latched off before they can be restarted.

During normal operation, the RCIN pin is internally pulled low. Once an overcurrent condition is detected, the RCIN pin capacitor is charged up by an internal current source until the voltage reaches the V_{RCIN+} threshold and the latch is reset. The outputs are then enabled.

The delay time can be approximated by applying Equation 4-1.

EQUATION 4-1:

$$t_{DLY} = \frac{C_{RCIN} \times V_{RCIN+}}{I_{RCIN}}$$

Where:

C_{RCIN}	=	External capacitance on the RCIN pin
I_{RCIN}	=	RCIN pin current source (typically 0.44 µA)
V_{RCIN+}	=	Internal comparator threshold

4.8.3 $\overline{\text{FAULT}}$

This open-drain output is asserted low for an overcurrent condition or when the V_{DD} voltage is below the UVLO threshold. It will de-assert to a high-impedance state once the V_{DD} rises above the UVLO threshold or when the RCIN pin voltage has reached the V_{RCIN+} threshold. During normal operation, the internal pull-down MOSFET of the pin is high impedance. A pull-up resistor must be connected to this pin.

5.0 APPLICATION INFORMATION

5.1 Bootstrap Circuit

The high-side gate drive cannot be operated continuously (100% duty cycle). It must be periodically turned off to refresh/recharge the bootstrap capacitor, C_B. There are two separate requirements to consider when choosing the bootstrap capacitor value:

- IGBT or MOSFET gate charge
- Duration of the high-side switch on-time

The high-side bootstrap circuit for Phase A is illustrated in Figure 5-1.

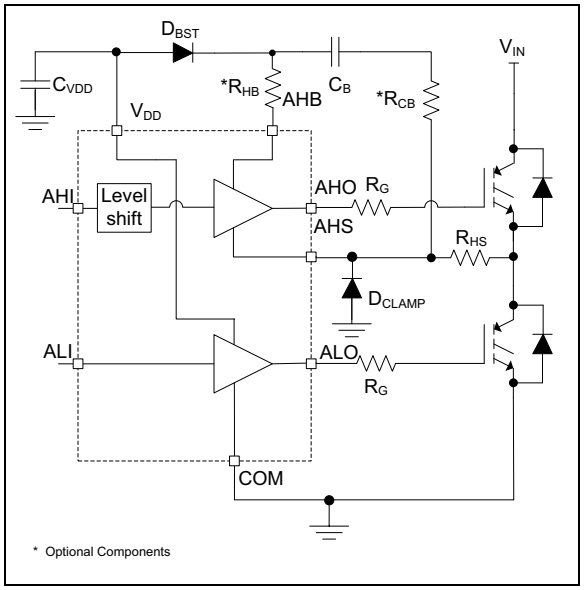


FIGURE 5-1: *MIC4609 – Bootstrap Circuit.*

The bootstrap capacitor voltage drops each time it delivers charge to turn on the IGBT. The voltage drop depends on the gate charge required by the IGBT. Most IGBT and MOSFET specifications contain gate charge versus V_{GE} or V_{GS} voltage information or graphs. Based on this information and a recommended ΔV_{HB} of 0.1V to 0.5V, the minimum value of bootstrap capacitance is calculated by applying Equation 5-1.

EQUATION 5-1:

$$C_B \geq \frac{Q_{GATE}}{\Delta V_{HB}}$$

Where:

Q_{GATE}	=	Total gate charge at V_{HB}
ΔV_{HB}	=	Voltage drop at the HB pin

After the high-side switch has turned on, the bootstrap capacitor will continue to discharge due to leakage currents in the bootstrap capacitor, the IGBT/MOSFET gate-to-source and the driver (HS-pin-to-ground leakage).

Typical leakage currents for the bootstrap capacitor and IGBT/MOSFET are in the 100 nA range. The MIC4609 HS-pin-to-driver leakage current is generally higher with typical values in the 1 µA range (or higher at high junction temperature and voltage). The minimum value of bootstrap capacitor that prevents an excessive drop in the gate drive voltage to the high-side switch is calculated as per Equation 5-2.

EQUATION 5-2:

$$C_B \geq \frac{t_{ON} \times I_{discharge}}{\Delta V_{HB}}$$

Where:

t_{ON}	=	Maximum ON-time of the high-side switch
ΔV_{HB}	=	Voltage drop at the HB pin
$I_{discharge}$	=	Total discharge current at the HB pin (capacitor, IGBT/MOSFET, and HB pin)

Resistors R_{HB} and R_{CB} can be used to reduce the peak C_B charge current or modify the high-side IGBT/MOSFET turn-on time. This helps reduce noise and EMI as well as ripple on the V_{DD} pin.

The resistor in series with the HB pin, R_{HB}, controls the turn-on time of the high-side switch by limiting the charge current into the gate.

Adding a resistor in series with capacitor C_B will reduce the peak charging current drawn through diode D_{BST}. It has some effect on slowing down the high-side switch turn-on time, however, it is not as effective as resistor R_{HB} since charging current also comes from V_{DD} until the high-side switch starts to turn on and raise the voltage on the HB node.

5.2 HS Node Clamp

A resistor/diode clamp between the switching node and the HS pin is recommended to minimize large negative glitches or pulses on the HS pin.

As shown in Figure 5-2, the high-side and low-side IGBTs turn on and off to regulate motor speed. During the on-time, when the high-side IGBT is conducting, current flows into the motor. After the high-side IGBT turns off, and before the low-side IGBT turns on, there is a brief period of time (dead time) that prevents both IGBTs from being ON at the same time. During the dead time, current from the motor flows through the diode in parallel with the low-side IGBT. Depending on the diode characteristics (V_F and turn-on time), the motor current and circuit parasitics, the initial negative voltage on the switch node can be several volts or more.

Even though the HS pin is rated for negative voltage, it is good practice to clamp the HS pin with a resistor and diode to prevent excessive negative voltage from damaging the driver. Depending on the application and

amount of negative voltage on the switch node, a 1A fast recovery diode and a minimum 10Ω resistor are recommended. A higher current diode and/or larger values of resistance can be used if necessary.

Adding a series resistor in the switch node limits the peak high-side driver current, which affects the switching speed of the high-side driver. The resistor, in series with the HO pin, may be reduced to help compensate for the extra HS pin resistance.

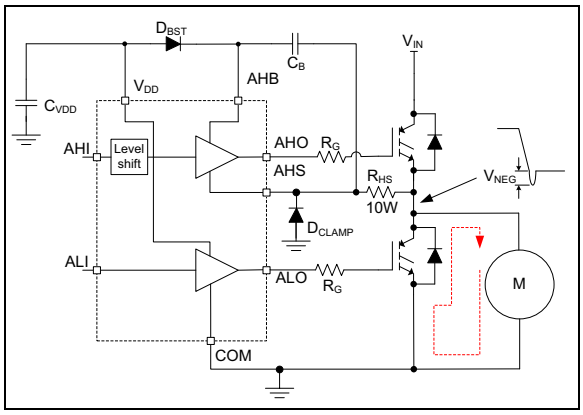


FIGURE 5-2: *Negative HS Pin Voltage.*

5.3 Power Dissipation Considerations

Power dissipation in the driver can be separated into two areas:

- Gate driver dissipation
- Quiescent current dissipation used to supply the internal logic and control functions

5.3.1 GATE DRIVER POWER DISSIPATION

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate-to-emitter and gate-to-collector capacitance of the external IGBT. Figure 5-3 shows a simplified equivalent circuit of the MIC4609 driving an external high-side IGBT.

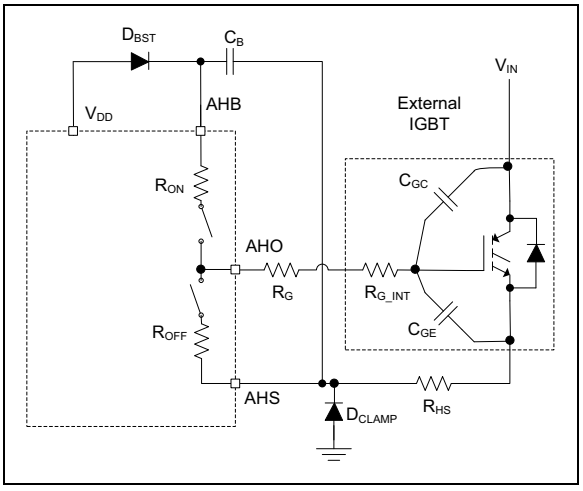


FIGURE 5-3: *MIC4609 High-Side Driving an External IGBT.*

5.3.2 DISSIPATION DURING THE EXTERNAL IGBT/MOSFET TURN-ON

Energy from capacitor C_B is used to charge up the input capacitance of the IGBT (C_{GE} and C_{GC}). The energy delivered to the gate is dissipated in the three resistive components, R_{ON}, R_G and R_{G_INT}. R_G is the series resistor between the driver output and the IGBT. R_{G_INT} is the gate resistance of the IGBT. R_{G_INT} is usually listed in the IGBT or MOSFET specifications. The ESR of capacitor C_B and the resistance of the connecting etch can be ignored since they are much less than R_{ON} and R_{G_INT}.

The effective capacitances of C_{GE} and C_{GC} are difficult to calculate because they vary nonlinearly with I_C, V_{GE}, and V_{CE}. Most power IGBT and MOSFET specifications include a graph of total gate charge versus V_{GE}. Figure 5-4 shows a typical gate charge curve for an arbitrary IGBT. The chart shows that for a gate voltage of 12V, the IGBT requires 12 nC of charge.

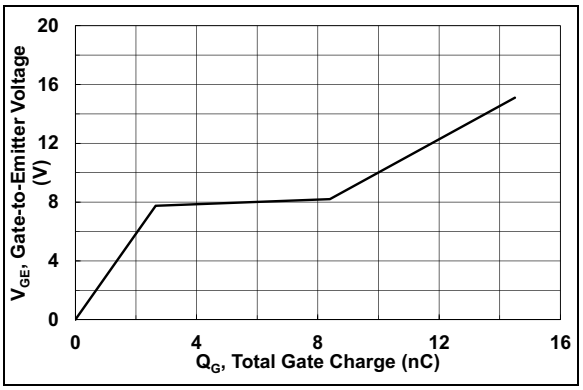


FIGURE 5-4: *Typical Gate Charge vs. V_{GE}.*

The power dissipated by the resistive components of the gate drive circuit during turn-on is calculated as shown in Equation 5-3.

EQUATION 5-3:

$$P_{DRIVER} = Q_G \times V_{GE} \times f_S \times D$$

Where:

P_{DRIVER} (1)	=	Average drive circuit power due to switching
Q_G	=	Total gate charge at V_{GE}
V_{GE}	=	Gate-to-emitter voltage on the IGBT
f_S	=	Switching frequency of the gate drive circuit
D (2)	=	Operating duty cycle of the driver output

Note 1: P_{DRIVER} is the power dissipated by the individual driver for one of the six gate drive outputs.

2: Operating duty cycle is the percentage of time that particular driver output is switching during one rotation of the motor.

The power dissipated by each of the internal gate drivers (high-side or low-side) is equal to the ratio of R_{ON} and R_{OFF} to the external resistive losses in R_G and R_{G_INT}.

Letting R_{ON} = R_{OFF}, the power dissipated in the individual driver output in the IC is calculated as shown in Equation 5-4:

EQUATION 5-4:

$$P_{DISS} = P_{DRIVER} \times \frac{R_{ON}}{R_{ON} + R_G + R_{G\_INT}}$$

The total power dissipated in the MIC4609, due to switching, is equal to the sum of all six driver dissipations.

5.3.3 SUPPLY CURRENT POWER DISSIPATION

Power is dissipated in the MIC4609 even if nothing is being driven. The supply current is drawn by the bias for the internal circuitry, the level shifting circuitry, and shoot-through current in the output drivers. The supply current is proportional to the operating frequency and the V_{DD} and V_{HB} voltages. Figures 2-9 and 2-10 show how supply current varies with switching frequency and supply voltage.

The power dissipated by the MIC4609 due to supply current is calculated by applying Equation 5-5.

EQUATION 5-5:

$$P_{DISS\_SUPPLY} = V_{DD} \times I_{DD} \times V_{HB} \times I_{HB}$$

5.3.4 TOTAL POWER DISSIPATION AND THERMAL CONSIDERATIONS

Total power dissipation in the MIC4609 is equal to the power dissipation caused by driving the external IGBTs and the supply current. Equation 5-6 shows this relation.

EQUATION 5-6:

$$P_{DISS\_TOTAL} = P_{DISS\_SUPPLY} + \sum P_{DISS\_DRIVERS}$$

The die temperature can be calculated after the total power dissipation is determined as shown in Equation 5-7.

EQUATION 5-7:

$$T_J = T_A + P_{DISS\_TOTAL} \times \theta_{JA}$$

Where:

T_A	=	Maximum ambient temperature (°C)
T_J	=	Junction temperature (°C)
P_{DISS_TOTAL}	=	MIC4609 power dissipation (W)
θ_{JA}	=	Thermal resistance from junction-to-ambient air (°C/W)

5.3.5 OTHER TIMING CONSIDERATIONS

Make sure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high-side on-time to switching period) is controlled by the minimum pulse width of the low side and by the time required for the C_B capacitors to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned on.

5.4 Decoupling Capacitor Selection

Decoupling capacitors are required on the V_{DD} pin to supply the charge necessary to drive the external IGBTs or MOSFETs and also to minimize the voltage ripple on these pins. The V_{DD} pin decoupling capacitor supplies the transient current for all six drivers (three high-side and three low-side). The minimum recommended V_{DD} capacitance should be greater than the sum of all three C_B capacitors with a minimum 1 µF ceramic capacitor regardless of C_B value.

Ceramic capacitors are recommended because of their low impedance and small size. Z5U-type ceramic capacitor dielectrics should not be used due to the large change in capacitance over temperature and voltage. Larger IGBTs/MOSFETs and low-switching frequencies may require larger capacitance values for proper operation. The voltage rating of the capacitors depends on the supply voltage, ambient temperature and the voltage derating used for reliability. 25V-rated X5R or X7R ceramic capacitors are recommended for most applications. The minimum capacitance value should be increased if low voltage capacitors are used because even good quality dielectric capacitors, such as X5R, will lose 40% to 70% of their capacitance value at the rated voltage.

Placement of the decoupling capacitors is critical. The bypass capacitor for V_{DD} should be placed as close as possible between the V_{DD} pin and the ground plane. The bypass capacitor (C_B) for the HB supply pin must be located as close as possible between the HB and HS pins. The etch connections must be short, wide, and direct. The use of a ground plane to minimize connection impedance is recommended.

5.5 Grounding, Component Placement and Circuit Layout

Nanosecond switching speeds and high-peak currents in and around the MIC4609 driver requires proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching, excessive ringing, or circuit latch-up.

Figure 5-5 shows the critical current paths when the driver outputs go high and turn on the external IGBTs. It also helps demonstrate the need for a low impedance ground plane. Charge needed to turn on the IGBT gates comes from the decoupling capacitors C_{VDD} and C_B. Current in the low-side gate driver flows from C_{VDD} through the internal driver, into the IGBT gate, and out the emitter. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the emitter of the IGBT. This voltage works against the gate drive voltage and can either slow down or turn off the IGBT during the period when it should be turned on.

Current in the high-side driver is sourced from capacitor C_B and flows into the HB pin and out the HO pin, into the gate of the high-side IGBT. The return path for the current is from the emitter of the IGBT and back to capacitor C_B. The high-side circuit return path usually does not have a low-impedance ground plane so the etch connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the IGBT emitter and the decoupling capacitor causes negative voltage feedback that fights the turn-on of the IGBT.

It is important to note that capacitor C_B must be placed close to the HB and HS pins. This capacitor not only provides the current for turn-on but it must also keep HB pin noise and ripple low for proper operation of the high-side drive circuitry.

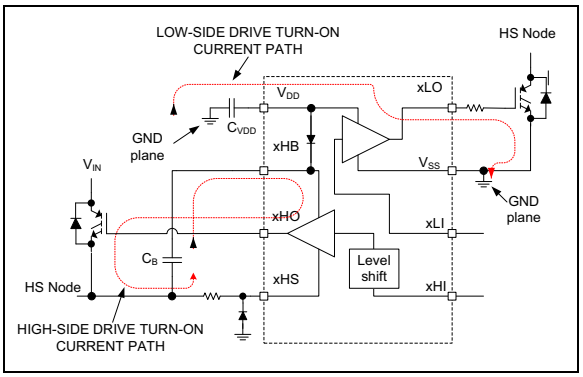


FIGURE 5-5: *Turn-On Current Paths.*

Figure 5-5 shows the critical current paths when the driver outputs go low and turn off the external IGBTs. Short, low-impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current flowing through the internal diode replenishes charge in the bootstrap capacitor, C_B.

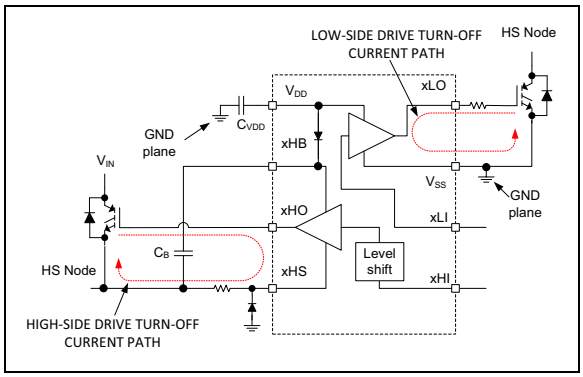
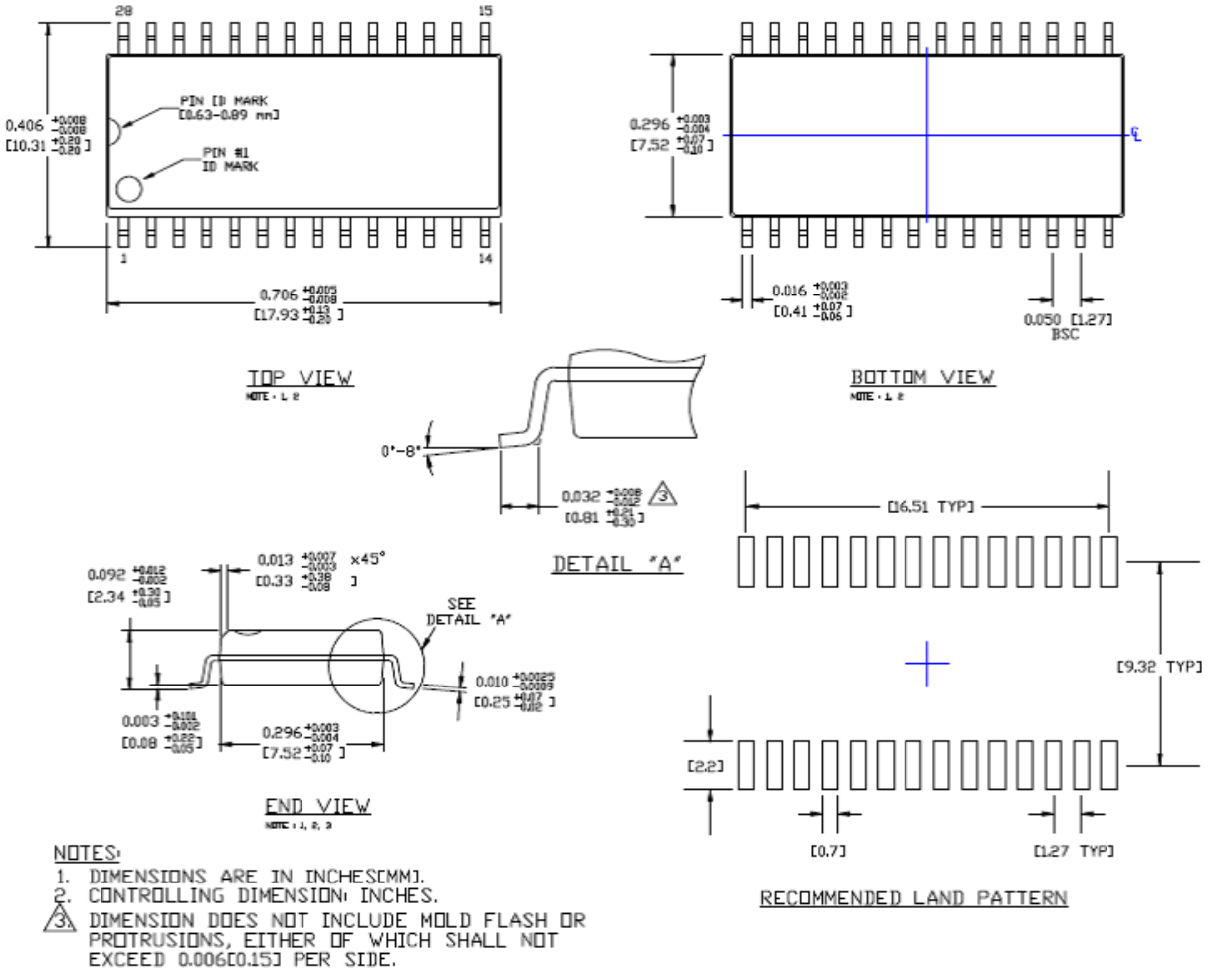


FIGURE 5-6: *Turn-Off Current Paths.*

It is highly recommended to use a ground plane to minimize parasitic inductance and impedance of the return paths. The MIC4609 is capable of greater than 1A peak currents and any impedance between the MIC4609, the decoupling capacitors, and the external IGBTs/MOSFETs will degrade the performance of the driver.

6.0 PACKAGING INFORMATION

DRAWING #	SOICW-28LD-PL-1	UNIT	INCH [MM]



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.

APPENDIX A: REVISION HISTORY

Revision A (March 2016)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	–X (1)
Device	Lead Finish	Package Code	Tape and Reel Option

Device:	MIC4609:		600V 3-Phase MOSFET/IGBT Driver
Lead Finish:	Y	=	Pb-Free with Industrial Temperature Grade
Package Code:	WM	=	Plastic Small Outline, 7.52 mm Body, 28-Lead SOIC Wide Package

Examples:

a) MIC4609YWM-TR: 600V 3-Phase MOSFET/IGBT Driver, 7.52 mm body, 28LD SOIC Wide package, Tape and Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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