



SCCS053 - March 1997 - Revised March 2000

CY74FCT163373

16-Bit Latch

Features

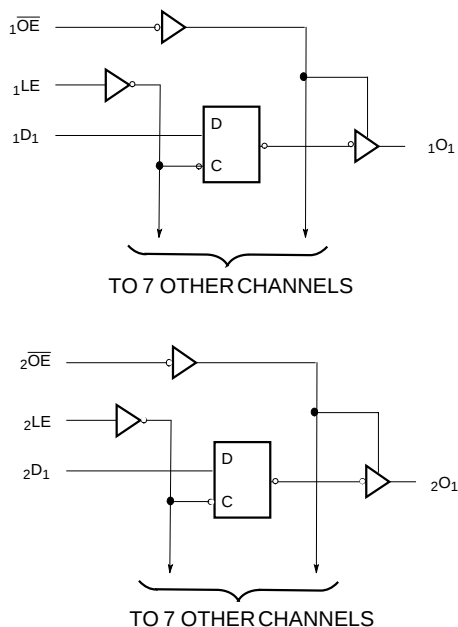
- Low power, pin-compatible replacement for LCX and LPT families
- 5V tolerant inputs and outputs
- 24 mA balanced drive outputs
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for reduced noise
- FCT-C speed at 4.2 ns
- Latch-up performance exceeds JEDEC standard no. 17
- Typical output skew < 250 ps
- Industrial temperature range of -40°C to $+85^{\circ}\text{C}$
- TSSOP (19.6-mil pitch) or SSOP (25-mil pitch)
- Typical V_{olp} (ground bounce) performance exceeds Mil Std 883D
- $V_{\text{CC}} = 2.7\text{V}$ to 3.6V
- ESD (HBM) > 2000V

Functional Description

This device is a 16-bit, D-type latch, designed for use in bus applications requiring high speed and low power. It can either be used as two independent 8-bit latches, or as a single 16-bit latch by connecting the Output Enable ($\overline{\text{OE}}$) and Latch (LE) inputs. The outputs are 24-mA balanced output drivers with current limiting resistors to reduce the need for external terminating resistors and provide for minimal undershoot and reduced ground bounce. Flow-through pinout and small shrink packaging aid in simplifying board layout.

The CY74FCT163373 is designed with inputs and outputs capable of being driven by 5.0V buses, allowing its use in mixed voltage systems as a translator. The outputs are also designed with a power off disable feature enabling its use in applications requiring live insertion.

Logic Block Diagrams CY74FCT163373



Pin Configuration

SSOP/TSSOP Top View			
$\overline{1\text{OE}}$	1	48	1LE
1O_1	2	47	1D_1
1O_2	3	46	1D_2
GND	4	45	GND
1O_3	5	44	1D_3
1O_4	6	43	1D_4
V_{CC}	7	42	V_{CC}
1O_5	8	41	1D_5
1O_6	9	40	1D_6
GND	10	39	GND
1O_7	11	38	1D_7
1O_8	12	37	1D_8
2O_1	13	36	2D_1
2O_2	14	35	2D_2
GND	15	34	GND
2O_3	16	33	2D_3
2O_4	17	32	2D_4
V_{CC}	18	31	V_{CC}
2O_5	19	30	2D_5
2O_6	20	29	2D_6
GND	21	28	GND
2O_7	22	27	2D_7
2O_8	23	26	2D_8
2OE	24	25	2LE

Pin Description

Name	Description
D	Data Inputs
LE	Latch Enable Inputs (Active HIGH)
$\overline{OE}$	Output Enable Inputs (Active LOW)
O	Three-State Outputs

Function Table^[1]

Inputs			Outputs
D	LE	$\overline{OE}$	O
H	H	L	H
L	H	L	L
X	L	L	Q ₀
X	X	H	Z

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -55°C to +125°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage Range 0.5V to +4.6V

DC Input Voltage -0.5V to +7.0V

DC Output Voltage -0.5V to +7.0V

DC Output Current

(Maximum Sink Current/Pin) -60 to +120 mA

Power Dissipation 1.0W

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40°C to +85°C	2.7V to 3.6V

Electrical Characteristics for Non Bus Hold Devices Over the Operating Range V_{CC}=2.7V to 3.6V

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{IH}	Input HIGH Voltage	All Inputs	2.0		5.5	V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[5]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =5.5			±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	μA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =5.5V			±1	μA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =GND			±1	μA
I _{OS}	Short Circuit Current ^[6]	V _{CC} =Max., V _{OUT} =GND	-60	-135	-240	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V			±100	μA
I _{CC}	Quiescent Power Supply Current	V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V, V _{CC} =Max.		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{IN} =V _{CC} -0.6V ^[7] , V _{CC} =Max.		2.0	30	μA

Note:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance. Q₀=Previous state of flip-flop.
2. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. With the exception of inputs with bus hold, unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. Typical values are at V_{CC}=3.3V, T_A = +25°C ambient.
5. This parameter is specified but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
7. Per TTL driven input; all other inputs at V_{CC} or GND.

Electrical Characteristics For Balanced Drive Devices Over the Operating Range $V_{CC}=2.7V$ to $3.6V$

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
I_{ODL}	Output LOW Dynamic Current ^[6]	$V_{CC}=3.3V$, $V_{IN}=V_{IH}$ or V_{IL} , $V_{OUT}=1.5V$	45		180	mA
I_{ODH}	Output HIGH Dynamic Current ^[6]	$V_{CC}=3.3V$, $V_{IN}=V_{IH}$ or V_{IL} , $V_{OUT}=1.5V$	-45	-	-180	mA
V_{OH}	Output HIGH Voltage	$V_{CC}=\text{Min.}$, $I_{OH} = -0.1 \text{ mA}$	$V_{CC}-0.2$			V
		$V_{CC}=\text{Min.}$, $I_{OH} = -8 \text{ mA}$	2.4 ^[8]	3.0		V
		$V_{CC}=3.0V$, $I_{OH} = -24 \text{ mA}$	2.0	3.0		V
V_{OL}	Output LOW Voltage	$V_{CC}=\text{Min.}$, $I_{OL} = 0.1 \text{ mA}$			0.2	V
		$V_{CC}=\text{Min.}$, $I_{OL} = 24 \text{ mA}$		0.3	0.55	

Note:

8. $V_{OH}=V_{CC}-0.6 \text{ V}$ at rated current.

Capacitance^[5] ($T_A = +25^\circ\text{C}$, $f = 1.0 \text{ MHz}$)

Parameter	Description	Test Conditions	Typ. ^[4]	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4.5	6.0	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[4]	Max.	Unit
I_{CCD}	Dynamic Power Supply Current ^[9]	$V_{CC}=\text{Max.}$, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}=\text{GND}$ $V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	50	75	$\mu\text{A}/\text{MHz}$
I_C	Total Power Supply Current ^[10]	$V_{CC}=\text{Max.}$, $f_1=10 \text{ MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}=\text{GND}$ $V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	0.5	0.8	mA
		$V_{IN}=V_{CC}-0.6V$ or $V_{IN}=\text{GND}$	0.5	0.8	mA
		$V_{CC}=\text{Max.}$, $f_1=2.5 \text{ MHz}$, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}=\text{GND}$ $V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	2.0	3.0 ^[11]	mA
		$V_{IN}=V_{CC}-0.6V$ or $V_{IN}=\text{GND}$	2.0	3.3 ^[11]	mA

Switching Characteristics Over the Operating Range $V_{CC}=3.0V$ to $3.6V$ ^[12,13]

Parameter	Description	CY74FCT163373C		Unit	Fig. No. ^[14]
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to Q Output	1.5	4.1	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay LE to Q Output	2.0	5.5	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.2	ns	1, 7, 8
t_{SU}	Input Setup time	2.0	-	ns	1, 4
t_H	Input Hold time	1.5	-	ns	1, 4
$t_{SK(O)}$	Output Skew ^[15]		0.5	ns	—

Notes:

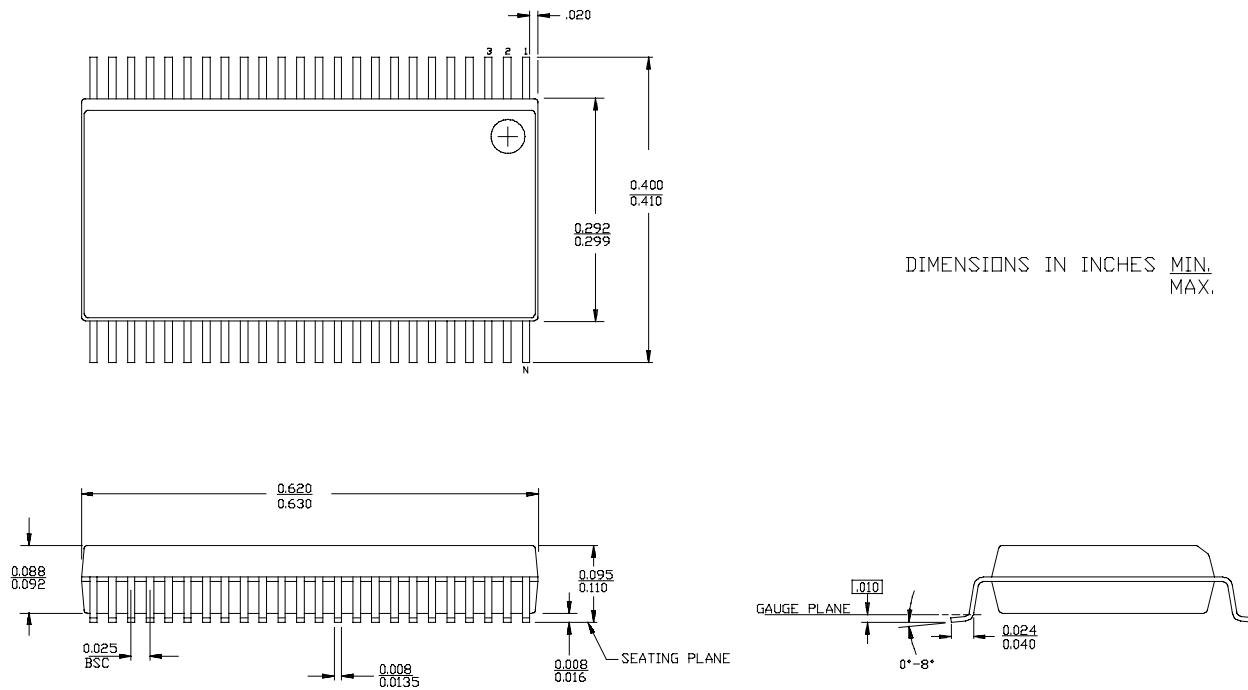
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN}=3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.
12. Minimum limits are specified but not tested on Propagation Delays.
13. For $V_{CC}=2.7$, propagation delay, output enable and output disable times should be degraded by 20%.
14. See "Parameter Measurement Information" in the General Information section.
15. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

Ordering Information CY74FCT163373

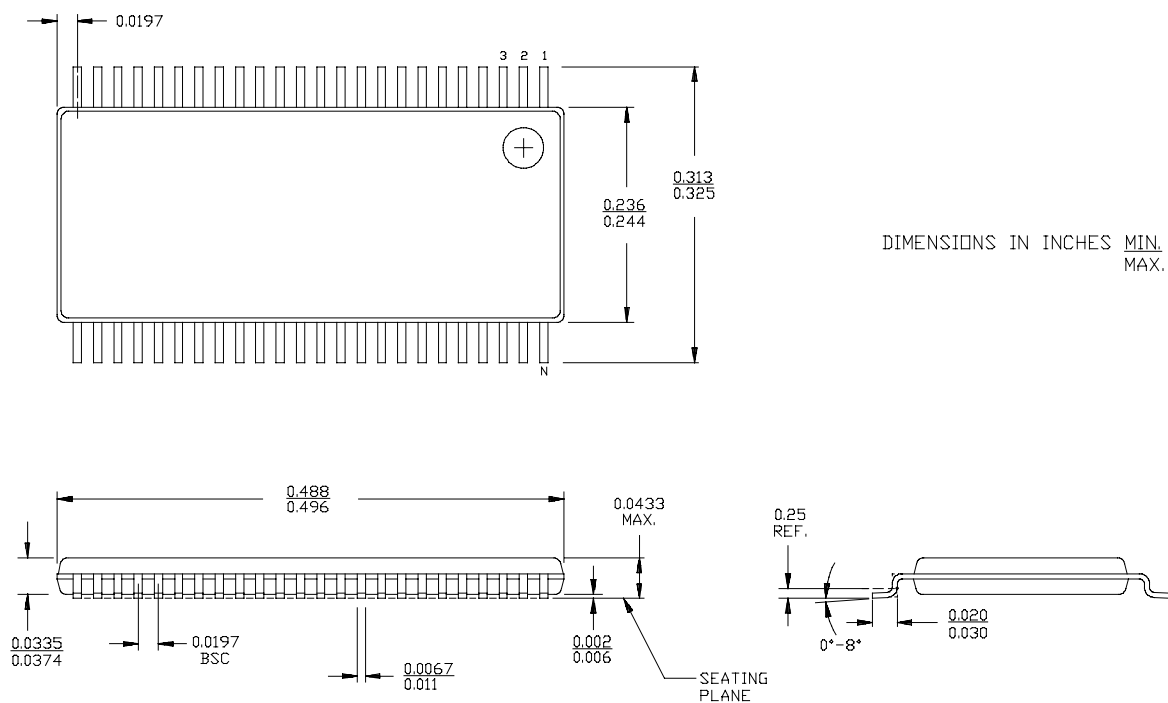
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT163373CPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163373CPVC/PVCT	O48	48-Lead (300-Mil) SSOP	

Package Diagrams

48-Lead Shrunk Small Outline Package O48



48-Lead Thin Shrunk Small Outline Package Z48



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