



74HC4020-Q100; 74HCT4020-Q100

14-stage binary ripple counter

Rev. 3 — 27 March 2024

Product data sheet

1. General description

The 74HC4020-Q100; 74HCT4020-Q100 is a 14-stage binary ripple counter with a clock input (CP), an overriding asynchronous master reset input (MR) and 12 buffered parallel outputs (Q0, and Q3 to Q13). The counter advances on the HIGH-to-LOW transition of CP. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of CP. Each counter stage is a static toggle flip-flop. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Input levels:
 - For 74HC4020-Q100: CMOS level
 - For 74HCT4020-Q100: TTL level
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Applications

- Frequency dividing circuits
- Time delay circuits
- Control counters

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC4020D-Q100 74HCT4020D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4020PW-Q100 74HCT4020PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4020BQ-Q100 74HCT4020BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

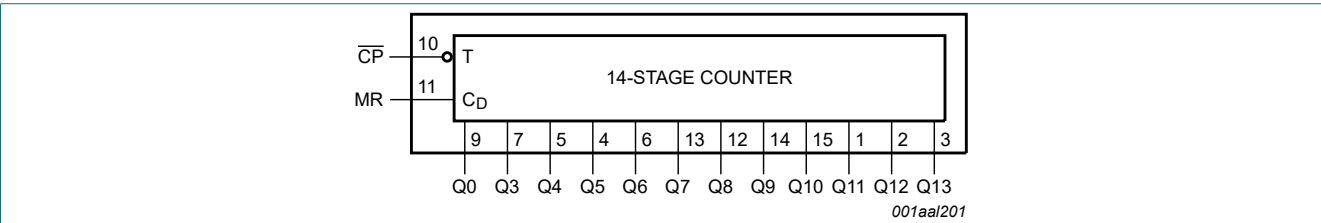


Fig. 1. Functional diagram

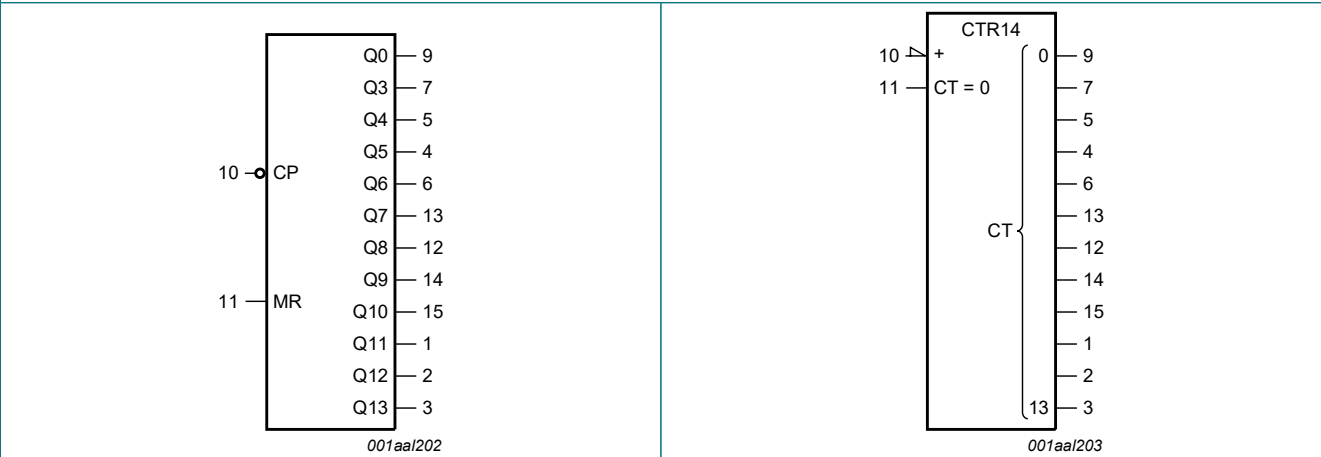


Fig. 2. Logic symbol

Fig. 3. IEC logic symbol

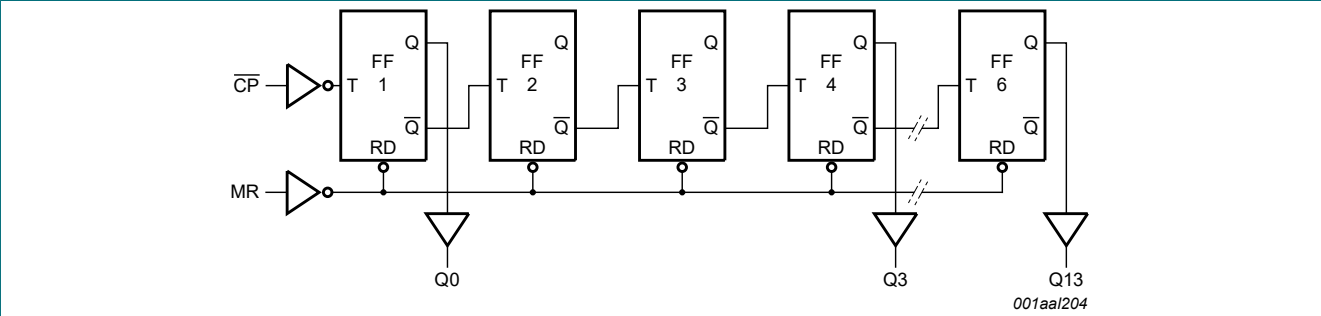
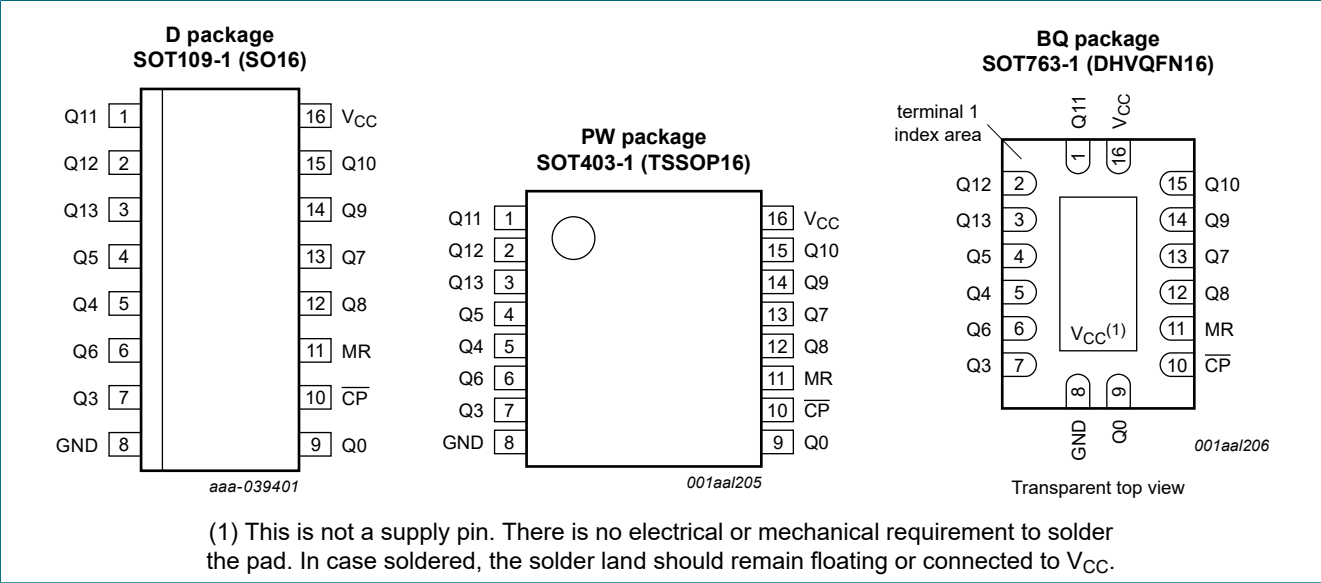


Fig. 4. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q3 to Q13	9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	output
GND	8	ground (0 V)
CP	10	clock input (HIGH-to-LOW, edge-triggered)
MR	11	master reset input (active HIGH)
V _{CC}	16	positive supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;
↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

Input		Output
CP	MR	Q0, Q3 to Q13
↑	L	no change
↓	L	count
X	H	L

7.1. Timing diagram

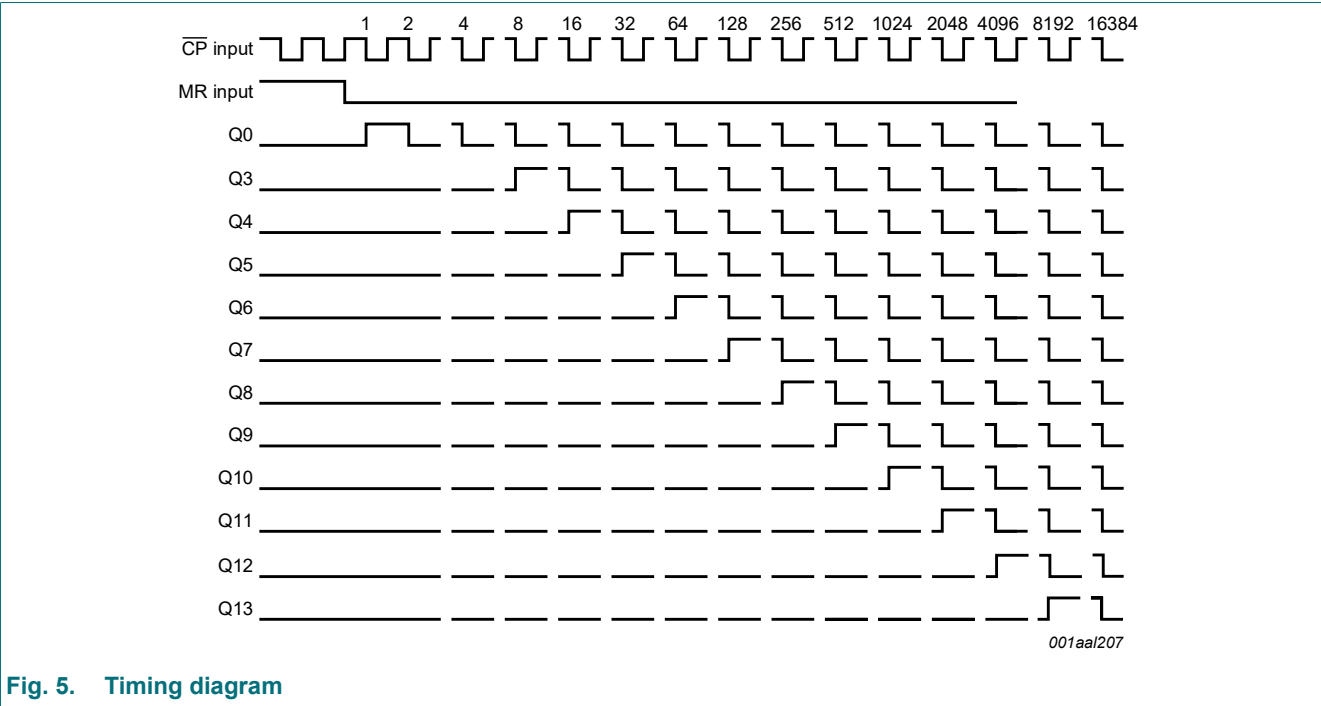


Fig. 5. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	±50	mA
I _{GND}	ground current		-	±50	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [1]	-	500	mW

- [1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4020-Q100			74HCT4020-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
Δt/ΔV	input transition rise and fall rate	except for Schmitt trigger inputs							
		V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4020-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT4020-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 2.1 V; I _O = 0 A; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		pin MR	-	110	396	-	495	-	539	µA
		pin $\overline{\text{CP}}$	-	85	306	-	383	-	417	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 8

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4020-Q100										
t _{pd}	propagation delay	CP to Q0; see Fig. 6 [1]								
		V _{CC} = 2.0 V	-	39	140	-	175	-	210	ns
		V _{CC} = 4.5 V	-	14	28	-	35	-	42	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	11	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	11	24	-	30	-	36	ns
		Qn to Qn+1; see Fig. 7								
		V _{CC} = 2.0 V	-	22	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	8	15	-	19	-	22	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	6	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 6								
		V _{CC} = 2.0 V	-	55	170	-	215	-	225	ns
		V _{CC} = 4.5 V	-	20	34	-	43	-	51	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	17	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	16	29	-	37	-	43	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_t	transition time	Qn; see Fig. 6 [2]								
		$V_{CC} = 2.0 \text{ V}$	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0 \text{ V}$	-	6	13	-	16	-	19	ns
t_W	pulse width	$\overline{CP}$ HIGH or LOW; see Fig. 6								
		$V_{CC} = 2.0 \text{ V}$	80	14	-	100	-	120	-	ns
		$V_{CC} = 4.5 \text{ V}$	16	4	-	20	-	24	-	ns
		$V_{CC} = 6.0 \text{ V}$	14	3	-	17	-	20	-	ns
		MR HIGH; see Fig. 6								
		$V_{CC} = 2.0 \text{ V}$	80	17	-	100	-	120	-	ns
		$V_{CC} = 4.5 \text{ V}$	16	6	-	20	-	24	-	ns
		$V_{CC} = 6.0 \text{ V}$	14	5	-	17	-	20	-	ns
t_{rec}	recovery time	MR to $\overline{CP}$; see Fig. 6								
		$V_{CC} = 2.0 \text{ V}$	50	6	-	65	-	75	-	ns
		$V_{CC} = 4.5 \text{ V}$	10	2	-	13	-	15	-	ns
		$V_{CC} = 6.0 \text{ V}$	9	2	-	11	-	13	-	ns
f_{max}	maximum frequency	see Fig. 6								
		$V_{CC} = 2.0 \text{ V}$	6.0	30	-	4.8	-	4.0	-	MHz
		$V_{CC} = 4.5 \text{ V}$	30	92	-	24	-	20	-	MHz
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	101	-	-	-	-	-	MHz
		$V_{CC} = 6.0 \text{ V}$	35	109	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	[3]	-	19	-	-	-	-	-	pF
74HCT4020-Q100										
t_{pd}	propagation delay	$\overline{CP}$ to Q0; see Fig. 6 [1]								
		$V_{CC} = 4.5 \text{ V}$	-	18	36	-	45	-	54	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	15	-	-	-	-	-	ns
		Qn to Qn+1; see Fig. 7								
		$V_{CC} = 4.5 \text{ V}$	-	8	15	-	19	-	22	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	6	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 6								
		$V_{CC} = 4.5 \text{ V}$	-	22	45	-	56	-	68	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	19	-	-	-	-	-	ns
t_t	transition time	Qn; see Fig. 6 [2]								
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	-	22	ns
t_W	pulse width	$\overline{CP}$ HIGH or LOW; see Fig. 6								
		$V_{CC} = 4.5 \text{ V}$	20	7	-	25	-	30	-	ns
		MR HIGH; see Fig. 6								
		$V_{CC} = 4.5 \text{ V}$	20	8	-	25	-	30	-	ns
t_{rec}	recovery time	MR to $\overline{CP}$; see Fig. 6								
		$V_{CC} = 4.5 \text{ V}$	10	2	-	13	-	15	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
f _{max}	maximum frequency	see Fig. 6								
		V _{CC} = 4.5 V	25	47	-	20	-	17	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	52	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	[3]	-	20	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

[2] t_t is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

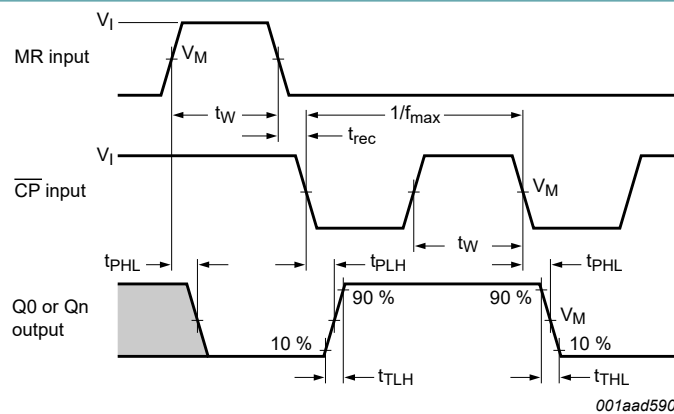
f_o = output frequency in MHz;

$$\Sigma (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs};$$

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

11.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Clock timing, propagation delays and pulse widths

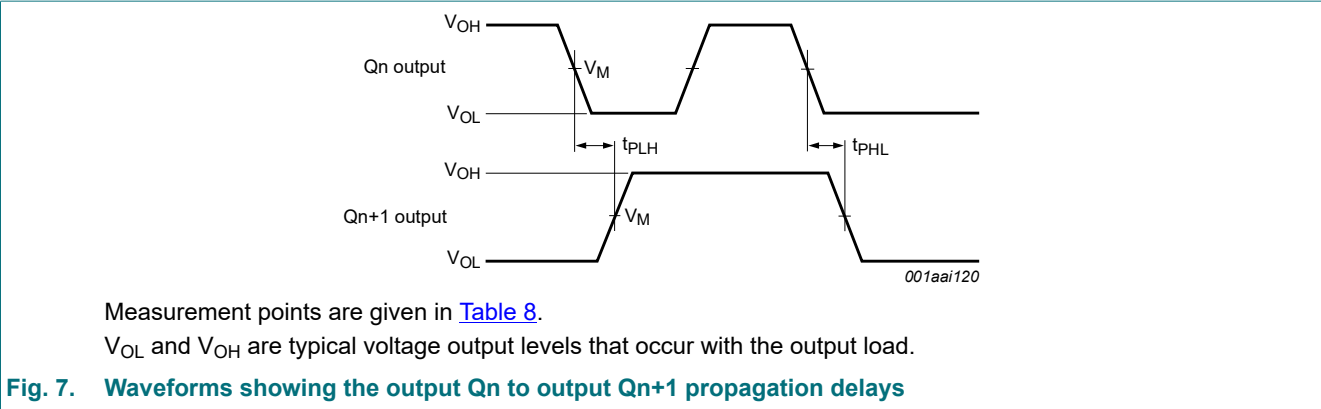


Table 8. Measurement points

Type	Input		Output
	V_M		V_M
74HC4020-Q100	$0.5 \times V_{CC}$		$0.5 \times V_{CC}$
74HCT4020-Q100	1.3 V		1.3 V

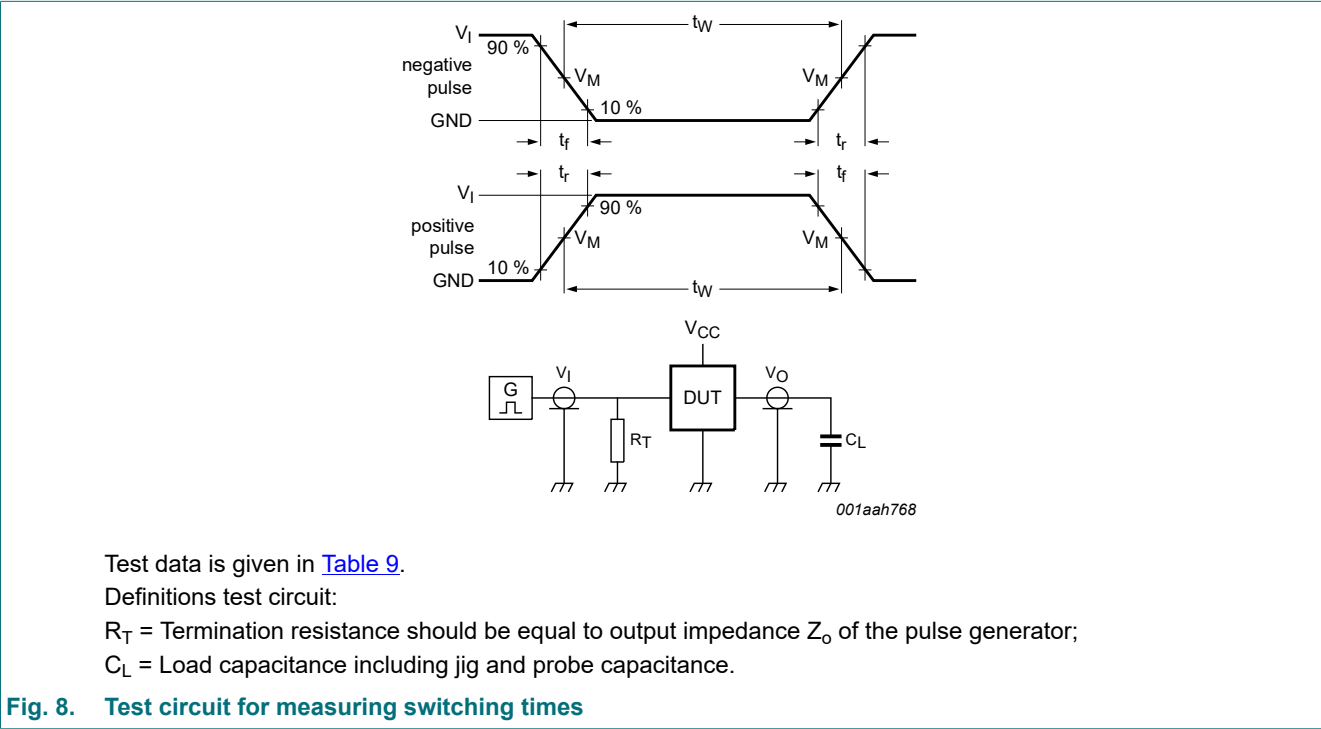


Table 9. Test data

Type	Input		Load
	V_I	t_r, t_f	C_L
74HC4020-Q100	V_{CC}	6 ns	15 pF, 50 pF
74HCT4020-Q100	3 V	6 ns	15 pF, 50 pF

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

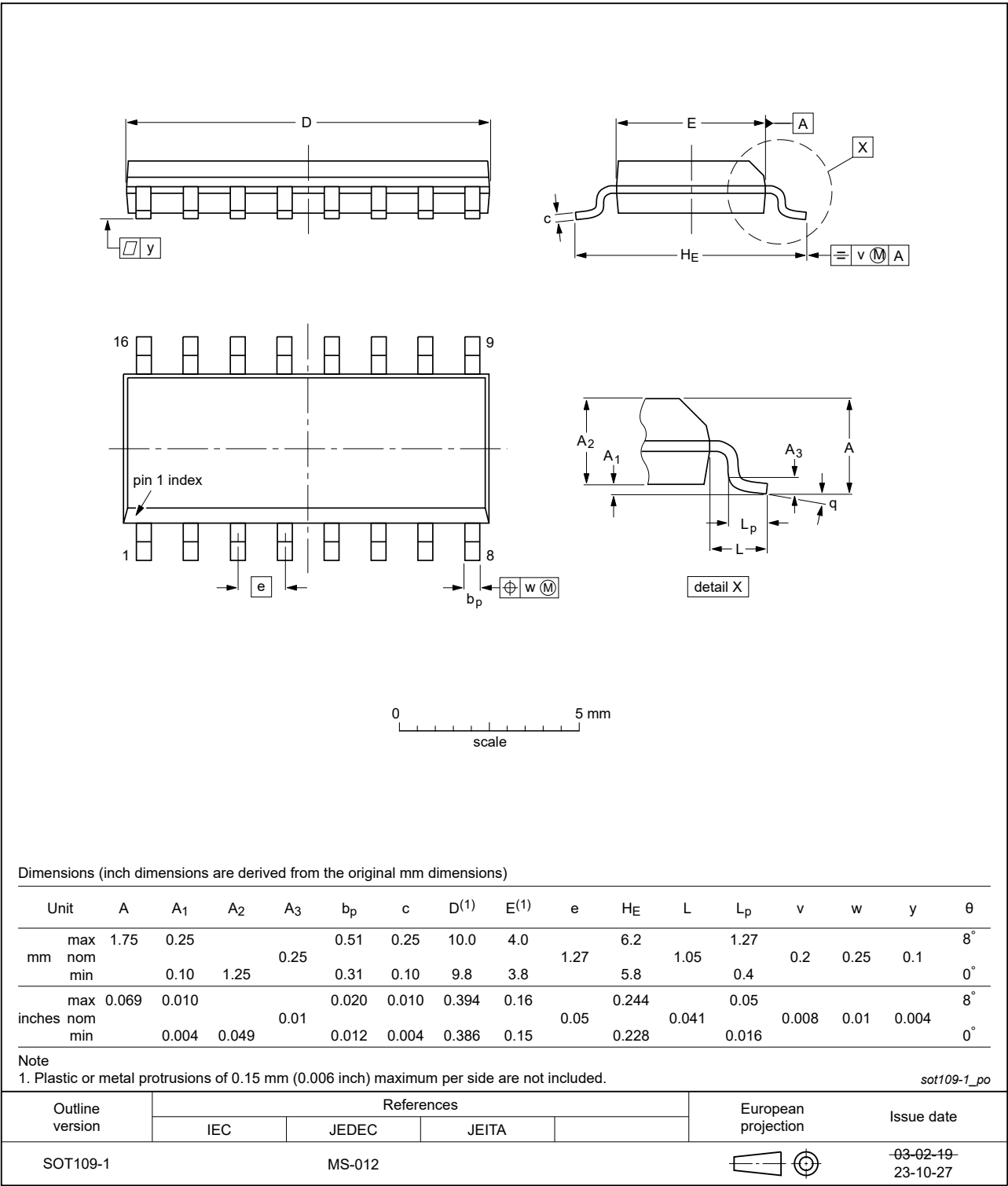


Fig. 9. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

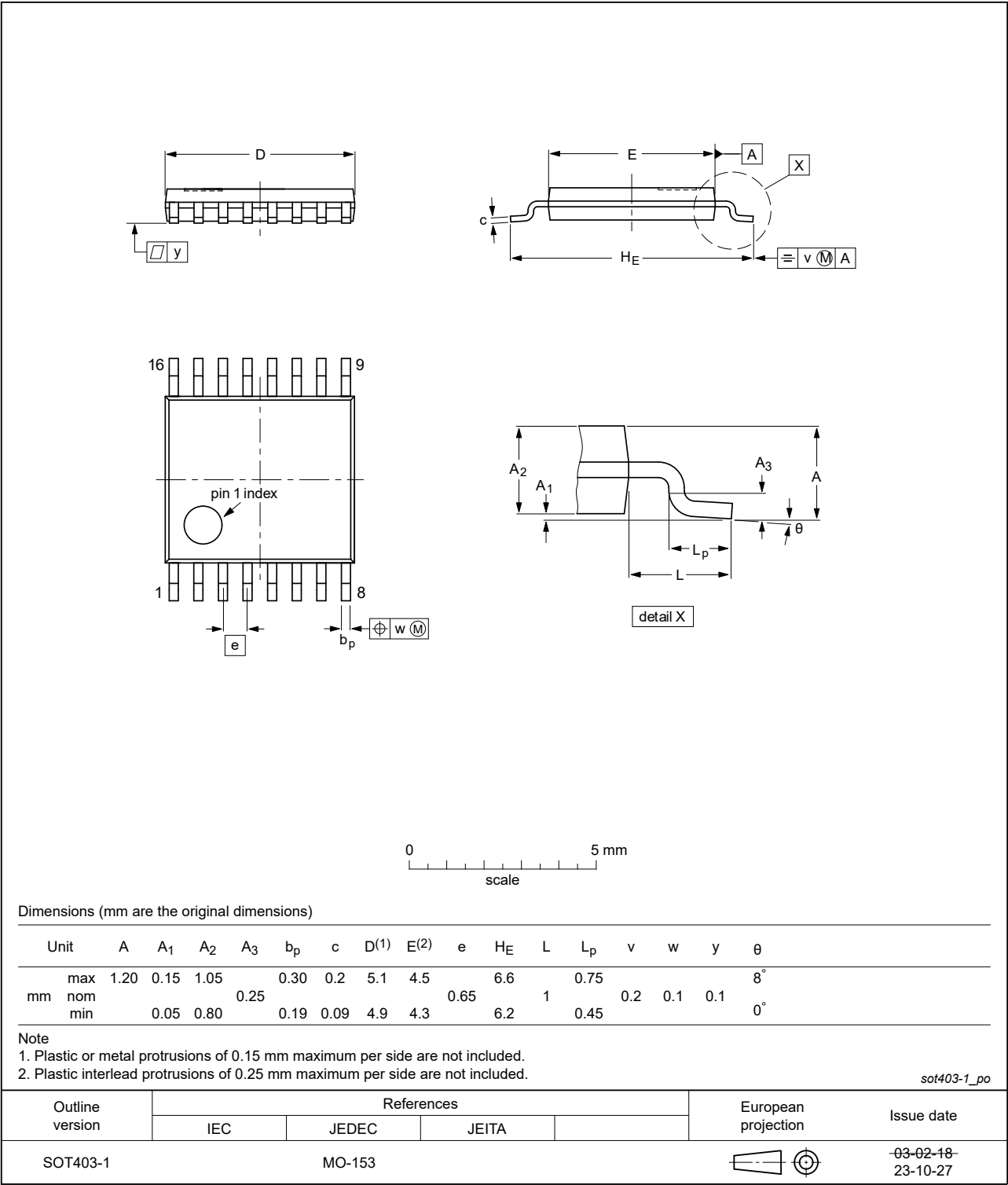


Fig. 10. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

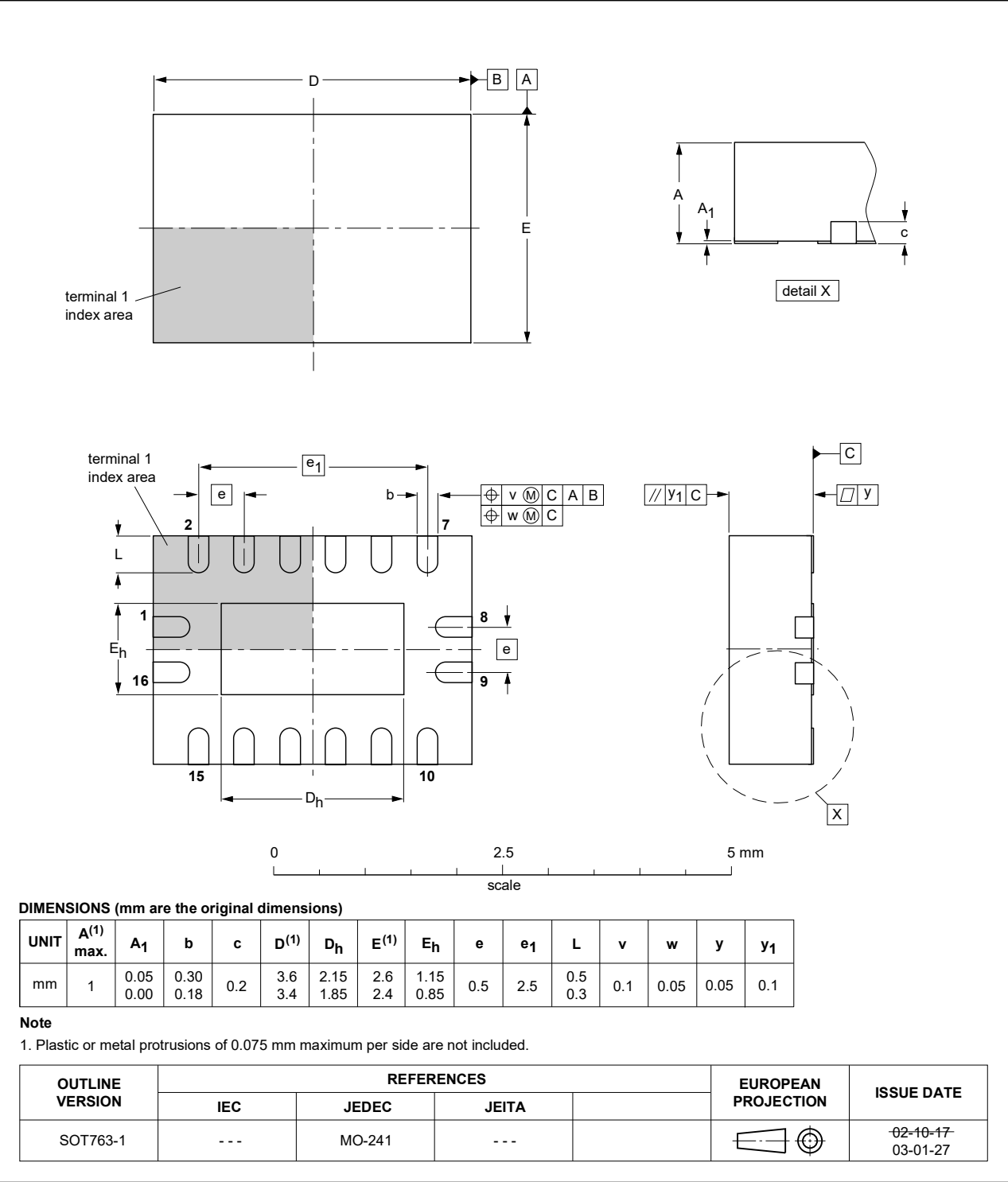


Fig. 11. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4020_Q100 v.3	20240327	Product data sheet	-	74HC_HCT4020_Q100 v.2
Modifications:	- Section 2: ESD specification updated according to the latest JEDEC standard. - Fig. 9, Fig. 10: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153			
74HC_HCT4020_Q100 v.2	20200618	Product data sheet	-	74HC_HCT4020_Q100 v.1
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Section 1 and Section 2 updated. - Table 4: Derating values for P_{tot} total power dissipation have been updated.			
74HC_HCT4020_Q100 v.1	20130523	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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