



FJ3P02100L

Silicon P-channel MOSFET

For Load-switching

Features

- Low drain-source ON resistance: $R_{DS(on)typ.} = 12.0m\Omega$ ($V_{GS} = -2.5V$)
- High heat dissipated and ultra-compact package PMCP
- RoHS compliant (EU RoHS / MSL:Level 1 compliant)

Marking Symbol: A0

Packaging

Embossed type (Thermo-compression sealing) : 7 000 pcs / reel (standard)

Absolute Maximum Ratings $T_a = 25^\circ C$

Parameter	Symbol	Rating	Unit
Drain-source voltage	VDS	-20	V
Gate-source voltage	VGS	± 8	V
Drain current	$T_a = 25^\circ C, DC^{*2}$	ID1	-4.4
	$T_a = 25^\circ C, DC^{*3}$	ID2	-7.5
Drain current (Pulsed)	$T_a = 25^\circ C^{*1*2}$	IDp1	-13.2
	$T_a = 25^\circ C^{*1*3}$	IDp2	-22.5
Total power dissipation	$T_a = 25^\circ C, DC^{*2}$	PD1	300
	$T_a = 25^\circ C, DC^{*3}$	PD2	850
Channel temperature	Tch	150	
Operating ambient temperature	Topr	-40 to +85	$^\circ C$
Storage temperature range	Tstg	-55 to +150	

Note : *1 $t = 10 \mu s$, Duty Cycle < 1%

*2 When mounted on glass epoxy board typeA (Refer to Figure1)

*3 When mounted on glass epoxy board typeB (Refer to Figure2)

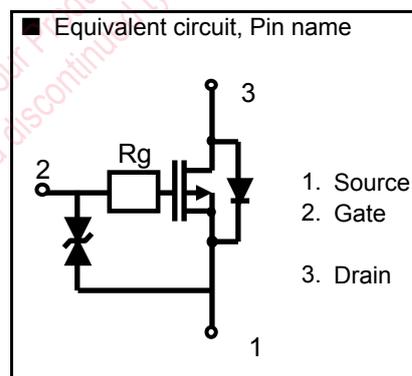
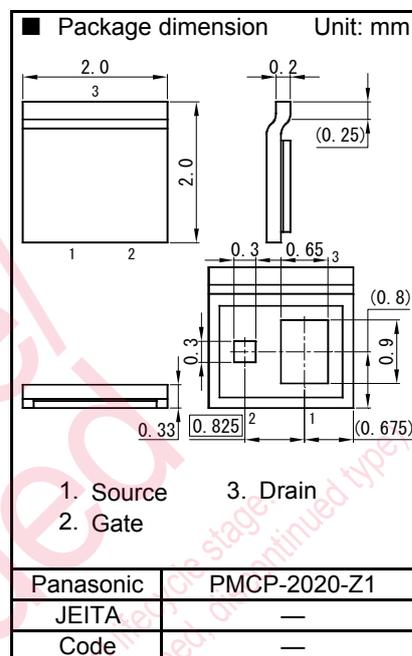
Electrical Characteristics $T_a = 25^\circ C \pm 3^\circ C$

Static Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	VDSS	$I_D = -1.0 mA, V_{GS} = 0 V$	-20			V
Zero gate voltage drain current	IDSS	$V_{DS} = -20 V, V_{GS} = 0 V$			-10	μA
Gate-source leakage current	IGSS	$V_{GS} = \pm 8 V, V_{DS} = 0 V$			± 10	μA
Gate-source threshold voltage	Vth	$I_D = -1.0 mA, V_{DS} = -10 V$	-0.3	-0.65	-1.05	V
Drain-source on-state resistance	RDS(on)1	$I_D = -3.7 A, V_{GS} = -4.5 V$		9.5	12.5	m Ω
	RDS(on)2	$I_D = -3.7 A, V_{GS} = -2.5 V$		12.0	16.5	
	RDS(on)3	$I_D = -3.7 A, V_{GS} = -2.0 V$		16.0	30.0	

Dynamic Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance ^{*1}	Ciss	$V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz$		3000		pF
Output capacitance ^{*1}	Coss			330		
Reverse transfer capacitance ^{*1}	Crss			350		





Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Turn-on delay time ^{*1 *2}	td(on)	VDD = -10 V, VGS = 0 to -4 V, ID = -3.7 A		1		μs
Rise time ^{*1 *2}	tr			1.9		
Turn-off delay time ^{*1 *2}	td(off)	VDD = -10 V, VGS = -4 to 0 V, ID = -3.7 A		6.5		μs
Fall time ^{*1 *2}	tf			3.9		

Note : 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

2. *1 Assured by design

*2 Refer to figure3, measurement circuit for Turn-on delay time / Rise time / Turn-off delay time / Fall time

Figure1: Glass epoxy board typeA

Material:FR4, Size:25.4mm x 25.4mm x t 1.0mm, Cu pad:thickness 36μm, 25.9mm²

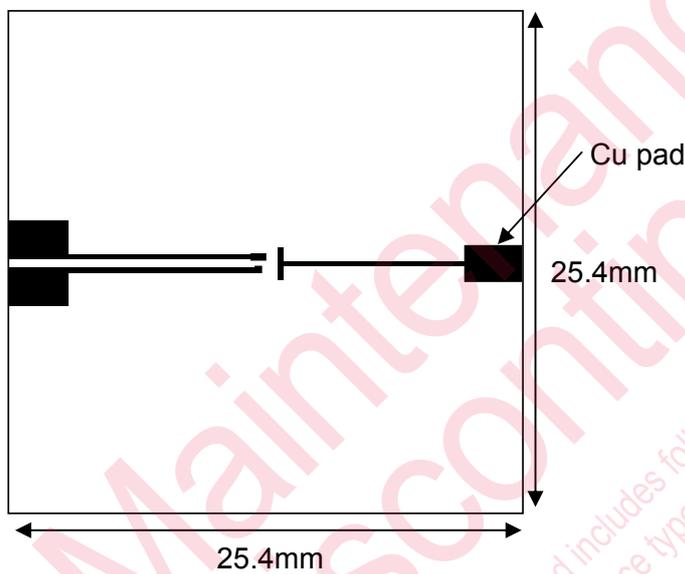


Figure2: Glass epoxy board typeB

Material:FR4, Size:25.4mm x 25.4mm x t 1.0mm, Cu pad:thickness 36μm, 82.0mm²

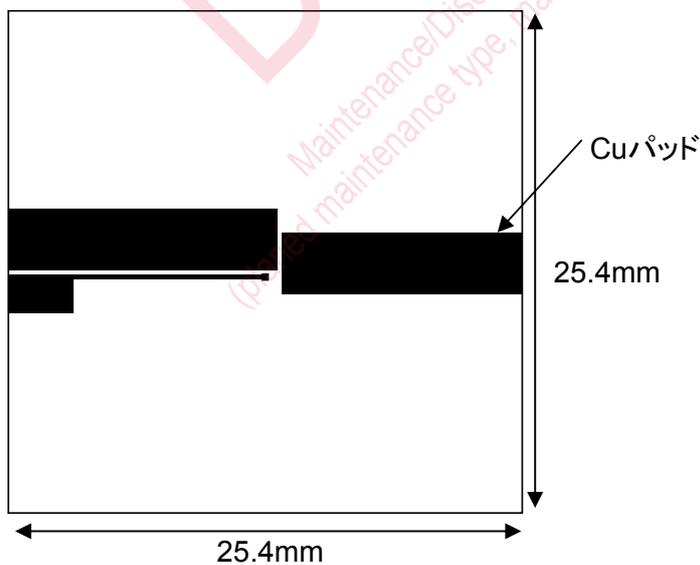
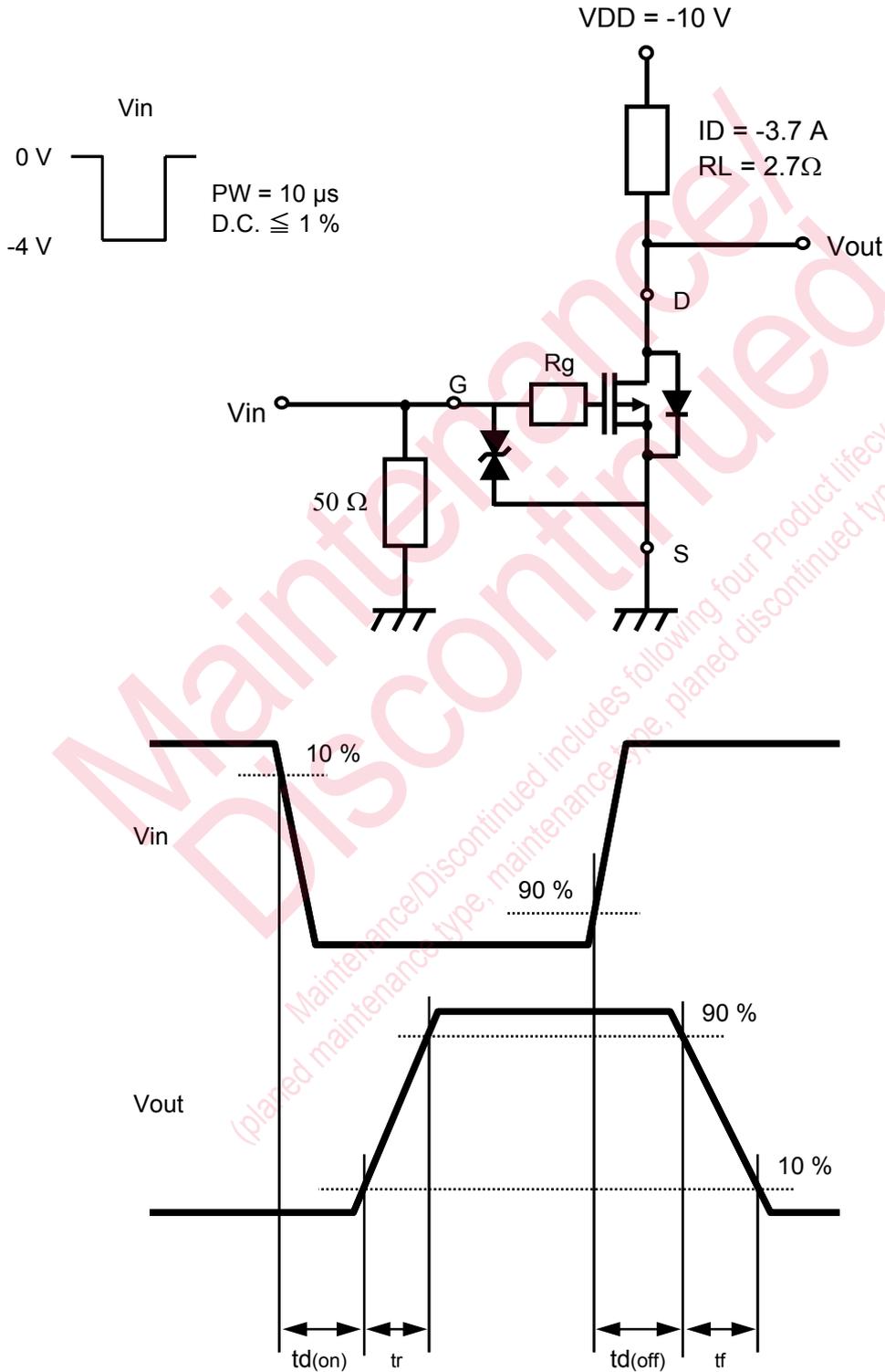


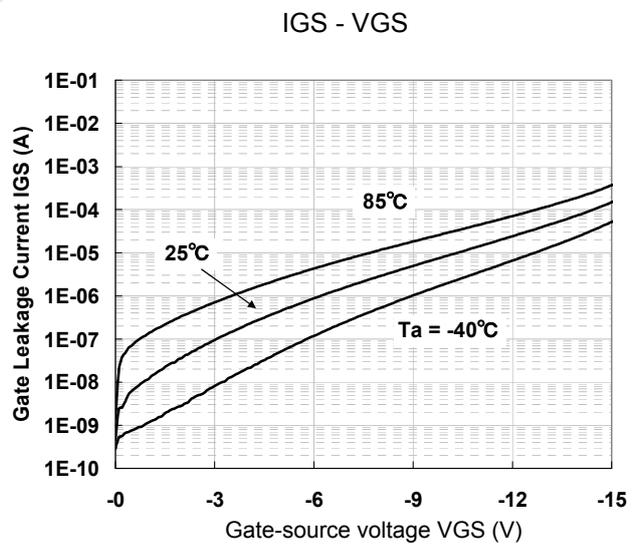
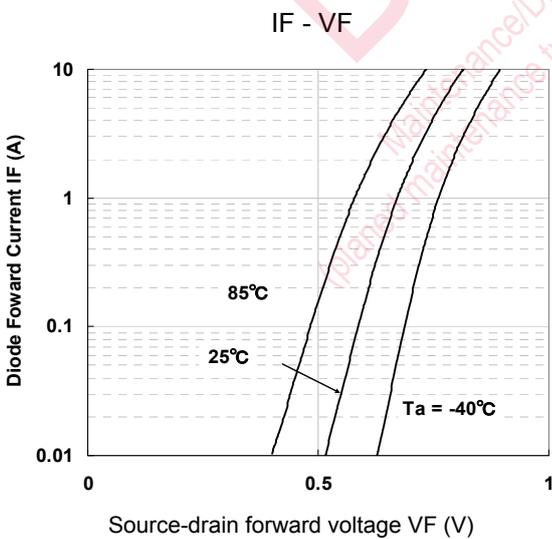
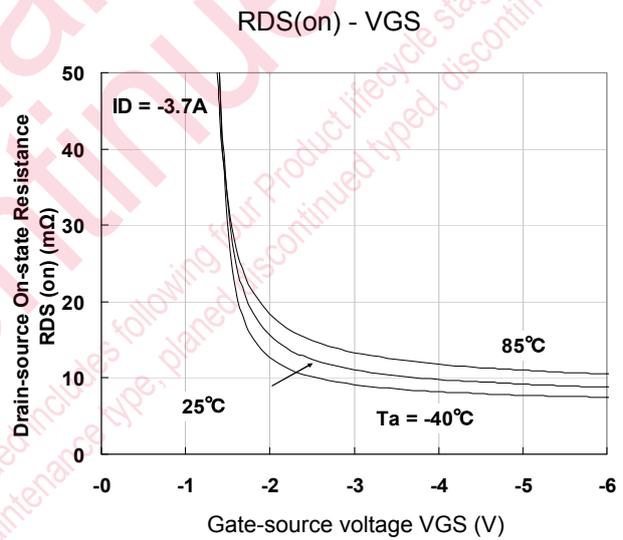
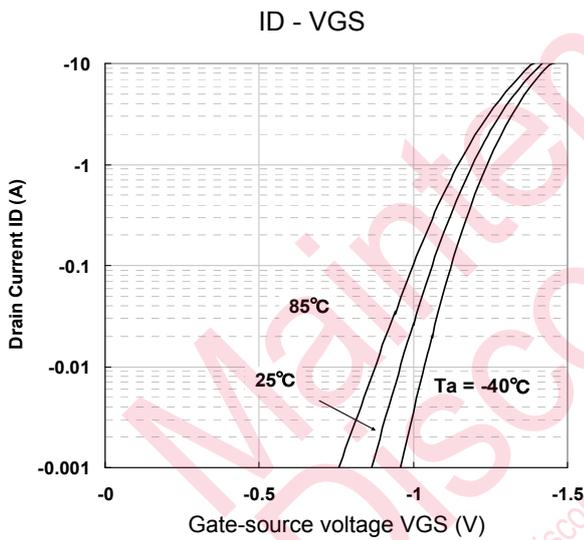
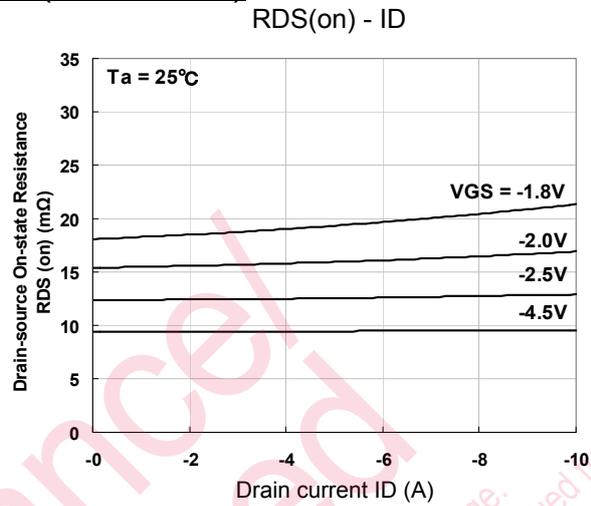
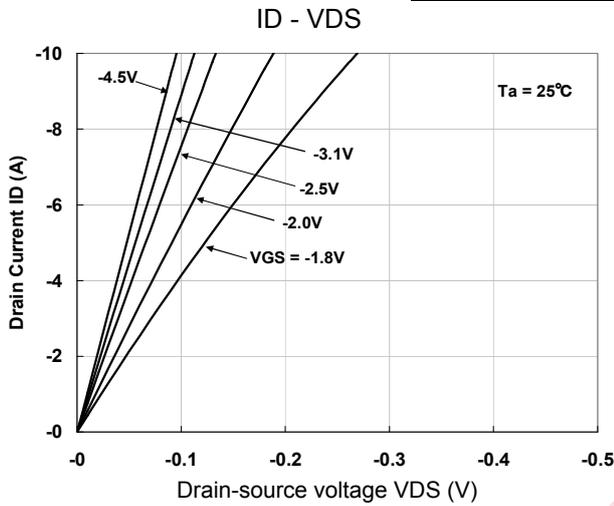


Figure3: Measurement circuit for Turn-on delay time / Rise time / Turn-off delay time / Fall time





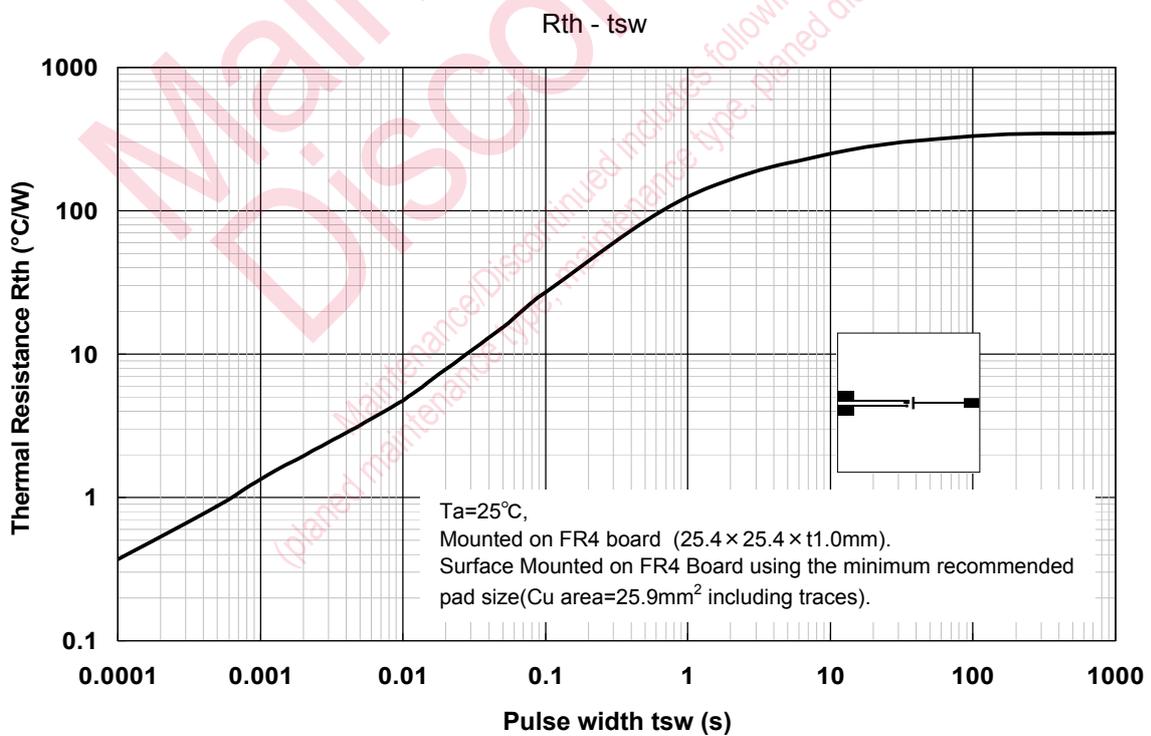
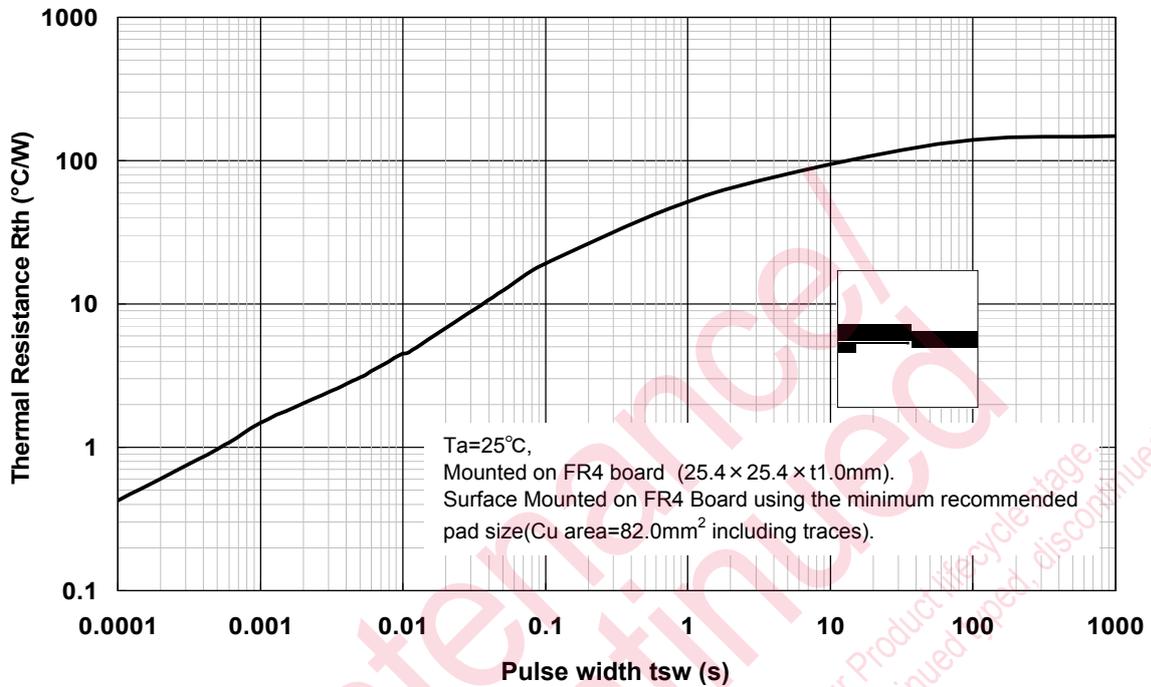
Technical Data (reference)





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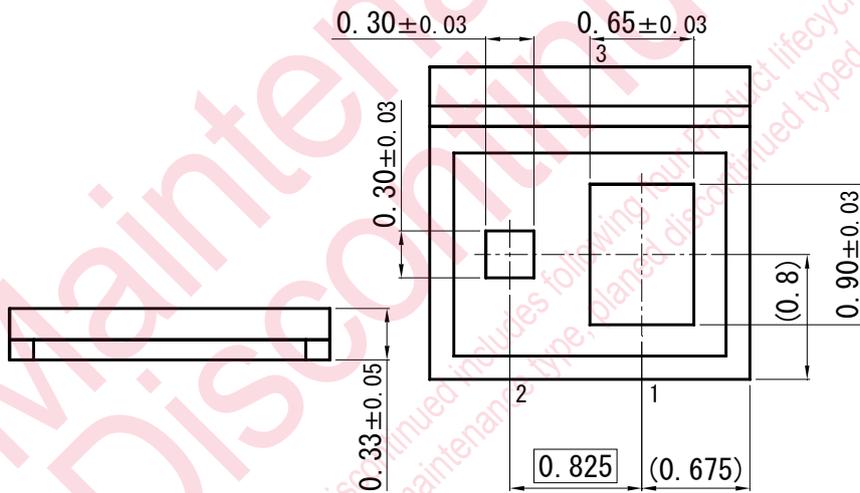
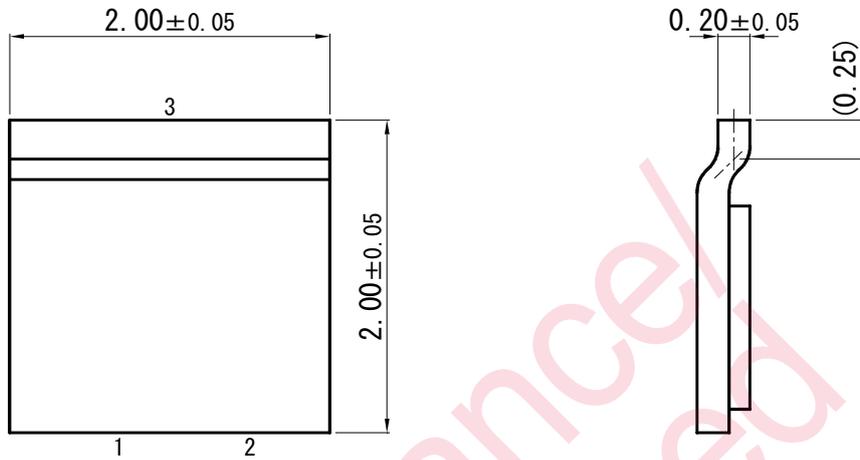
Rth - tsw



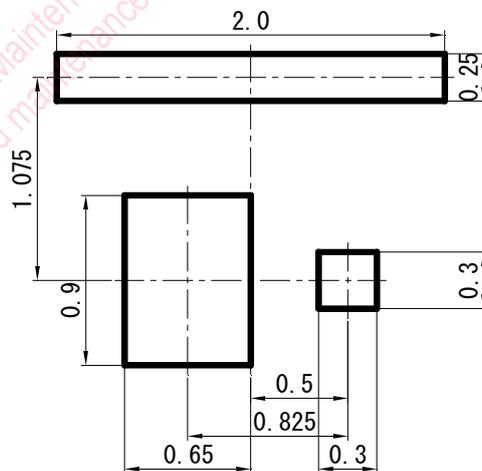


PMCP-2020-Z1

Unit: mm



■ Land Pattern (Reference) (Unit: mm)



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