User's Guide
SLVU279–December 2008

TPS54617EVM-414 6-A, SWIFT™ Regulator Evaluation Module

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1 Introduction

This user's guide contains background information for the TPS54617 as well as support documentation for the TPS54617EVM-414 evaluation module (HPA414). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54617EVM-414.

1.1 Background

The TPS54617 dc/dc converter is designed to provide up to a 6 A output from an input voltage source of 3 V to 6 V. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54617 regulator. The switching frequency is externally set at a nominal 1600 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS54617 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS54617 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54617 provides adjustable slow start, synchonization, enable and frequency adjust inputs along with a powergood output. The absolute maximum input voltage is 7 V for the TPS54617EVM-414.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54617EVM-414	VIN = 3 V to 6 V	0 A to 6 A

1.2 Performance Specification Summary

A summary of the TPS54617EVM-414 performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 5 V and an output voltage of 1.8 V, unless otherwise specified. The TPS54617EVM-414 is designed and tested for V_{IN} = 3 V to 6 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS54617EVM-414 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			3	3.3	6	V
Output voltage set point				1.8		V
Output current range	V_{IN} = 3 V to 6 V		0		6	A
Line regulation	I_O = 3 A, V_{IN} = 3 V to 6 V			±0.2%		
Load regulation	V_{IN} = 3.3 V, I_O = 0 A to 6 A			±0.07%		
Load transient response	I_O = 1.5 A to 4.5 A	Voltage change		–10		mV
		Recovery time		300		µs
	I_O = 4.5 A to 1.5 A	Voltage change		10		mV
		Recovery time		300		µs
Loop bandwidth	V_{IN} = 5 V, I_O = 3 A			45		kHz
Phase margin	V_{IN} = 5 V , I_O = 3 A			57		°
Input ripple voltage	I_O = 6 A			80		mVpp
Output ripple voltage	I_O = 6 A			15		mVpp
Output rise time				6		ms
Operating frequency				1600		kHz
Maximum efficiency	TPS54617EVM-414, V_{IN} = 3.3 V, I_O = 1.0 A			82.7%		

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54617. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

To change the output voltage of the EVM, it is necessary to change the value of resistor R_2. Changing the value of R_2 can change the output voltage above 0.891 V. The value of R_2 for a specific output voltage can be calculated using Equation 1.

$$R_2 = 10\ k\Omega \times \frac{0.891\ V}{V_{OUT} - 0.891\ V} \quad (1)$$

Table 3 lists the R_6 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 130 ns, and the maximum duty cycle is less than 91%. The values given in Table 3 are standard values, not the exact value calculated using Equation 1.

Table 3. Output Voltages Available

Output Voltage (V)	R_2 Value (kΩ)
1.2	28.7
1.8	10
2.5	5.49
3.3	3.74

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54617EVM-414 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input / Output Connections

The TPS54617EVM-414 is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 5 A must be connected to J3 through a pair of 18 AWG wires. The load must be connected to J2 through a pair of 18 AWG wires. The maximum load current capability must be 6 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP2 provides a place to monitor the V_{IN} input voltages with TP5 providing a convenient ground reference. TP1 is used to monitor the output voltage with TP6 as the ground reference.

Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	Sync input.
J2	V_{OUT}, 3.3 V at 2 A maximum
J3	V_{IN} (see Table 1 for V_{IN} range)
J4	2-pin header for enable. Connect SS/ENA to ground to disable, open to enable.
TP1	Output voltage test point at OUT connector
TP2	V_{IN} test point at V_{IN} connector
TP3	Test point between voltage divider network and output. Used for loop response measurements.
TP4	PH test point
TP5	GND test point at V_{IN}
TP6	GND test point at OUT connector

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 0.5 A – 1 A and then decreases as the load current increases towards full load. Figure 1 shows the efficiency for the TPs54617EVM-414 at an ambient temperature of 25°C.

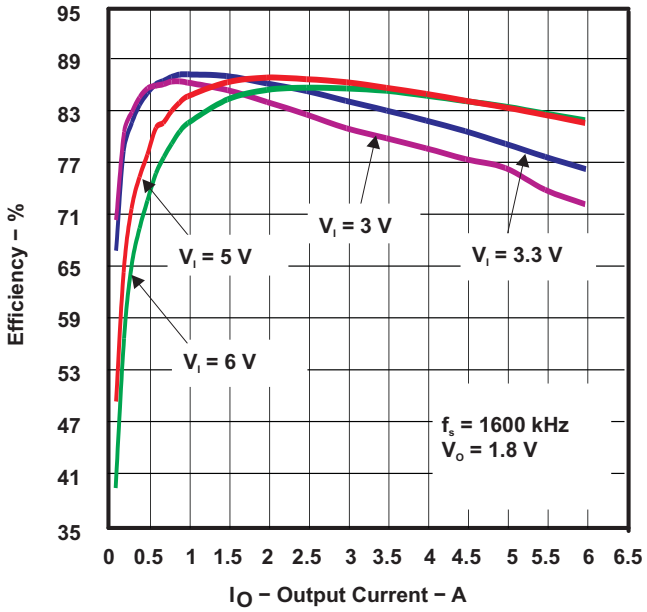

Figure 1. TPS54617EVM-414 Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

The load regulation for the TPS54617EVM-414 is shown in Figure 2.

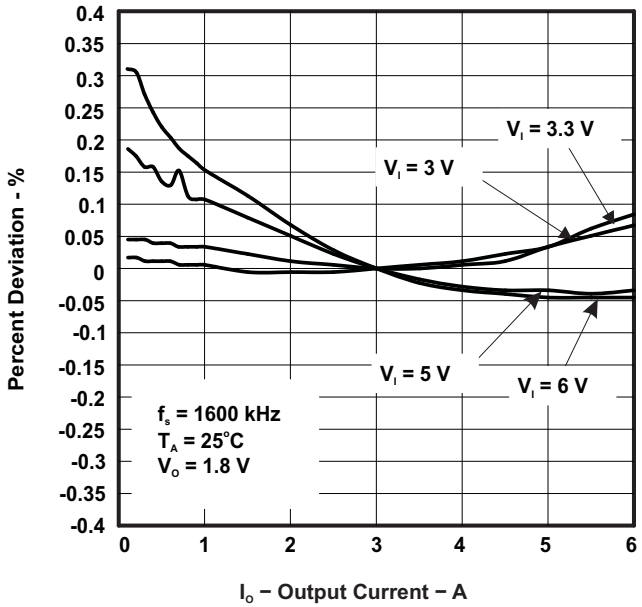

Figure 2. TPS54617EVM-414 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

The line regulation for the TPS54617EVM-414 is shown in Figure 3.

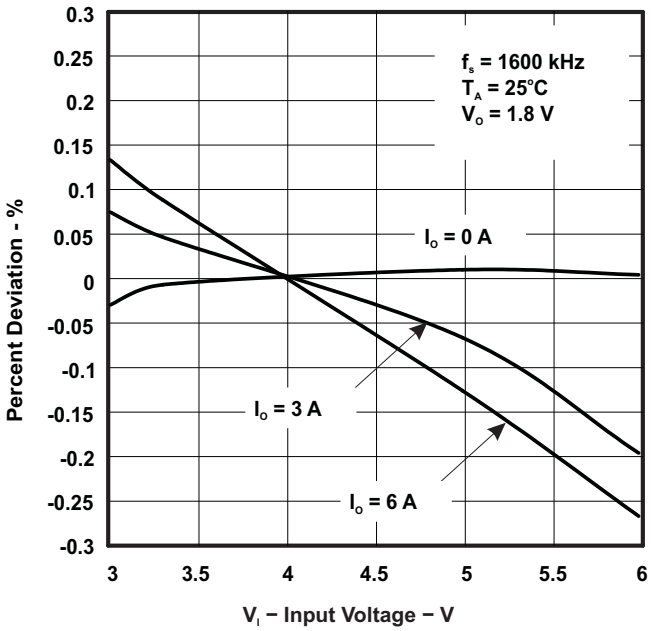

Figure 3. TPS54617EVM-414 Line Regulation

2.5 Load Transients

The TPS54617EVM-414 response to load transients is shown in Figure 4. The current step (displayed at 2 A / div) is from 25% to 75% of maximum rated load (1.5 to 4.5 A) at 5 V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

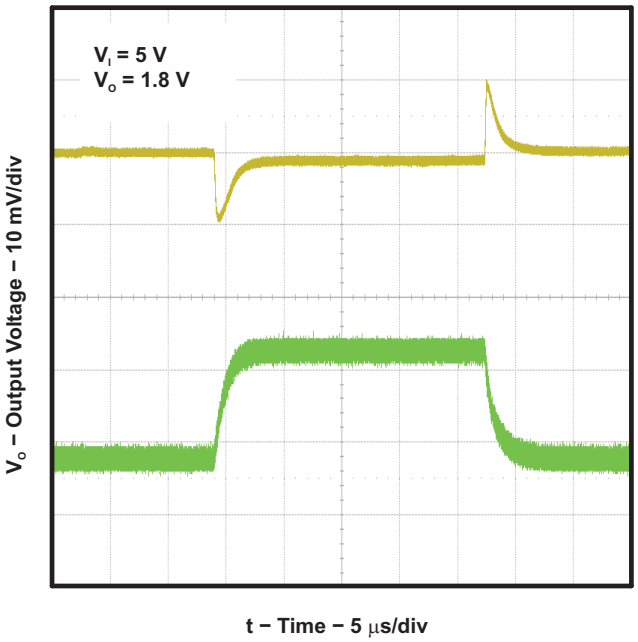

Figure 4. TPS54617EVM-414 Transient Response

2.6 Loop Characteristics

The TPS54617EVM-414 loop-response characteristics are shown in Figure 5 . Gain and phase plots are shown for V_{IN} voltage of 5 V. Load current for the measurement is 3 A.

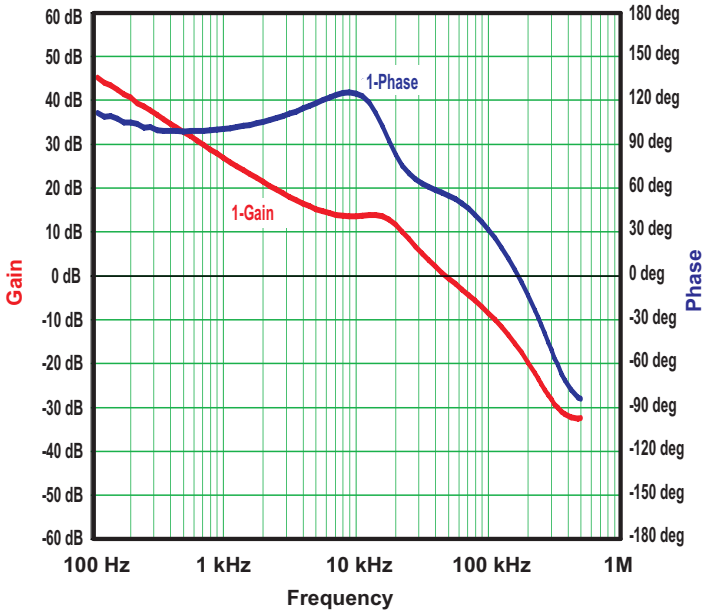

Figure 5. TPS54617EVM-414 Loop Response

2.7 Output Voltage Ripple

The TPS54617EVM-414 output voltage ripple is shown in Figure 6. The output current is the rated full load of 6 A and V_{IN} = 5 V. The ripple voltage is measured directly across the output capacitors.

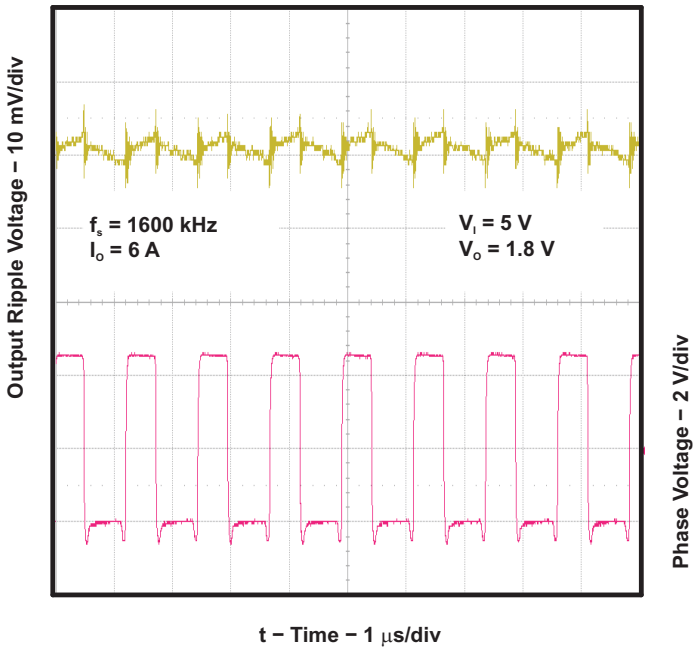

Figure 6. TPS54617EVM-414 Output Ripple

2.8 Input Voltage Ripple

The TPS54617EVM-414 input voltage ripple is shown in Figure 7. The output current is the rated full load of 6 A and V_{IN} = 5 V. The ripple voltage is measured directly across the input capacitors.

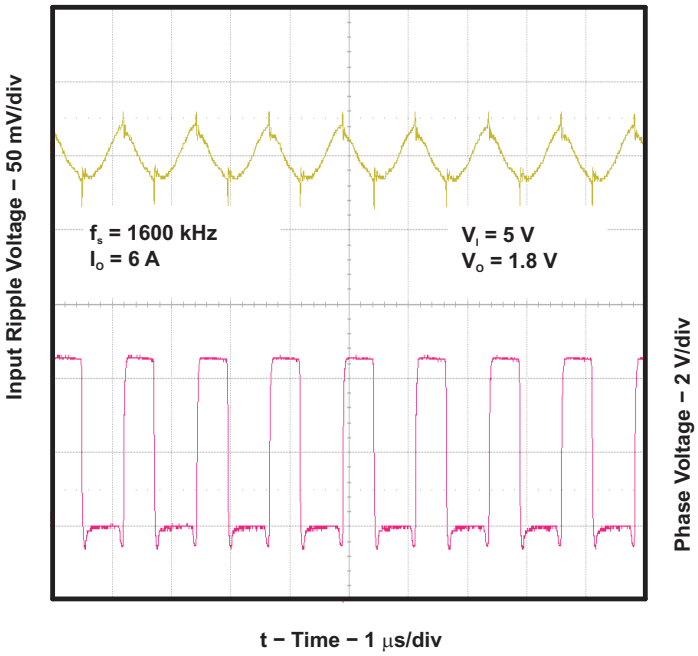

Figure 7. TPS54617EVM-414 Input Ripple

2.9 Powering Up

The start-up waveforms are shown in Figure 8. The top trace shows V_{IN}, and the bottom trace shows V_{OUT}. The top trace shows EN (enable) whereas the bottom trace shows V_{OUT}. The input voltage is initially applied and the output is inhibited by using a jumper at J2 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage of 1.25 V, the start-up sequence begins and the internal reference voltage begins to ramp up at the internally set rate toward 0.8 V and the output voltage ramps up to the externally set value of 3.3 V. The input voltage for these plots is 15 V and there is no load.

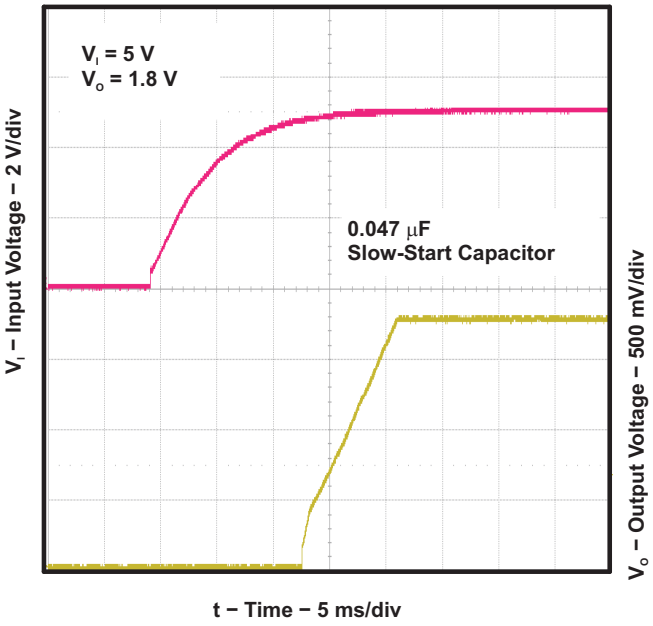

Figure 8. TPS54617EVM-414 Start-up Relative to Input Voltage

3 Board Layout

This section provides a description of the TPS54617EVM-414, board layout, and layer illustrations.

3.1 Layout

The board layout for the TPS54617EVM-414 is shown in Figure 9 through Figure 13. The topside layer of the EVM is laid out in a manner typical of a user application. The two internal layers and bottom-side layer are dedicated ground planes. All layers are 2-oz. copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54617 and a large area filled with ground. The top, bottom and internal ground traces are connected with multiple vias placed around the board including twelve vias directly under the TPS54617 device to provide a thermal path from the top-side ground plane to the bottom-side ground plane.

The input decoupling capacitors (C1, C2, and C12) and bootstrap capacitor (C6) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider and compensation components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the V_{OUT} copper pour areanear the output connector J2 and TP1. For the TPS54617, an additional input bulk capacitor C13 may be required, depending on the EVM connection to the input supply.

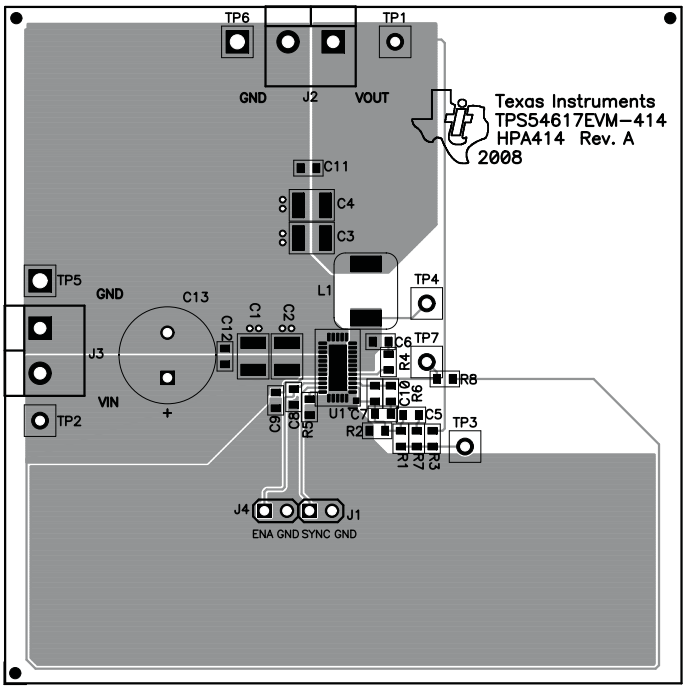

Figure 9. TPS54617EVM-414 Top-Side Layout

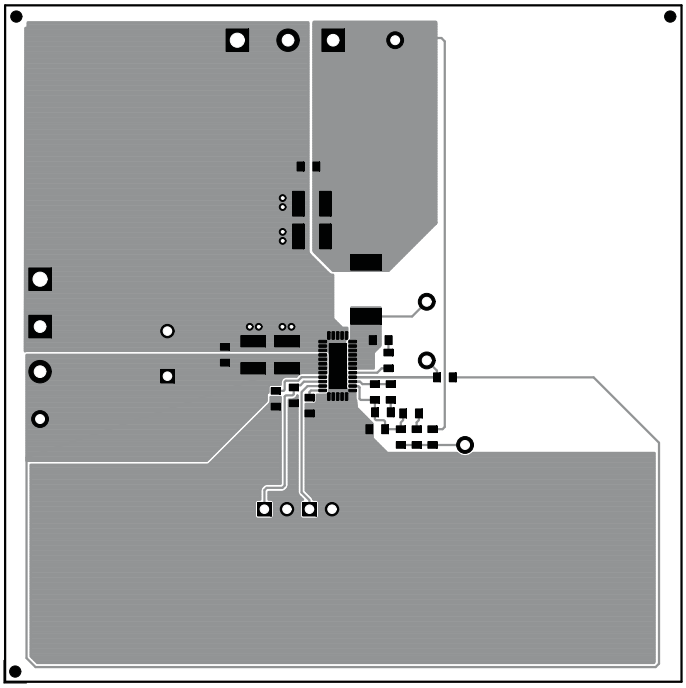

Figure 10. TPS54617EVM-414 Another Layer

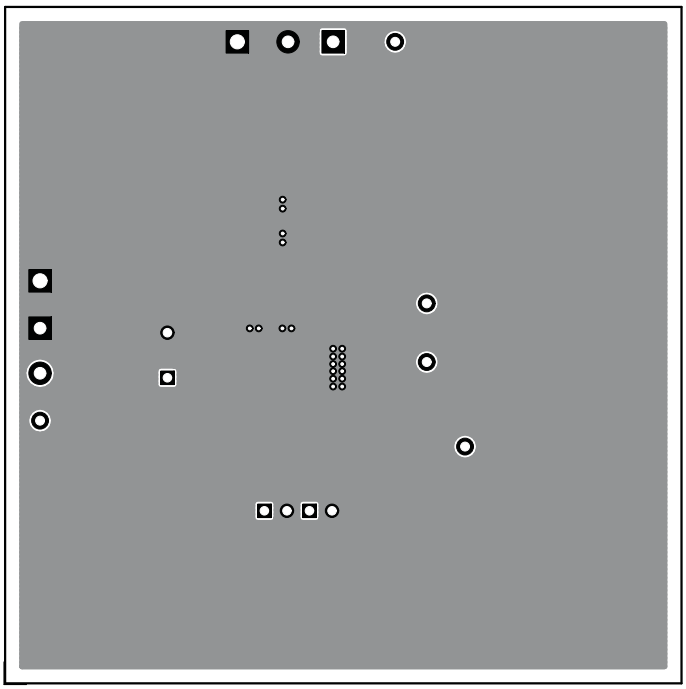

Figure 11. TPS54617EVM-414 And Another Layer

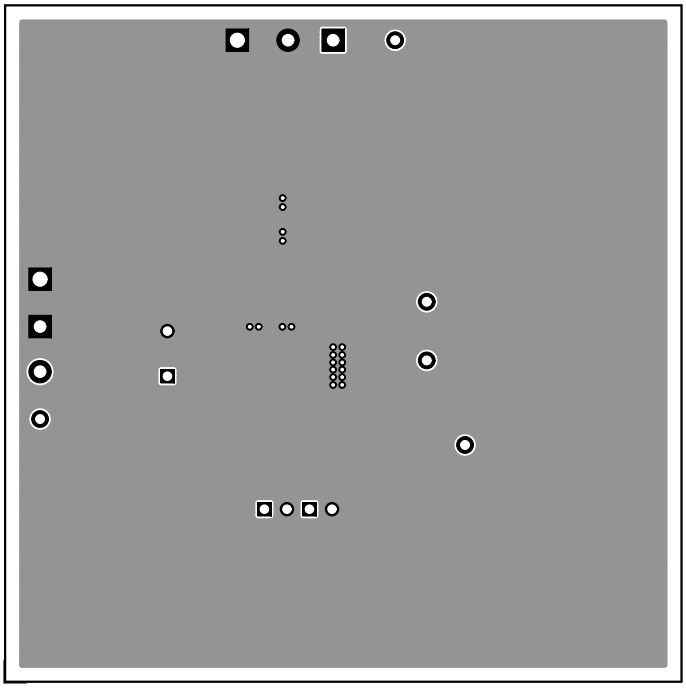

Figure 12. TPS54617EVM-414 Bottom-Side Layout

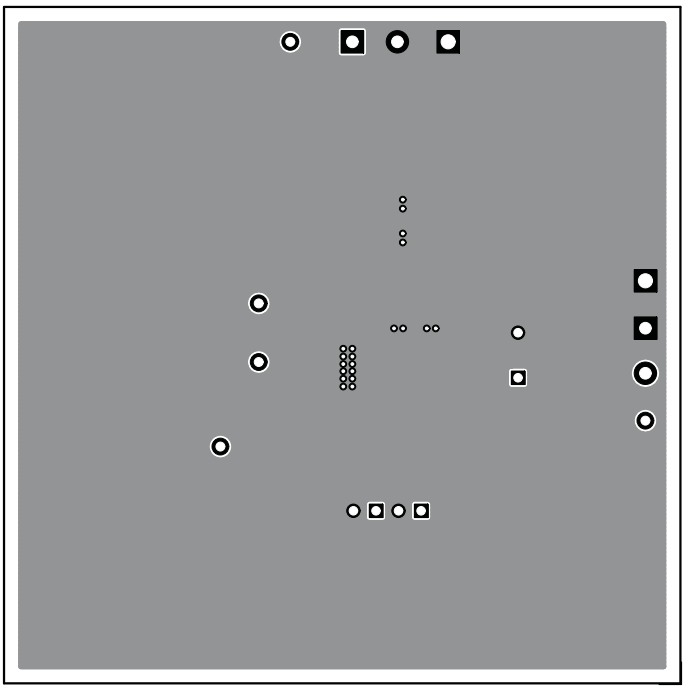

Figure 13. TPS54617EVM-414 Top-Side Assembly

3.2 Estimated Circuit Area

The estimated printed circuit board area for the components used in this design is 0.55 in^2. This area does not include test point or connectors.

4 Schematic and Bill of Materials

This section presents the TPS54617EVM-414 schematic and bill of materials.

4.1 Schematic

Figure 14 is the schematic for the TPS54617EVM-414.

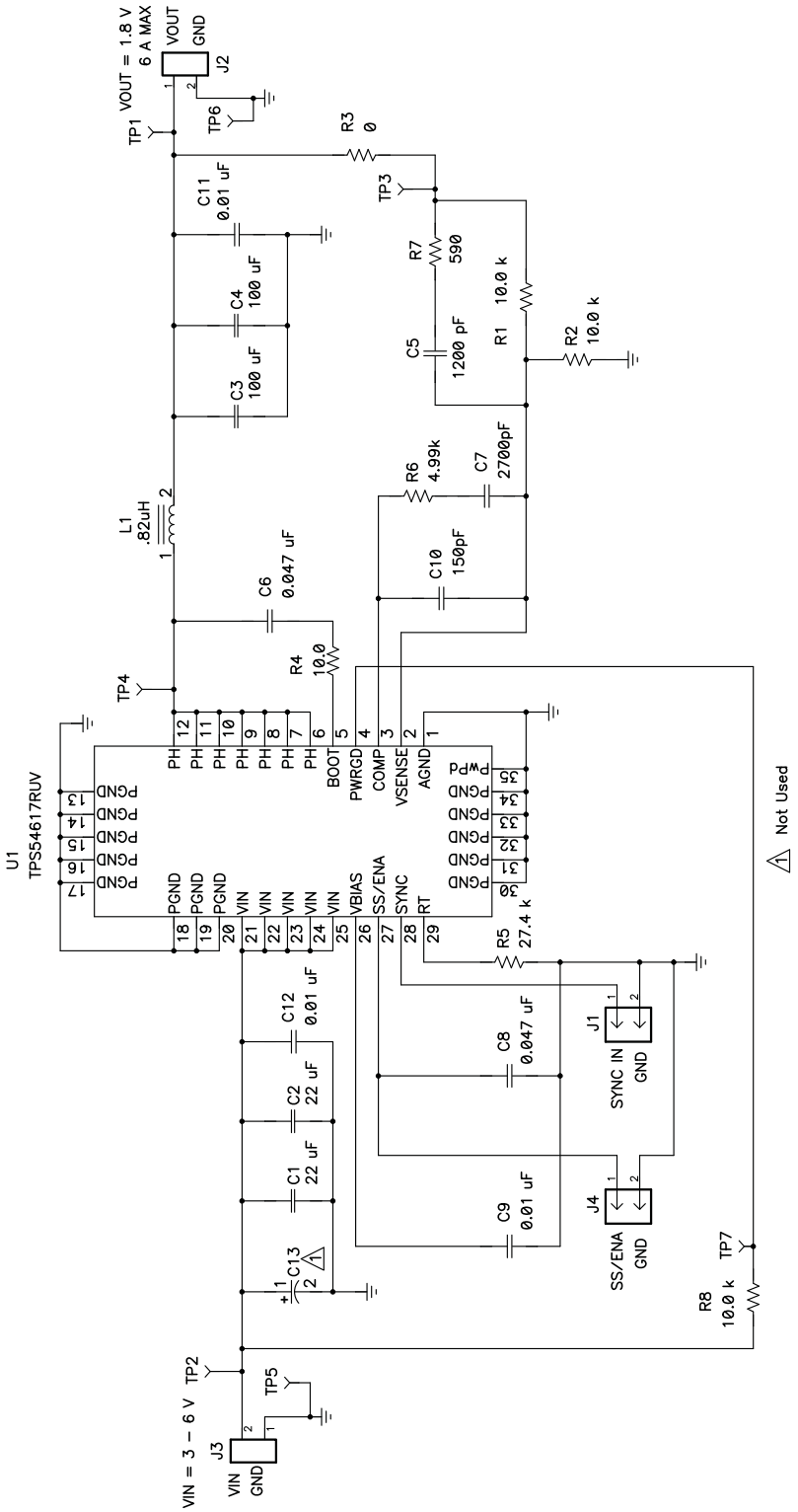

Figure 14. TPS54617EVM-414 Schematic

4.2 Bill of Materials

Table 5 presents the bill of materials for the TPS54617EVM-414.

Table 5. TPS54617EVM-414 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	—		Shunt, 100-mil, Black	0.100	929950-00	3M
2	C1, C2	22 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	1210	GRM32DR60J22KA01	Murata
1	C10	150 pF	Capacitor, Ceramic, 50V, NPO, 5%	0603	Std	Std
0	C13	Open	Capacitor, Interference Suppression, xx µF, 275 VAC	0.394 inch	STD	Sanyo
1	C3, C4	100 µF	Capacitor, Ceramic, 6.3V, X5R	1210	C3225X5R0J107M	TDK
1	C5	1200 pF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std	Std
2	C6, C8	0.047 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std	Std
1	C7	2700pF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std	Std
3	C9, C11, C12	0.01 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	Std	Std
2	J1, J4	PTC36SAAN	Header, Male 2-pin, 100mil spacing, (36-pin strip)	0.100 inch × 2	PTC36SAAN	Sullins
2	J2, J3	ED1609	Terminal Block, 2-pin, 15-A, 5,1mm	0.40" x 0.35"	ED1609	OST
1	L1	0.82µH	Inductor, SMT, 13A, 6.7 mΩ	0.255 × 0.270 inch	IHLP2525CZERR82M	Vishay
3	R1, R2, R8	10.0 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	10	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	27.4 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	4.99k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	590	Resistor, Chip, 1/16W, 1%	0603	Std	Std
4	TP1–TP4	5000	Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100 inch	5000	Keystone
2	TP5, TP6	5006	Test Point, Black, Thru Hole Compact Style	0.125 × 0.125 inch	5006	Keystone
1	TP7	5001	Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100 inch	5001	Keystone
1	U1	TPS54617RUV	IC, 3V TO 6V Input, 6A, Small synchronous-buck	RUV-34	TPS54617RUV	TI
1	—		PCB	3" × 3" × 0.062"	HPA414	Any

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no-clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Reference designators marked with an asterisk (**) cannot be substituted. All other components can be substituted with equivalent MFR's components.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range and the output current range specified in Table 1.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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