

54ABT16244

54ABT16244 16-Bit Buffer/Line Driver with TRI-STATE Outputs



Literature Number: SNOS050A

16-Bit Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'ABT16244 contains sixteen non-inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

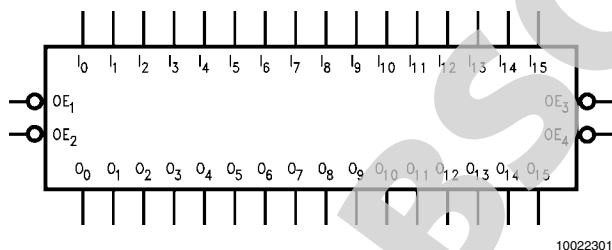
Features

- Separate control logic for each nibble
- 16-bit version of the 'ABT244
- Outputs sink capability of 48 mA, source capability of 24 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9317402

Ordering Code

Military	Package Number	Package Description
54ABT16244W-QML	WA48A	48-Lead Cerpack

Logic Symbol

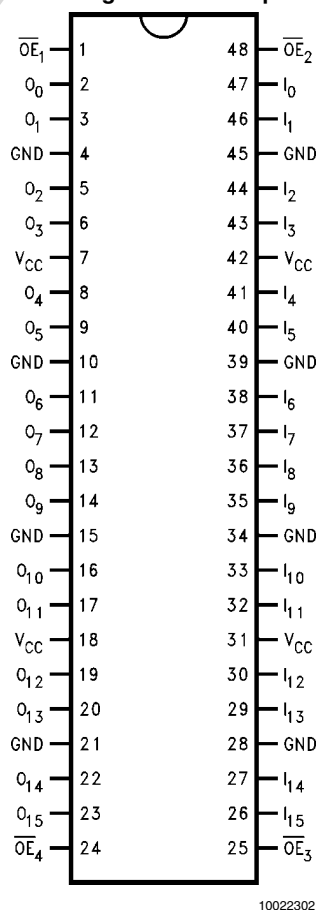


Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active Low)
I_0-I_{15}	Inputs
O_0-O_{15}	Outputs

Connection Diagram

Pin Assignment for Cerpack



Functional Description

The 'ABT16244 contains sixteen non-inverting buffers with TRI-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Table

Inputs		Outputs
$\overline{OE}_1$	I_0-I_3	O_0-O_3
L	L	L
L	H	H
H	X	Z

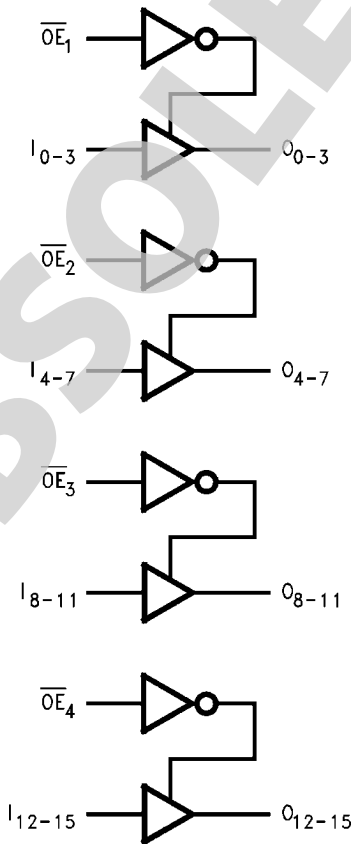
Inputs		Outputs
$\overline{OE}_3$	I_8-I_{11}	O_8-O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4-I_7	O_4-O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	$I_{12}-I_{15}$	$O_{12}-O_{15}$
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



10022303

Absolute Maximum Ratings (Note 1)

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	
Ceramic	–55°C to +175°C
V _{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-off State	–0.5V to 5.5V
in the HIGH State	–0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

DC Latchup Source Current	–500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	–55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	ABT16244			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			–1.2	V	Min	I _{IN} = –18 mA
V _{OH}	Output HIGH Voltage	54ABT	2.5		V	Min	I _{OH} = –3 mA
		54ABT	2.0		V	Min	I _{OH} = –24 mA
V _{OL}	Output LOW Voltage	54ABT		0.55	V	Min	I _{OL} = 48 mA
I _{IH}	Input HIGH Current			5	μA	Max	V _{IN} = 2.7V (Note 3)
				5			V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			–5	μA	Max	V _{IN} = 0.5V (Note 3)
				–5			V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OZH}	Output Leakage Current			50	μA	0 – 5.5V	V _{OUT} = 2.7V; $\overline{OE}_n = 2.0V$
I _{OZL}	Output Leakage Current			–50	μA	0 – 5.5V	V _{OUT} = 0.5V; $\overline{OE}_n = 2.0V$
I _{OS}	Output Short-Circuit Current	–100		–275	mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output High Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test			100	μA	0.0	V _{OUT} = 5.5V All Other Pins GND
I _{CCH}	Power Supply Current			2.0	mA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			60	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			2.0	mA	Max	$\overline{OE}_n = V_{CC}$ All Others at V _{CC} or GND
I _{CCT}	Additional I _{CC} /Input	Outputs Enabled	2.5	mA			V _I = V _{CC} – 2.1V
		Outputs TRI-STATE	2.5	mA	Max		Enable Input V _I = V _{CC} – 2.1V
		Outputs TRI-STATE	50	μA			Data Input V _I = V _{CC} – 2.1V All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC} (Note 3)	No Load		0.1	mA/ MHz	Max	Outputs Open, $\overline{OE}_n = GND$ One Bit Toggling, 50% Duty Cycle

Note 3: Guaranteed but not tested.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V _{CC}	Conditions C _L = 50 pF, R _L = 500Ω
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}		1.1	V	5.0	T _A = 25°C (<i>Note 4</i>)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}		-0.45	V	5.0	T _A = 25°C (<i>Note 4</i>)

Note 4: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW.

AC Electrical Characteristics

Symbol	Parameter	54ABT		Units	Fig. No.
		T _A = -55°C to +125°C V _{CC} = 4.5V-5.5V C _L = 50 pF			
		Min	Max		
t _{PLH}	Propagation	0.5	5.3	ns	Figure 2
t _{PHL}	Delay Data to Outputs	0.5	5.9		
t _{PZH}	Output Enable	1.5	6.8	ns	Figure 5
t _{PZL}	Time	1.5	7.0		
t _{PHZ}	Output Disable	1.5	7.7	ns	Figure 5
t _{PLZ}	Time	1.5	6.5		

Capacitance

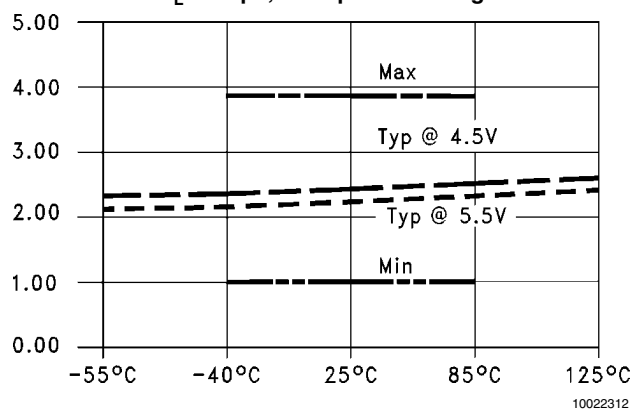
Symbol	Parameter	Typ	Units	Conditions T _A = 25°C
C _{IN}	Input Capacitance	5.0	pF	V _{CC} = 5.0V
C _{OUT} (<i>Note 5</i>)	Output Capacitance	9.0	pF	V _{CC} = 5.0V

Note 5: C_{OUT} is measured at frequency f = 1 MHz; per MIL STD-883B, Method 3012.

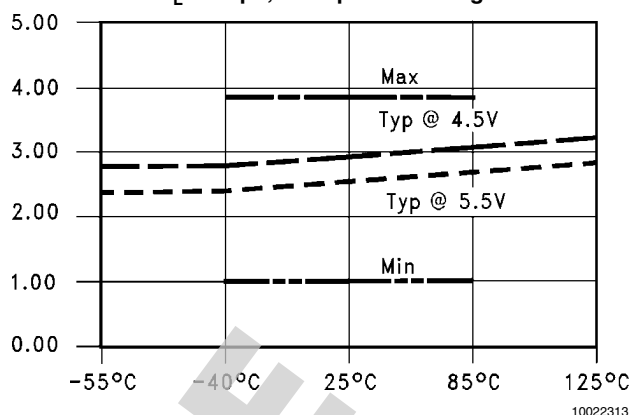
Capacitance

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

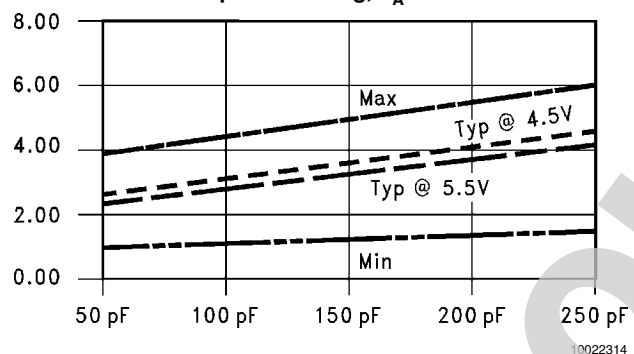
t_{PLH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



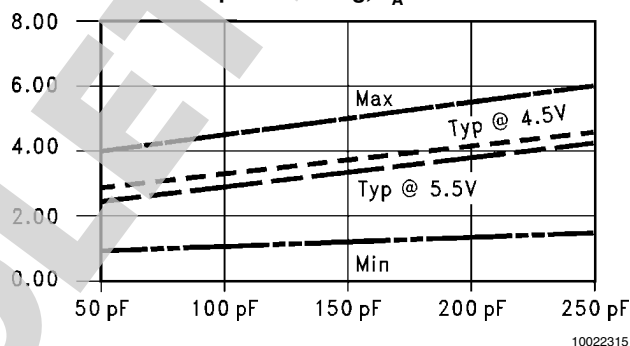
t_{PHL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



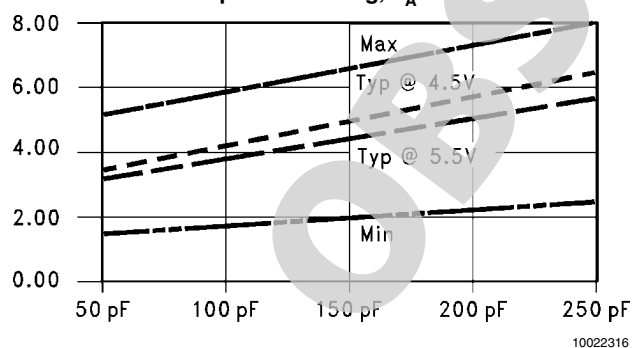
t_{PLH} vs Load Capacitance
 1 Output Switching, $T_A = 25^\circ\text{C}$



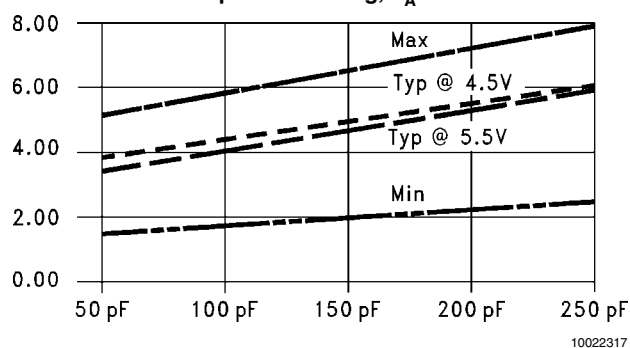
t_{PHL} vs Load Capacitance
 1 Output Switching, $T_A = 25^\circ\text{C}$



t_{PLH} vs Load Capacitance
 16 Outputs Switching, $T_A = 25^\circ\text{C}$

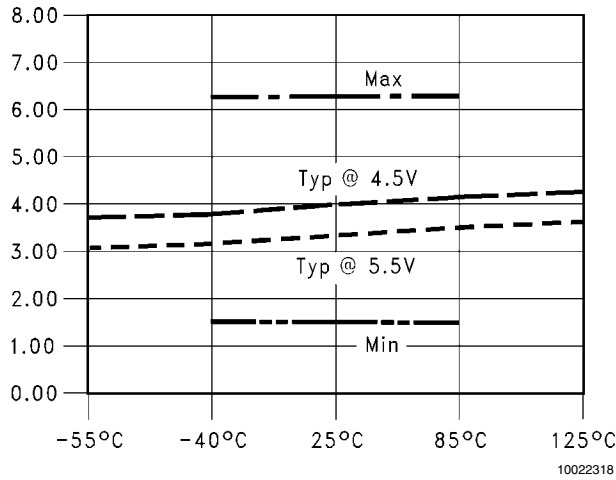


t_{PHL} vs Load Capacitance
 16 Outputs Switching, $T_A = 25^\circ\text{C}$

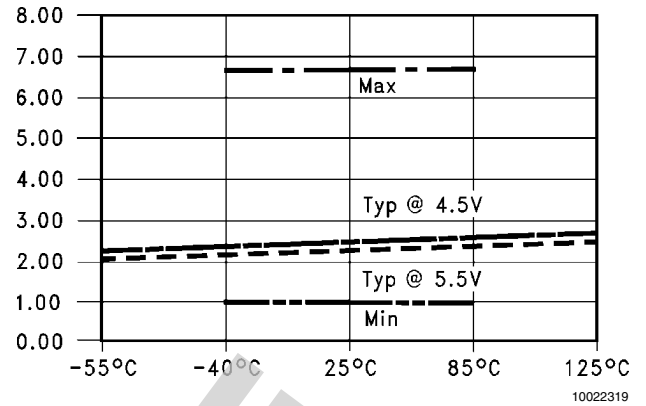


Note: Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

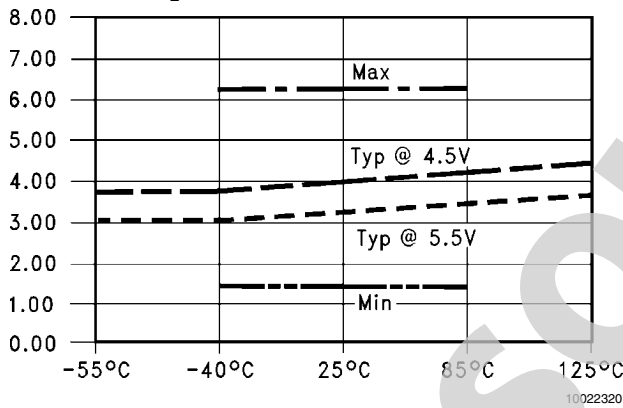
t_{pZL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



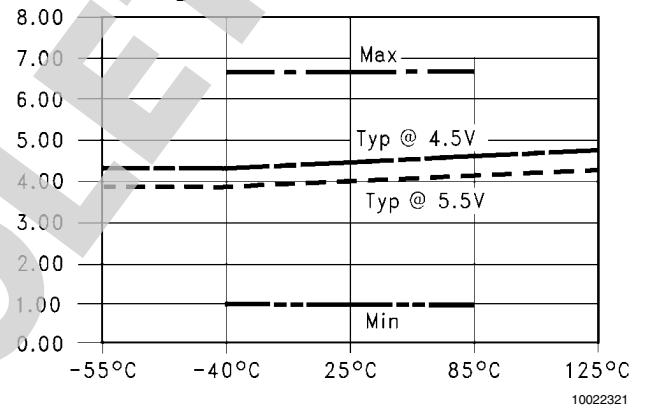
t_{pLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



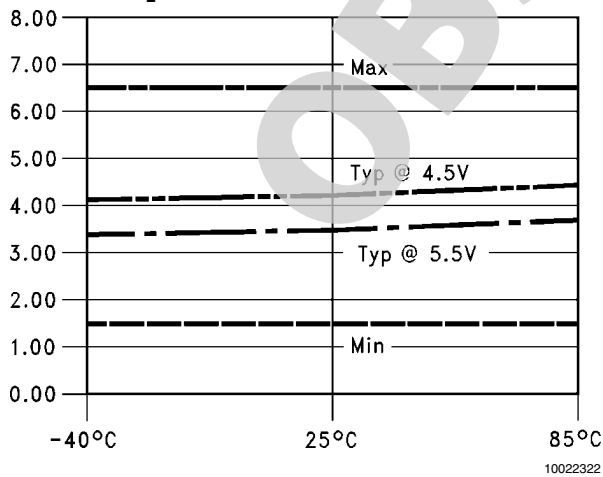
t_{pZH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



t_{pHZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching

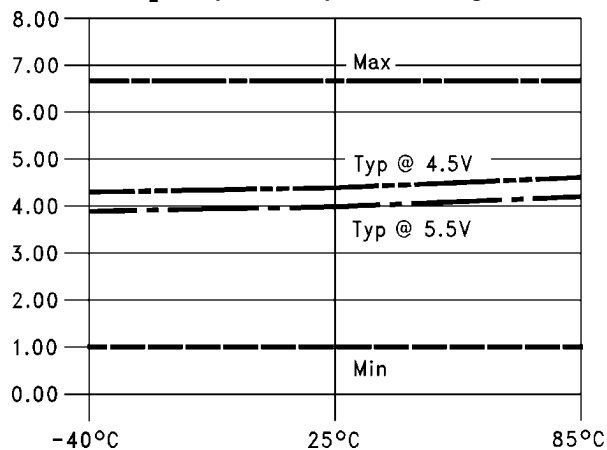


t_{pZH} vs Temperature (T_A)
 $C_L = 50$ pF, 16 Outputs Switching



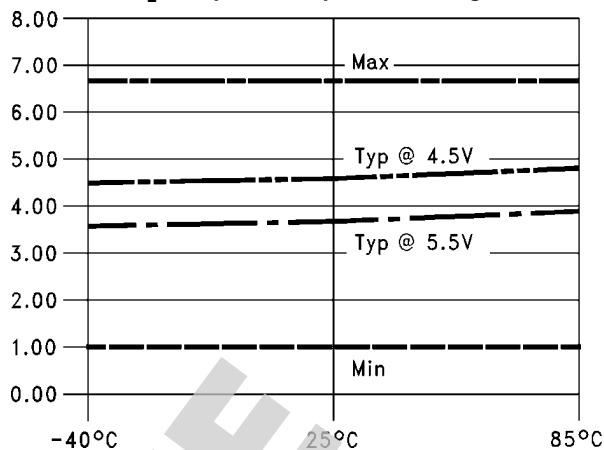
Note: Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

t_{PHZ} vs Temperature (T_A)
 $C_L = 50$ pF, 16 Outputs Switching



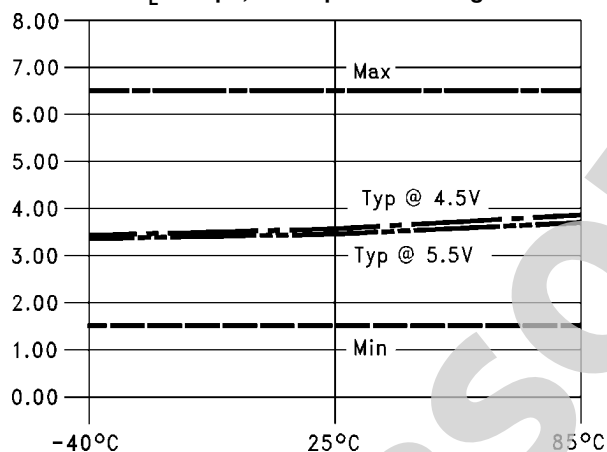
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t_{PZL} vs Temperature (T_A)
 $C_L = 50$ pF, 16 Outputs Switching



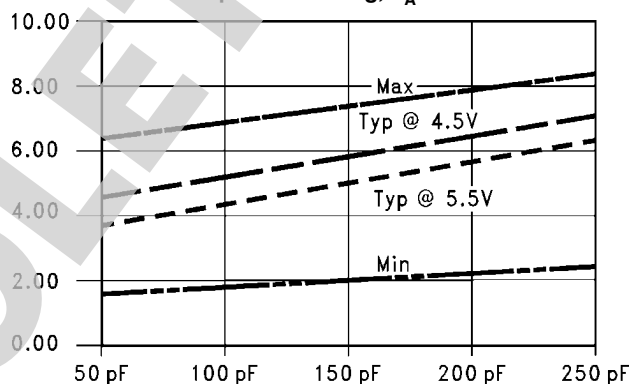
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t_{PLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 16 Outputs Switching



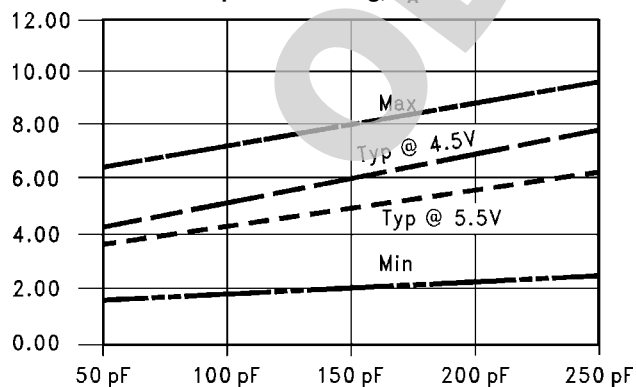
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t_{PZL} vs Load Capacitance
 16 Outputs Switching, $T_A = 25^\circ\text{C}$



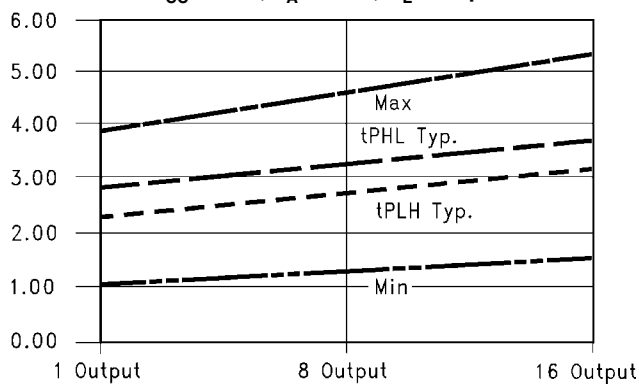
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t_{PZH} vs Load Capacitance
 16 Outputs Switching, $T_A = 25^\circ\text{C}$



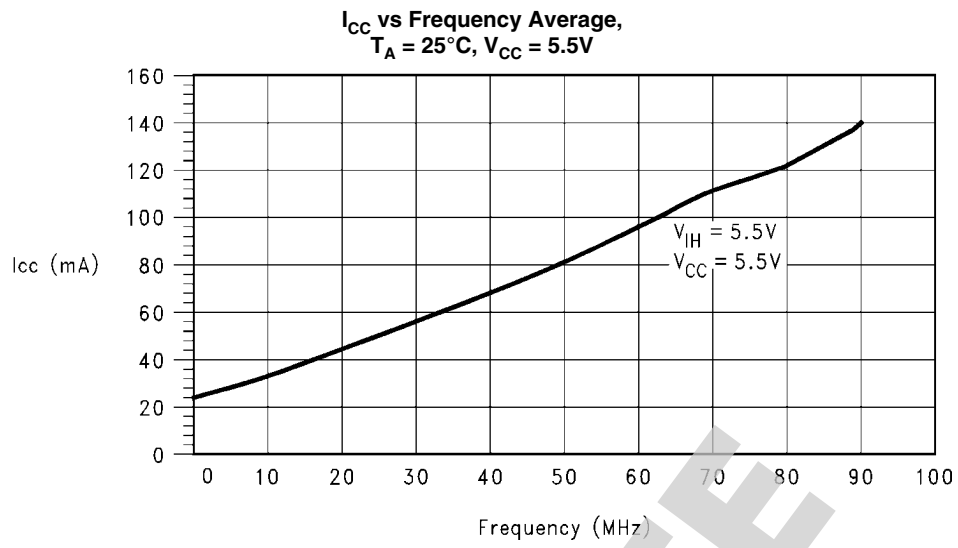
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t_{PLH} and t_{PHL} vs Number Output Switching
 $V_{CC} = 5.0\text{V}$, $T_A = 25^\circ\text{C}$, $C_L = 50$ pF



10022328

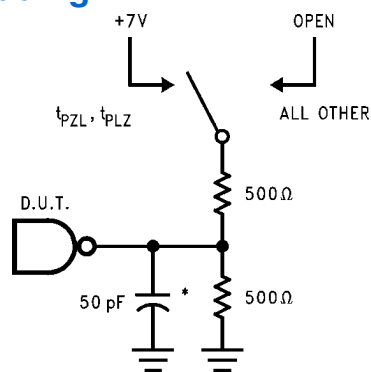
Note: Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.



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AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

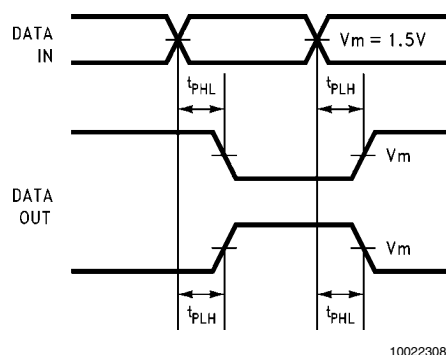


FIGURE 2. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

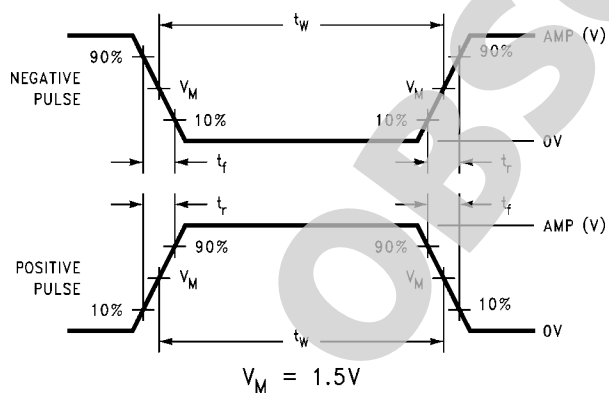


FIGURE 3. Test Input Pulse Requirements

Amplitude	Rep Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 4. Test Input Signal Requirements

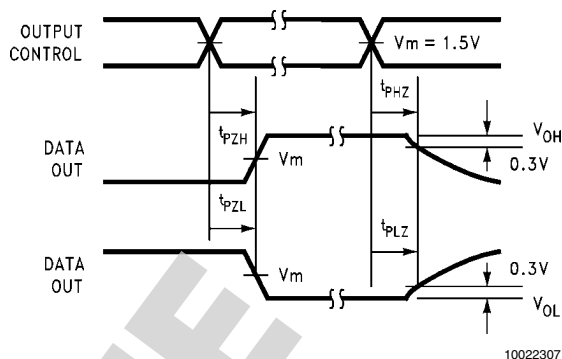
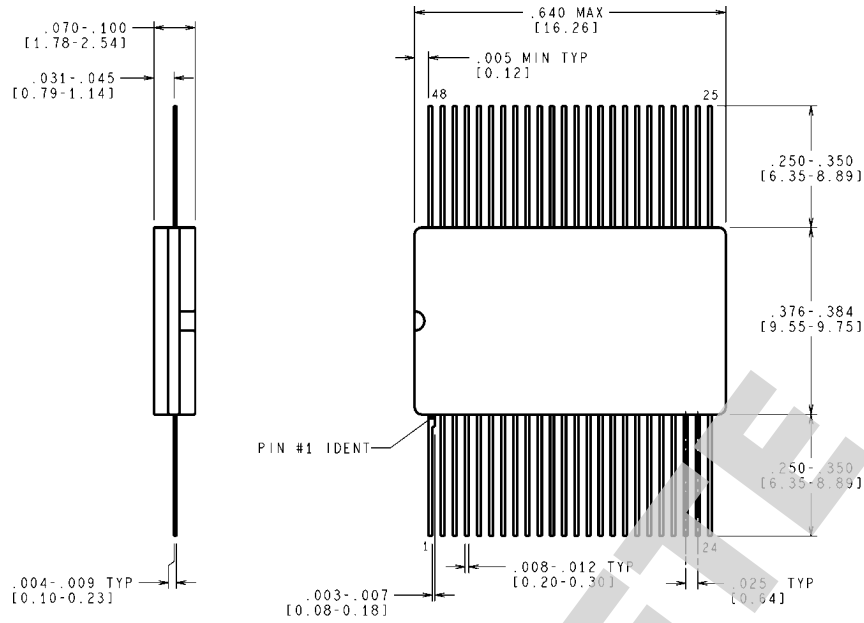


FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times

Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

48-Lead Cerpack
NS Package Number WA48A

WA48A (Rev B)

Notes

OBSOLETE

Notes

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