CY7C1049CV33

4-Mbit (512K X 8) Static RAM

Features

- Temperature ranges
  - Commercial: 0°C to 70°C
  - Industrial/Automotive -A: –40°C to 85°C
  - Automotive-E: –40°C to 125°C
- High speed
  - t_{AA} = 10 ns
- Low active power
  - 324 mW (max)
- 2.0 V data retention
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features

Functional Description

The CY7C1049CV33 is a high performance CMOS Static RAM organized as 524,288 words by eight bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

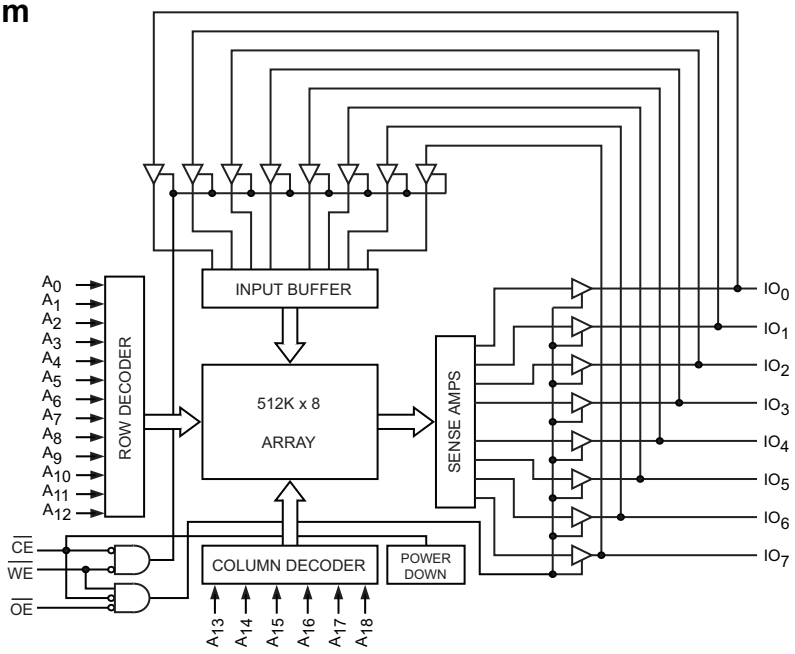
Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1049CV33 is available in standard 400-mil-wide 36-pin SOJ package and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Logic Block Diagram



Contents

Selection Guide

Description		-10	-12	-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Commercial	90	85	-	mA
	Industrial/Automotive-A	100	95	-	mA
	Automotive-E	-	-	95	mA
Maximum CMOS Standby Current	Commercial/Industrial/ Automotive-A	10	10	-	mA
	Automotive-E	-	-	15	mA

Pin Configuration

Figure 1. 36-Pin SOJ (Top View)

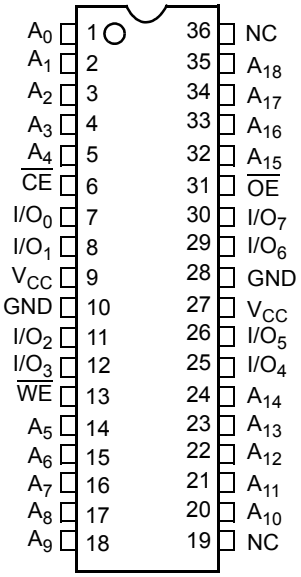
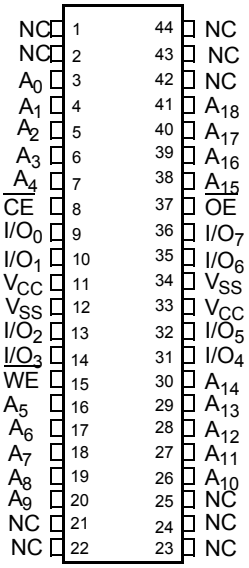


Figure 2. 44-Pin TSOP II (Top View)



Pin Definitions

Pin Name	36 SOJ Pin Number	44 TSOP II Pin Number	I/O Type	Description
A_0–A_{18}	1–5,14–18, 20–24,32–35	3–7,16–20, 26–30,38–41	Input	**Address inputs used to select one of the address locations.**
I/O_0–I/O_7	7,8,11,12,25, 26,29,30	9,10,13,14, 31,32,35,36	Input/Output	**Bidirectional data I/O lines.** Used as input or output lines depending on operation
NC[1]	19,36	1,2,21,22,23,2 4,25,42,43, 44	No Connect	**No connects.** This pin is not connected to the die
$\overline{WE}$	13	15	Input/Control	**Write Enable input, active LOW.** When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
$\overline{CE}$	6	8	Input/Control	**Chip Enable input, active LOW.** When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	31	37	Input/Control	**Output Enable, active LOW.** Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins.
V_{SS}, GND	10,28	12,34	Ground	**Ground for the device.** Should be connected to ground of the system.
V_{CC}	9,27	11,33	Power Supply	**Power supply inputs to the device.**

Note
1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] ..... –0.5 V to +4.6 VDC

Voltage Applied to Outputs in High Z State[2] ..... –0.5 V to V_{CC} + 0.5 V

Input Voltage[2] ..... –0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3 V ± 0.3 V
Industrial/ Automotive-A	–40°C to +85°C	
Automotive-E	–40°C to +125°C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10		-12		-15		Unit
				Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min.; I_{OH} = –4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.,; I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[2]			–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	Com'l/Ind'l/ Auto-A	–1	+1	–1	+1			µA
			Auto-E					–20	+20	
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$	Com'l		90		85			mA
			Ind'l/Auto-A		100		95			
			Auto-E						95	
I_{SB1}	Automatic CE Power Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}; V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l/Ind'l/ Auto-A		40		40			mA
			Auto-E						45	mA
I_{SB2}	Automatic CE Power Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0	Com'l/Ind'l/ Auto-A		10		10			mA
			Auto-E						15	mA

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3 V	8	pF
C_{OUT}	I/O Capacitance		8	pF

Thermal Resistance

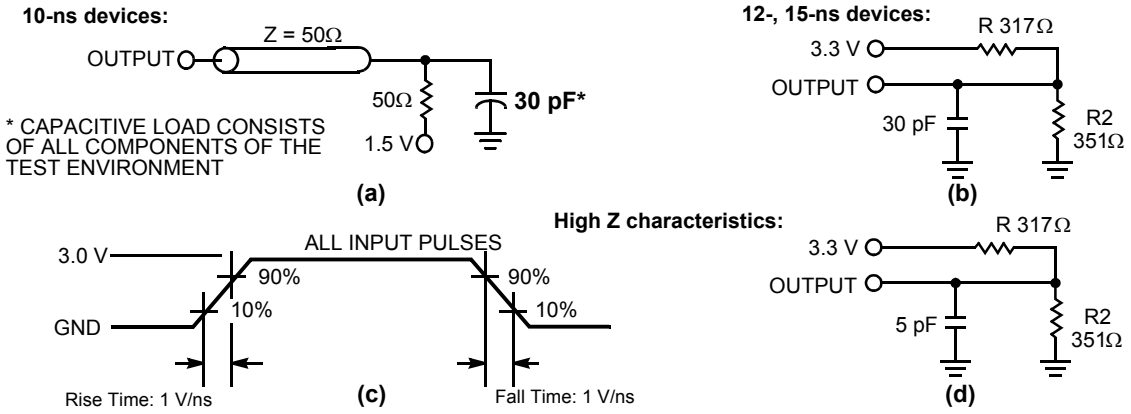
Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	36-Pin SOJ	44-TSOP-II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	46.51	41.66	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		18.8	10.56	°C/W

Notes

2. V_{IL} (min) = –2.0 V and V_{IH}(max) = V_{CC} + 0.5 V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.

Figure 3. AC Test Loads and Waveforms [4]



Notes

4. Tested initially and after any design or process changes that may affect these parameters.
5. AC characteristics (except High Z) for 10 ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High Z characteristics are tested for all speeds using the test load shown in Figure (d).

AC Switching Characteristics

Over the Operating Range [6]

Parameter	Description	-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t_{power} [7]	V_{CC}(typical) to the first access	100		100		100		µs
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3			3	ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [8, 9]		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [9]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [8, 9]		5		6		7	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		10		12		15	ns
Write Cycle [10, 11]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		8		10		ns
t_{AW}	Address Setup to Write End	7		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Setup to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		10		ns
t_{SD}	Data Setup to Write End	5		6		7		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [9]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [8, 9]		5		6		7	ns

Notes

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
7. t_{POWER} gives the minimum amount of time that the power supply should be at stable, typical V_{CC} values until the first memory access can be performed.
8. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
10. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the Write.
11. The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [12, 13]

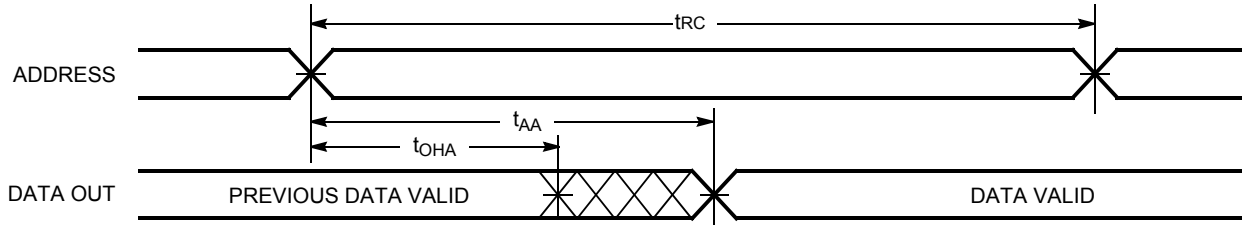


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [13, 14]

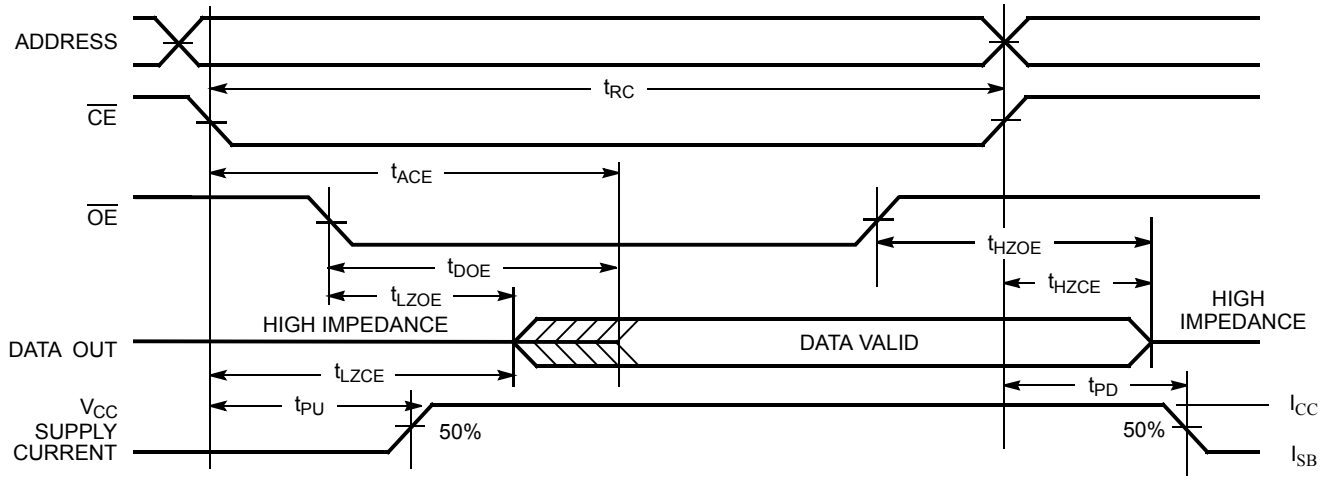
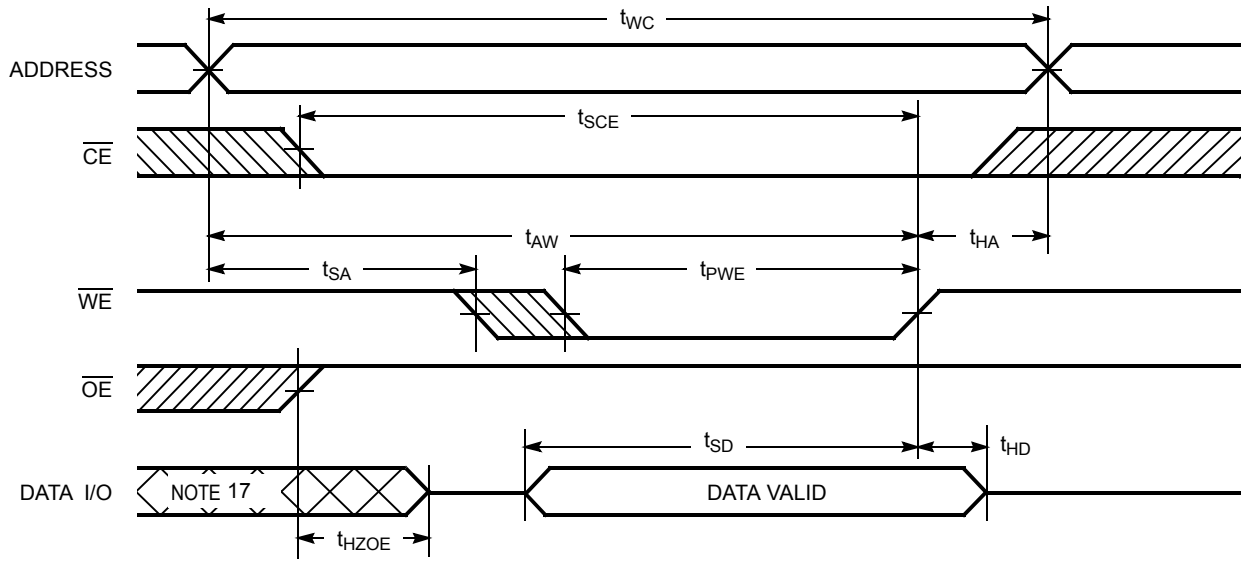


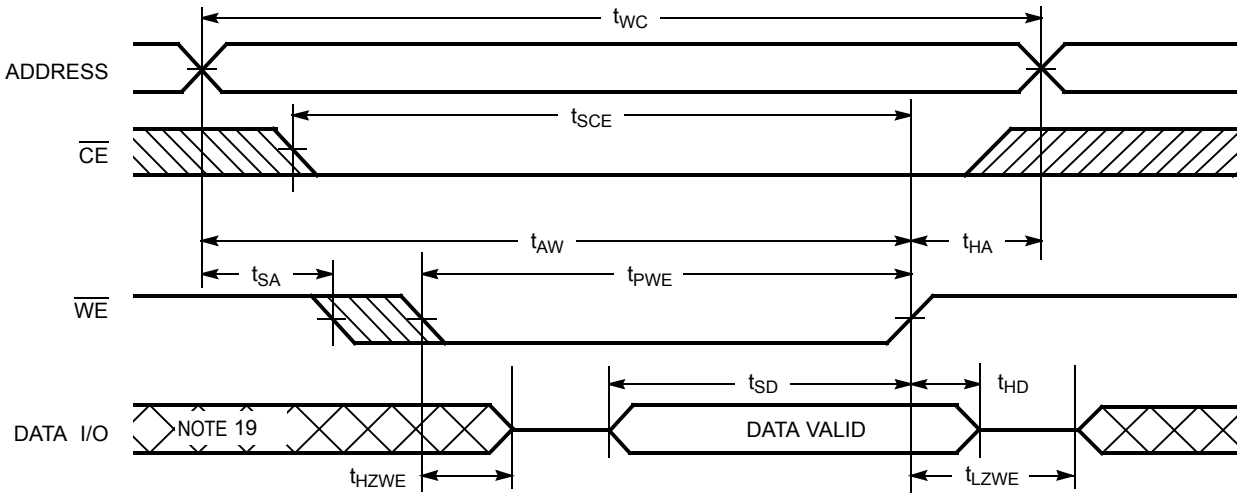
Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [15, 16]



Notes
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycles.
14. Address valid before or similar to $\overline{CE}$ transition LOW.
15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
17. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [18]



Truth Table

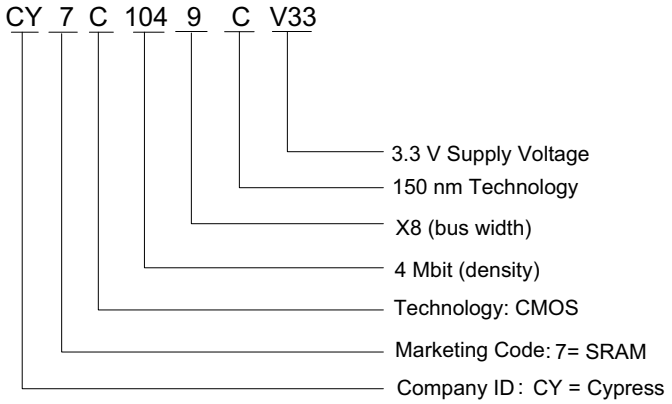
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	High Z	Power Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Notes
18. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
19. During this period, the I/Os are in output state. Do not apply input signals.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1049CV33-10VXA	51-85090	36-Pin (400-Mil) Molded SOJ (Pb-free)	Automotive-A
12	CY7C1049CV33-12ZSXA	51-85087	44-Pin TSOP II (Pb-free)	Automotive-A
15	CY7C1049CV33-15VXE	51-85090	36-Pin (400-Mil) Molded SOJ (Pb-free)	Automotive-E
	CY7C1049CV33-15ZSXE	51-85087	44-Pin TSOP II (Pb-free)	Automotive-E

Ordering Code Definitions



Package Diagrams

Figure 8. 36-Pin (400-Mil) Molded SOJ, 51-85090

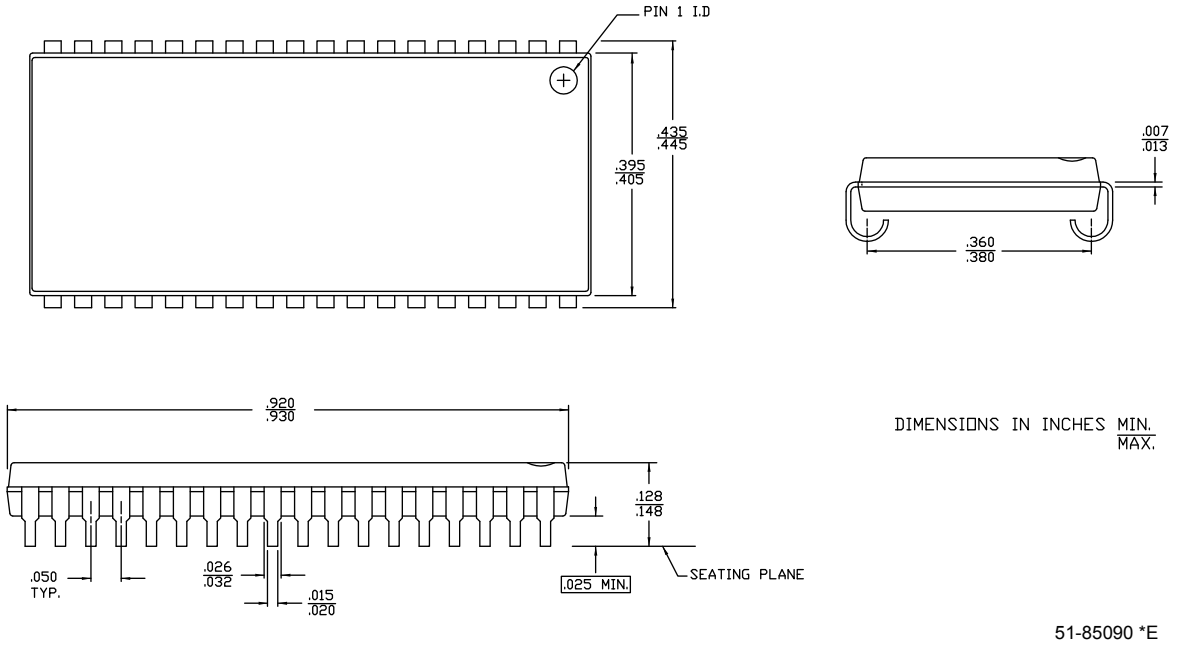
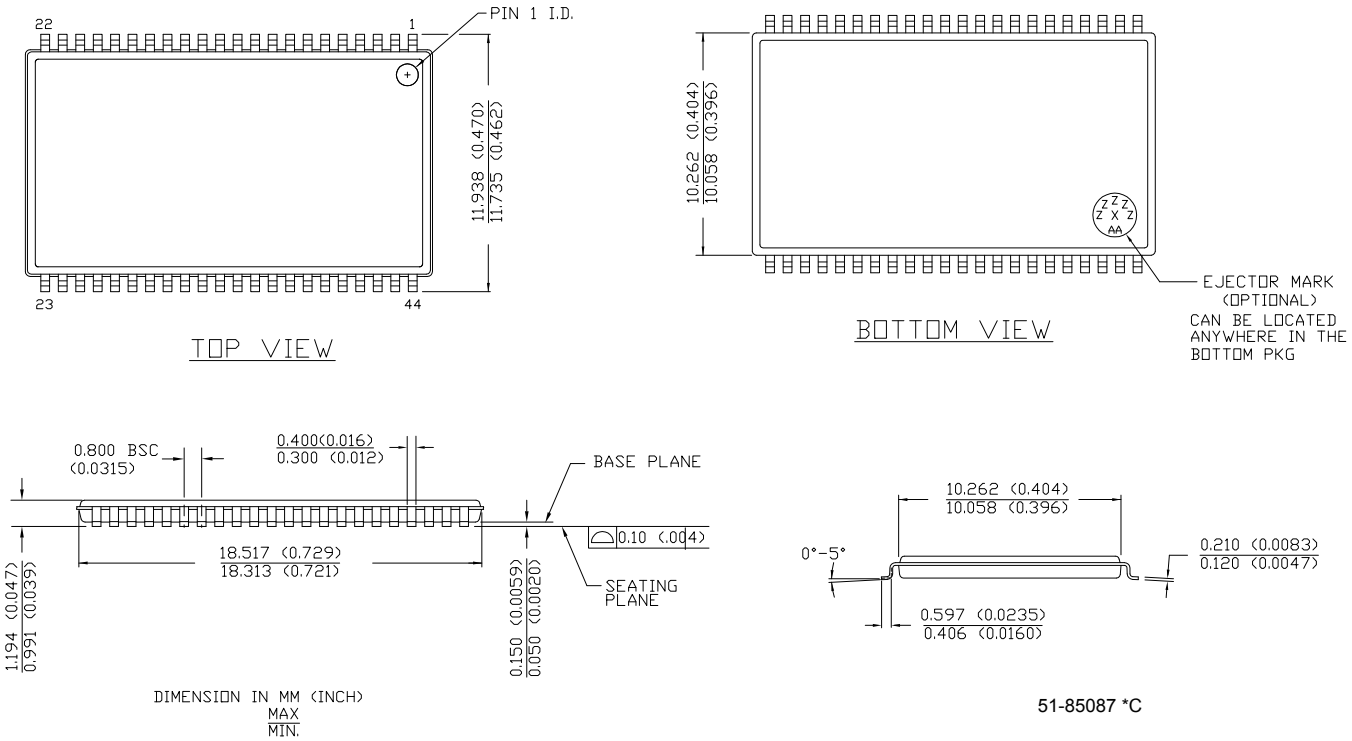


Figure 9. 44-Pin TSOP II, 51-85087



Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
TR	Thermal Resistance
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
RD	Row Decoder
IB	Input Buffer
RAM	Random Access Memory
I/O	Input/Output
MAT	Maximum Access Time
MOC	Maximum Operating Current

Document History Page

Document Title: CY7C1049CV33 4-Mbit (512K X 8) Static RAM Document Number: 38-05006				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	112569	HGK	03/06/02	New data sheet
*A	114091	DFP	04/25/02	Changed Tpower unit from ns to μs
*B	116479	CEA	09/16/02	Add applications foot note to data sheet, page 1.
*C	262949	RKF	See ECN	Added Automotive-E Specs Added Θ_{JA} and Θ_{JC} values on Page #3.
*D	300091	RKF	See ECN	Added -20-ns Speed bin
*E	344595	SYT	See ECN	Added Pb-free package on page #8 Removed shading for CY7C1049CV33-15ZSXE in the ordering Information on page 9
*F	2615344	VKN/PYRS	12/03/08	Added Automotive-A information Removed 8 ns and 20 ns speed bins, Changed t_{POWER} spec from 1 μs to 100 μs, Updated Ordering Information table.
*G	2841563	NXR/	01/07/2010	Added CY7C1049CV33-10VXA to Ordering Info table.
*H	2898958	AJU	03/25/10	Removed inactive parts from the ordering informaiton table. Updated package diagrams.
*I	2954734	AJU	06/30/2010	New Part Number added CY7C1049CV33-10ZXC to Ordering Info table.
*J	3072834	PRAS	11/12/2010	Removed obsolete parts and updated package diagram Figure 8 on page 10.

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