

LP4950C-5V and LP4951C Adjustable Micropower Voltage Regulators

Check for Samples: LP4950C-5V, LP4951C

FEATURES

- High Accuracy 5V Specified 100mA Output
- Extremely Low Quiescent Current
- Low Dropout Voltage
- Extremely Tight Load and Line Regulation
- Very Low Temperature Coefficient
- Use as Regulator or Reference
- Needs Only 1µF for Stability
- Current and Thermal Limiting

LP4951C VERSIONS ONLY

- Error Flag Warns of Output Dropout
- Logic-controlled Electronic Shutdown
- Output Pogrammable From 1.24 to 29V

DESCRIPTION

The LP4950C and LP4951C are micropower voltage regulators with very low quiescent current (75µA typ.) and very low dropout voltage (typ. 40mV at light loads and 380mV at 100mA). They are ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the LP4950C/LP4951C increases only slightly in dropout, prolonging battery life.

The LP4950C in the popular 3-pin TO-92 package is pin compatible with older 5V regulators. The 8-lead LP4951C is available in a plastic surface mount package and offers additional system functions.

One such feature is an error flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strapped for a 5V output or programmed from 1.24V to 29V with an external pair of resistors.

Careful design of the LP4950C/LP4951C has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typ.), extremely good load and line regulation (.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

BLOCK DIAGRAM AND TYPICAL APPLICATIONS

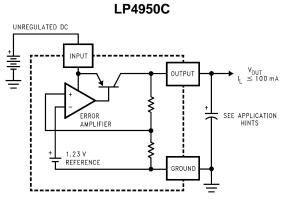


Figure 1.

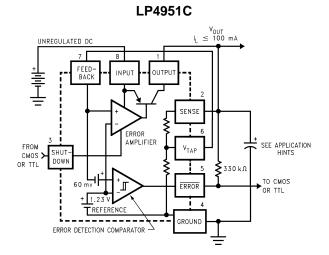


Figure 2.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)

Input Supply Voltage	-0.3 to +30V
SHUTDOWN Input Voltage, Error Comparator Output Voltage, ⁽²⁾	-0.3 to +30V
FEEDBACK Input Voltage (2) (3)	−1.5 to +30V
Power Dissipation	Internally Limited
Junction Temperature (T _J)	+150°C
Ambient Storage Temperature	−65° to +150°C
ESD Rating Human Body Model ⁽⁴⁾	2 kV
For soldering specifications, see the following document: www.ti.com/lit/snoa549	

- (1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) May exceed input supply voltage.
- (3) When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.
- (4) Human Body Model 1.5 kΩ in series with 100 pF. LP4950 passes 2 kV HBM. LP4951 All pins pass 2 kV except Vfb -1000V.

OPERATING RATINGS (1)

Maximum Input Supply Voltage	30V
Junction Temperature Range ⁽²⁾	
LP4950C, LP4951C	-40°C to 125°C

- (1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) The junction-to-ambient thermal resistances are as follows: 180°C/W and 160°C/W for the TO-92 package with 0.40 inch and 0.25 inch leads to the printed circuit board (PCB) respectively, 160°C/W for the molded plastic SOIC (D). The above thermal resistances for the SOIC package apply when the package is soldered directly to the PCB.

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ELECTRICAL CHARACTERISTICS (1)

	LP4950CZ						
.	Conditions		LP4951CM		Units		
Parameter	(1)		Tested	Design			
		Тур	Limit ⁽²⁾	Limit ⁽³⁾	Í		
Output Voltage	T _J = 25°C	5.0	5.1		V max		
			4.9		V min		
	-25°C ≤ T _J ≤ 85°C			5.15	V max		
				4.85	V min		
	Full Operating Temperature Range			5.2	V max		
				4.8	V min		
Output Voltage	100 μA ≤ I _L ≤ 100 mA			5.24	V max		
	$T_{J} \leq T_{JMAX}$			4.76	V min		
Output Voltage Temperature Coefficient	(4)			150	ppm/°C		
Line Regulation ⁽⁵⁾	6V ≤ V _{IN} ≤ 30V ⁽⁶⁾	0.04	0.2		% max		
				0.4	% max		
Load Regulation ⁽⁵⁾	100μA ≤ I _L ≤ 100mA	0.1	0.2		% max		
				0.3	% max		
Dropout Voltage ⁽⁷⁾	I _L = 100μA	50	80		mV max		
				150	mV max		
	I _L = 100mA	380	450		mV max		
				600	mV max		
Ground Current	I _L = 100μA	75	150		μA max		
				170	μA max		
	I _L = 100mA	8	15		mA max		
				19	mA max		
Dropout Ground Current	V _{IN} = 4.5V	110	200		μA max		
	I _L = 100μA			230	μA max		
Current Limit	V _{OUT} = 0	160	200		mA max		
				220	mA max		
Thermal Regulation	(8)	0.05	0.2		%/W max		
Output Noise, 10 Hz to 100 kHz	C _L = 1µF	430			μV rms		
	C _L = 200µF	160			μV rms		
	$C_L = 3.3 \mu F$ (Bypass = $0.01 \mu F$ Pins 7 to 1 (LP4951C)	100			μV rms		

- (1) Unless otherwise noted all limits specified for V_{IN} = 6V, I_L = 100μA and C_L = 1μF. Limits appearing in **boldface** type apply over the entire junction temperature range for operation. Limits appearing in normal type apply for T_A = T_J = 25°C. Additional conditions for the 8-pin versions are FEEDBACK tied to V_{TAP}, OUTPUT tied to SENSE (V_{OUT} = 5V), and V_{SHUTDOWN} ≤ 0.8V.
- (2) Specified and 100% production tested.
- (3) Specified but not 100% production tested. These limits are not used to calculate outgoing AQL levels.
- (4) Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
- (5) Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.
- (6) Line regulation for the LP4951C is tested at 150°C for I_L = 1 mA. For I_L = 100μA and T_J = 125°C, line regulation is specified by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.
- (7) Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2V (2.3V over temperature) must be taken into account.
- (8) Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50 mA load pulse at V_{IN} = 30V (1.25W pulse) for T = 10ms.



ELECTRICAL CHARACTERISTICS

			LP4951C			
Parameter	Conditions ⁽¹⁾	Тур	Tested Limit	Design Limit	Units	
8-PIN VERSIONS ONLY			•			
Reference Voltage		1.235	1.285		V max	
				1.295	V max	
			1.185		V min	
				1.165	Vmin	
Reference Voltage	(4)			1.335	V max	
				1.135	V min	
Feedback Pin Bias Current		20	40		nA max	
				60	nA max	
Reference Voltage Temperature Coefficient	(5)	50			ppm/°C	
Feedback Pin Bias Current Temperature Coefficient		0.1			nA/°C	
Error Comparator						
Output Leakage Current	V OH = 30V	0.01	1		μA max	
				2	μA max	
Output Low Voltage	V _{IN} = 4.5V	150	250		mV max	
	$I_{OL} = 400 \mu A$			400	mV max	
Upper Threshold Voltage	(3)	60	40		mV min	
				25	mV min	
Lower Threshold Voltage	(6)	75	95		mV max	
				140	mV max	
Hysteresis	(6)	15			mV	
Shutdown Input						
Input Logic Voltage		1.3			V	
	Low (Regulator ON)			0.7	V max	
	High (Regulator OFF)			2.0	V min	
Shutdown Pin Input Current	V _{SHUTDOWN} = 2.4V	30	50		μA max	
				100	μA max	
	V _{SHUTDOWN} = 30V	450	600		μA max	
				750	μA max	
Regulator Output Current in	(7)	3	10		µA max	
Shutdown				20	µA max	

- (1) Unless otherwise noted all limits specified for V_{IN} = 6V, I_L = 100 μ A and C_L = 1 μ F. Limits appearing in **boldface** type apply over the entire junction temperature range for operation. Limits appearing in normal type apply for T_A = T_J = 25°C. Additional conditions for the 8pin versions are FEEDBACK tied to V_{TAP}, OUTPUT tied to SENSE (V_{OUT} = 5V), and V_{SHUTDOWN} ≤ 0.8V.
- Specified and 100% production tested.
- Specified but not 100% production tested. These limits are not used to calculate outgoing AQL levels.
- (4)
- $V_{REF} \le V_{OUT} \le (V_{IN} 1V), 2.3V \le V_{IN} \le 30V, 100\mu A \le I_L \le 100mA, T_J \le T_{JMAX}.$ Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
- Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at $V_{IN} = 6V$. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT}/V_{REF} = (R1 + R2)/R2. For example, at a programmed output voltage of 5V, the Error output is specified to go low when the output drops by 95 mV \times 5V/1.235V = 384 mV. Thresholds remain constant as a percent of V_{OUT} as V_{OUT} is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% specified.
- V_{SHUTDOWN} ≥ 2V, V_{IN} ≤ 30V, V_{OUT} = 0, Feedback pin tied to V_{TAP}.



CONNECTION DIAGRAMS

OUTPUT INPUT

Figure 3. Bottom View

Surface-Mount Package (SOIC)

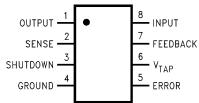
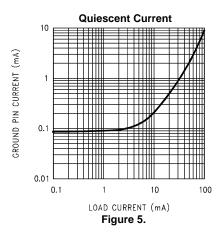
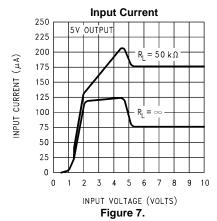


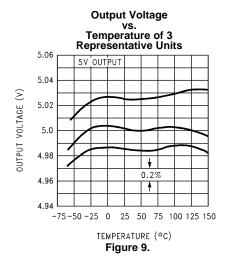
Figure 4. Top View

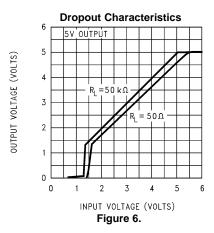


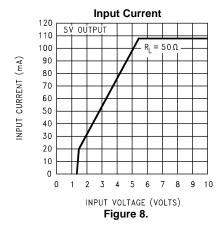
TYPICAL PERFORMANCE CHARACTERISTICS

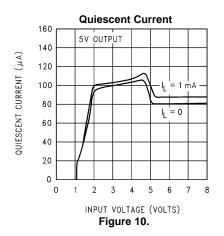














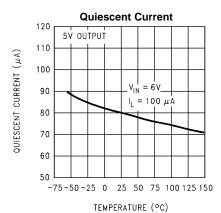
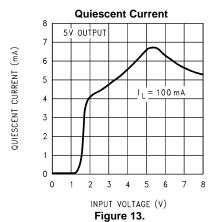
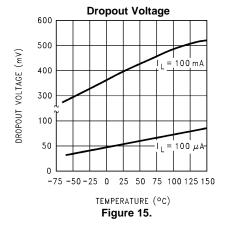


Figure 11.





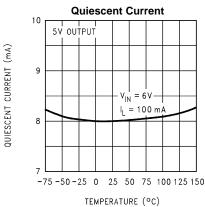
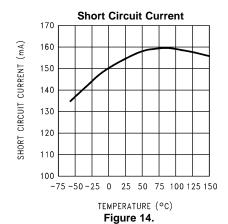


Figure 12.



Dropout Voltage

500

400

400

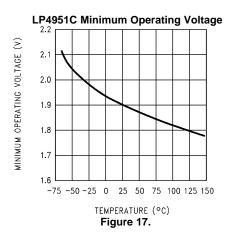
T_J = 25 °C

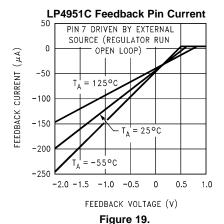
100 μA 1 mA 10 mA 100 mA

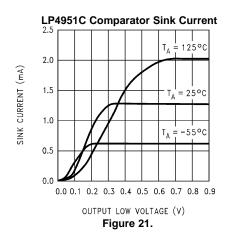
OUTPUT CURRENT

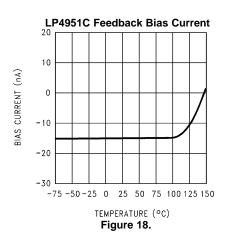
Figure 16.

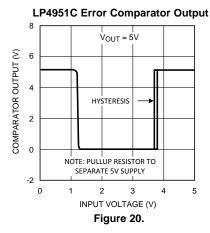


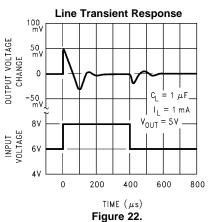




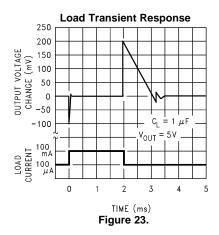


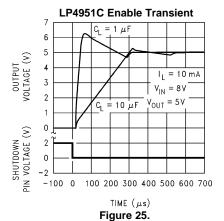


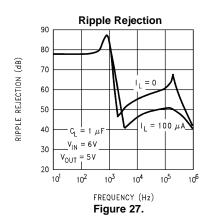


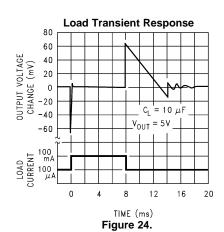












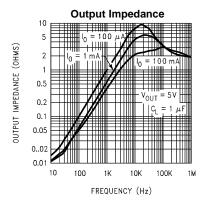
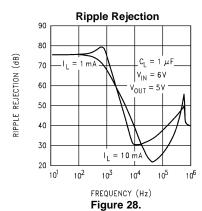


Figure 26.





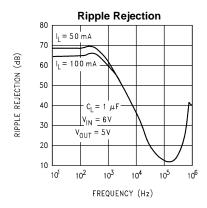
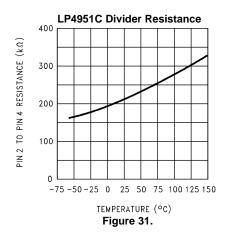
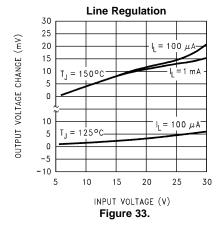


Figure 29.





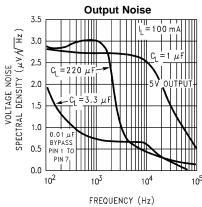
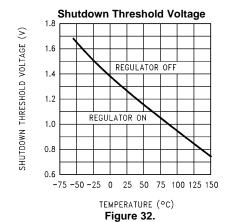


Figure 30.



LP4951C Maximum Rated Output Current

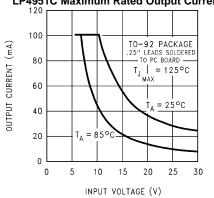
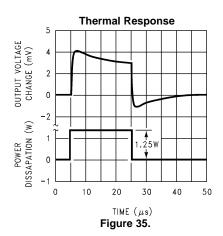


Figure 34.





APPLICATION HINTS

EXTERNAL CAPACITORS

A 1.0 μ F (or greater) capacitor is required between the output and ground for stability at output voltages of 5V or more. At lower output voltages, more capacitance is required. Without this capacitor the part will oscillate. Most types of tantalum or aluminum electrolytics work fine here; even film types work but are not recommended for reasons of cost. Many aluminum electrolytics have electrolytes that freeze at about -30° C, so solid tantalums are recommended for operation below -25° C. The important parameters of the capacitor are an ESR of about 5 Ω or less and a resonant frequency above 500 kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for stability. The capacitor can be reduced to 0.33 μ F for currents below 10 mA or 0.1 μ F for currents below 1 mA. Using the 8-pin version at voltages below 5V runs the error amplifier at lower gains so that *more* output capacitance is needed. For the worst-case situation of a 100 mA load at 1.23V output (Output shorted to Feedback) a 3.3 μ F (or greater) capacitor should be used.

Unlike many other regulators, the LP4950C will remain stable and in regulation with no load in addition to the internal voltage divider. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the LP4951C version with external resistors, a minimum load of 1µA is recommended.

A 0.1µF capacitor should be placed from the LP4950C/LP4951C input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Stray capacitance to the LP4951C Feedback terminal (pin 7) can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100pF capacitor between Output and Feedback and increasing the output capacitor to at least 3.3µF will fix this problem.

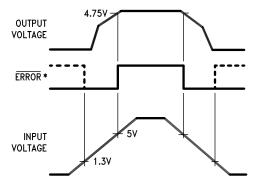
ERROR DETECTION COMPARATOR OUTPUT

The comparator produces a logic low output whenever the LP4951C output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60 mV divided by the 1.235 reference voltage. (See to the block diagram in the front of the datasheet.) This trip level remains "5% below normal" regardless of the programmed output voltage of the 4951C. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 36 below gives a timing diagram depicting the \overline{ERROR} signal and the regulated output voltage as the LP4951C input is ramped up and down. The \overline{ERROR} signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which $V_{OUT} = 4.75V$). Since the LP4951C's dropout voltage is load-dependent (see curve in typical performance characteristics), the **input** voltage trip point (about 5V) will vary with the load current. The **output** voltage trip point (approx. 4.75V) does not vary with load.



The error comparator has an open-collector output which requires an external pullup resistor. This resistor may be returned to the output or some other supply voltage depending on system requirements. In determining a value for this resistor, note that while the output is rated to sink $400\mu A$, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to $1~M\Omega$. The resistor is not required if this output is unused.



*When $V_{IN} \le 1.3V$, the error flag pin becomes a high impedance, and the error flag voltage rises to its pull-up voltage. Using V_{OUT} as the pull-up voltage (see Figure 37), rather than an external 5V source, will keep the error flag voltage under 1.2V (typ.) in this condition. The user may wish to divide down the error flag voltage using equal-value resistors (10 k Ω suggested), to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.

Figure 36. ERROR Output Timing

PROGRAMMING THE OUTPUT VOLTAGE (LP4951C)

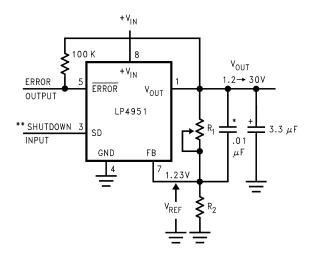
The LP4951C may be pin-strapped for 5V using its internal voltage divider by tying the pin 1 (output) to pin 2 (sense) pins together, and also tying the pin 7 (feedback) and pin 6 (V_{TAP}) pins together. Alternatively, it may be programmed for any output voltage between its 1.235V reference and its 30V maximum rating. As seen in Figure 37, an external pair of resistors is required.

The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2} \right) + I_{FB}R_1 \tag{1}$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the feedback pin bias current, nominally -20 nA. The minimum recommended load current of 1µA forces an upper limit of 1.2 M Ω on the value of R_2 , if the regulator must work with no load (a condition often found in CMOS in standby). I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1 . For better accuracy, choosing R_2 = 100k reduces this error to 0.17% while increasing the resistor program current to 12µA. Since the LP4951C typically draws 60µA at no load with Pin 2 open-circuited, this is a small price to pay.





*See Application Hints

$$V_{out} = V_{Ref} \left(1 + \frac{R_1}{R_2} \right)$$

**Drive with TTL-high to shut down. Ground or leave open if shutdown feature is not to be used.

Note: Pins 2 and 6 are left open.

Figure 37. Adjustable Regulator (LP4951C)

REDUCING OUTPUT NOISE

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only way noise can be reduced on the 3 lead LP4950C but is relatively inefficient, as increasing the capacitor from $1\mu F$ to $220\mu F$ only decreases the noise from $430\mu V$ to $160\mu V$ rms for a 100kHz bandwidth at 5V output.

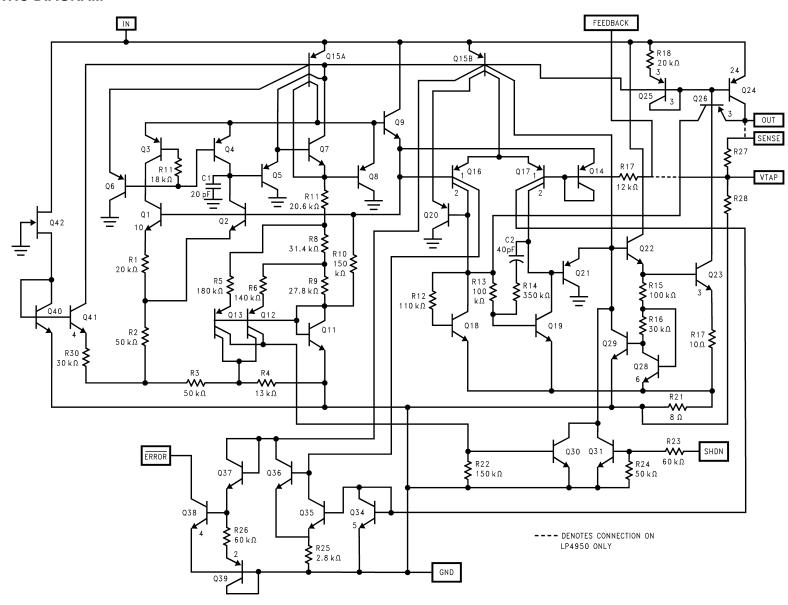
Noise can be reduced fourfold by a bypass capacitor across R₁, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{\text{BYPASS}} \cong \frac{1}{2\pi R_1 \cdot 200 \text{ Hz}} \tag{2}$$

or about $0.01\mu F$. When doing this, the output capacitor must be increased to $3.3\mu F$ to maintain stability. These changes reduce the output noise from $430\mu V$ to $100\mu V$ rms for a 100kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.



SCHEMATIC DIAGRAM







REVISION HISTORY

CI	Changes from Revision B (April 2013) to Revision C							
•	Changed layout of National Data Sheet to TI format		14					

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PACKAGE OPTION ADDENDUM

7-Oct-2013

PACKAGING INFORMATION

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Orderable Device	Status	Package Type	_	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)		(3)		(4/5)	
LP4951CM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS	CU SN	Level-1-260C-UNLIM	-40 to 125	LP495	Samples
						& no Sb/Br)				1CM	barripies
LP4951CMX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	LP495	Samples
										1CM	Dantiples
LP4951CMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS	CU SN	Level-1-260C-UNLIM	-40 to 125	LP495	Camples.
						& no Sb/Br)				1CM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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PACKAGE OPTION ADDENDUM

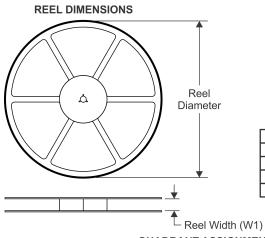
7-Oct-2013

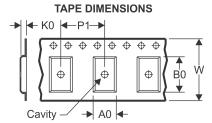
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

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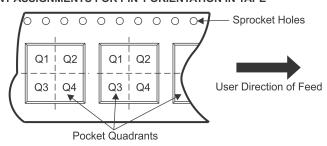
TAPE AND REEL INFORMATION





Α0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

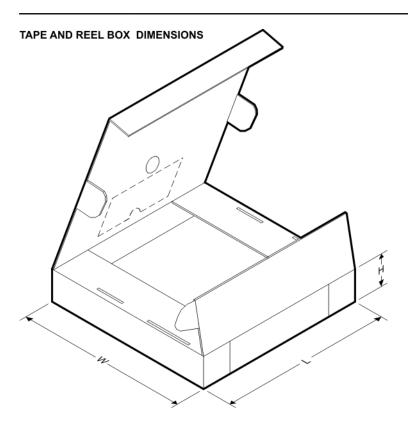
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP4951CMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP4951CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP4951CMX	SOIC	D	8	2500	367.0	367.0	35.0
LP4951CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



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