



# BT137X-600E

4Q Triac

9 October 2013

Product data sheet

## 1. General description

Planar passivated sensitive gate four quadrant triac in a SOT186A "full pack" plastic package intended for use in general purpose bidirectional switching and phase control applications. This sensitive gate "series E" triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

## 2. Features and benefits

- Direct triggering from low power drivers and logic ICs
- High blocking voltage capability
- Isolated package
- Low holding current for small load currents and lowest EMI at commutation
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate
- Triggering in all four quadrants

## 3. Applications

- General purpose motor control
- General purpose switching

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage			-	-	600	V
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25^\circ\text{C}$ ; $t_p = 20 \text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>		-	-	65	A
$I_{T(\text{RMS})}$	RMS on-state current	full sine wave; $T_h \leq 73^\circ\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>		-	-	8	A
Static characteristics							
$I_{GT}$	gate trigger current	$V_D = 12 \text{ V}$ ; $I_T = 0.1 \text{ A}$ ; T2+ G+; $T_j = 25^\circ\text{C}$ ; <a href="#">Fig. 7</a>		-	2.5	10	mA
		$V_D = 12 \text{ V}$ ; $I_T = 0.1 \text{ A}$ ; T2+ G-; $T_j = 25^\circ\text{C}$ ; <a href="#">Fig. 7</a>		-	4	10	mA



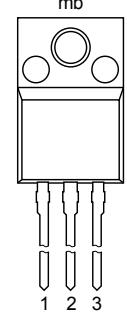
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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		$V_D = 12 \text{ V}$ ; $I_T = 0.1 \text{ A}$ ; T2- G-; $T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>		-	5	10	mA
		$V_D = 12 \text{ V}$ ; $I_T = 0.1 \text{ A}$ ; T2- G+; $T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>		-	11	20	mA
$I_H$	holding current	$V_D = 12 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>		-	2.5	20	mA

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated	 <b>TO-220F (SOT186A)</b>	 <b>sym051</b>

## 6. Ordering information

Table 3. Ordering information

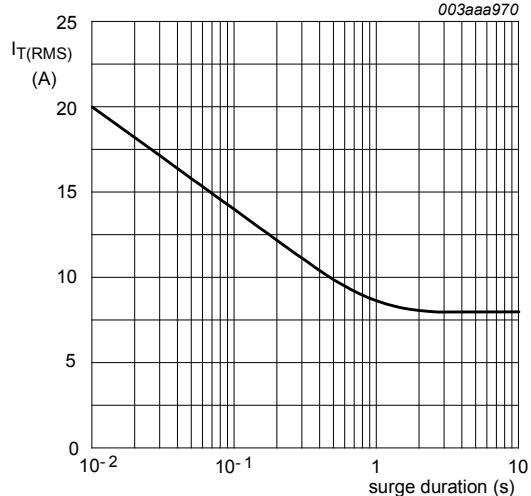
Type number	Package		
	Name	Description	Version
BT137X-600E	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage			-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 73$ °C; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>		-	8	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>		-	65	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		-	71	A
$I^2t$	$I^2t$ for fusing	$t_p = 10$ ms; SIN		-	21	$A^2s$
$dI_T/dt$	rate of rise of on-state current	$I_T = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/ $\mu$ s; T2+ G+		-	50	$A/\mu$ s
		$I_T = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/ $\mu$ s; T2+ G-		-	50	$A/\mu$ s
		$I_T = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/ $\mu$ s; T2- G-		-	50	$A/\mu$ s
		$I_T = 12$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/ $\mu$ s; T2- G+		-	10	$A/\mu$ s
$I_{GM}$	peak gate current			-	2	A
$P_{GM}$	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
$T_{stg}$	storage temperature			-40	150	°C
$T_j$	junction temperature			-	125	°C



$f = 50$  Hz;  $T_h = 73$  °C

Fig. 1. RMS on-state current as a function of surge duration; maximum values

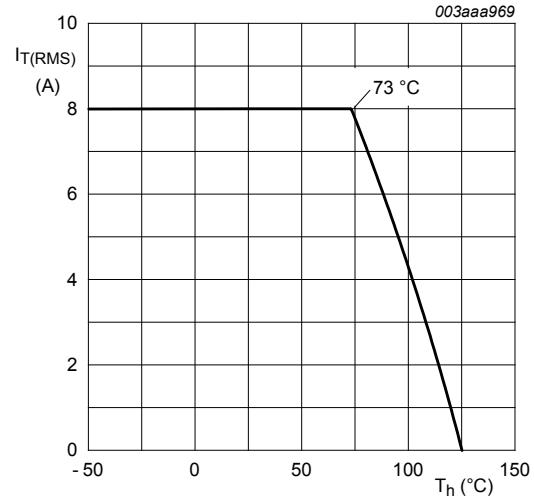
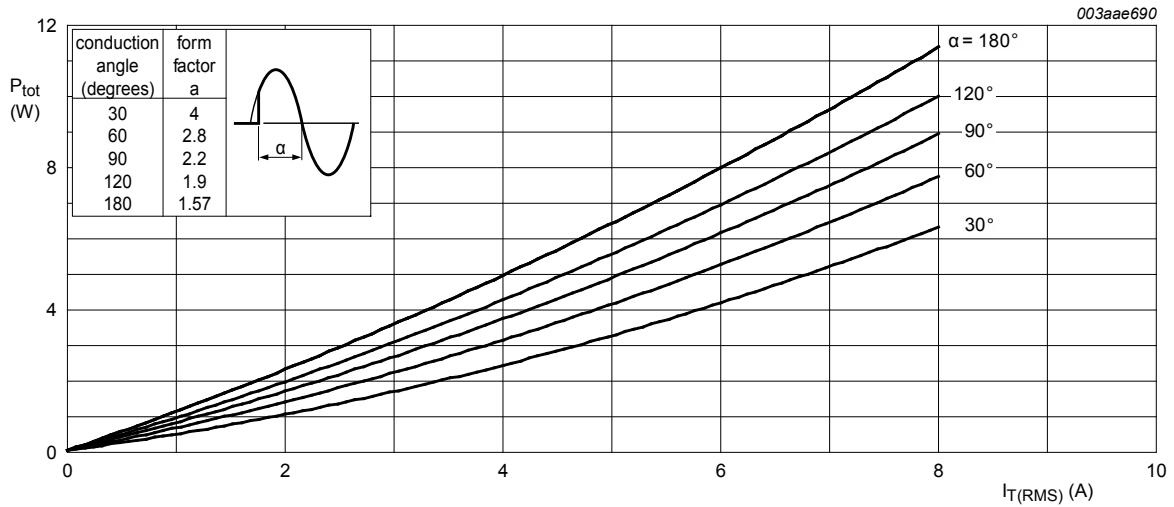


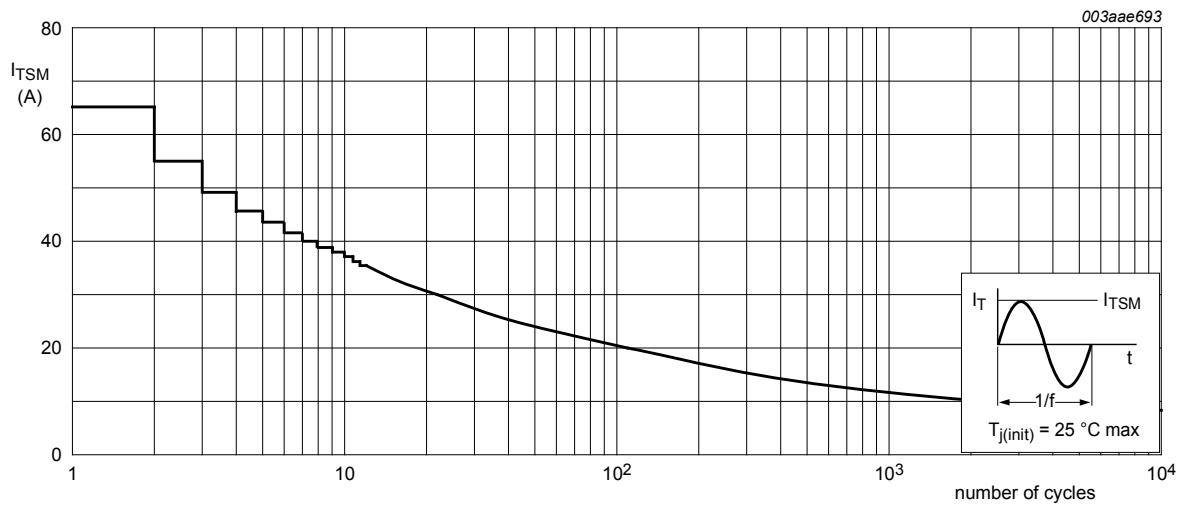
Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values



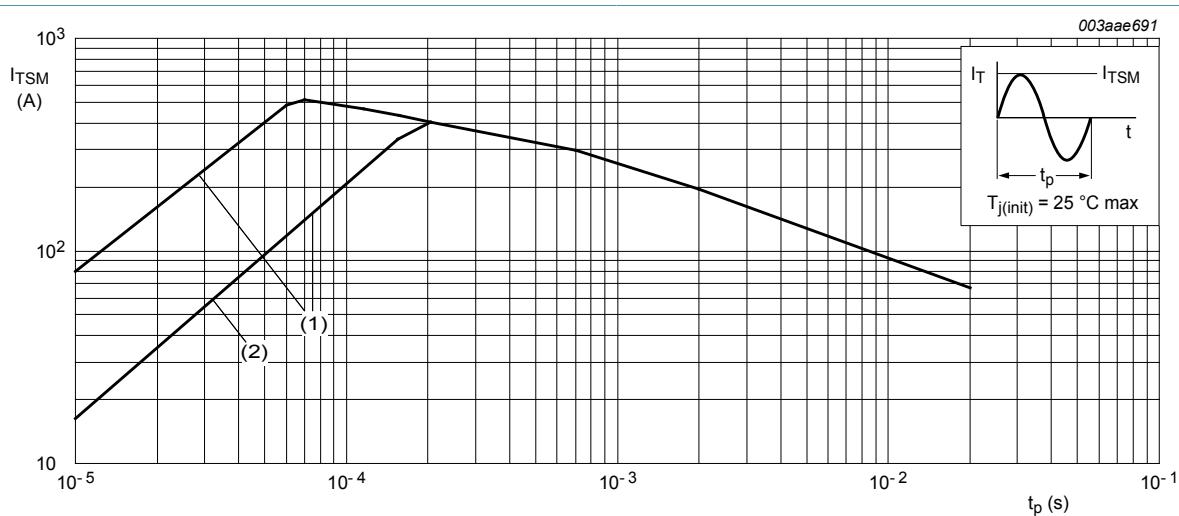
$\alpha$  = conduction angle

$a$  = form factor =  $I_{T(RMS)}/I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



**Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**

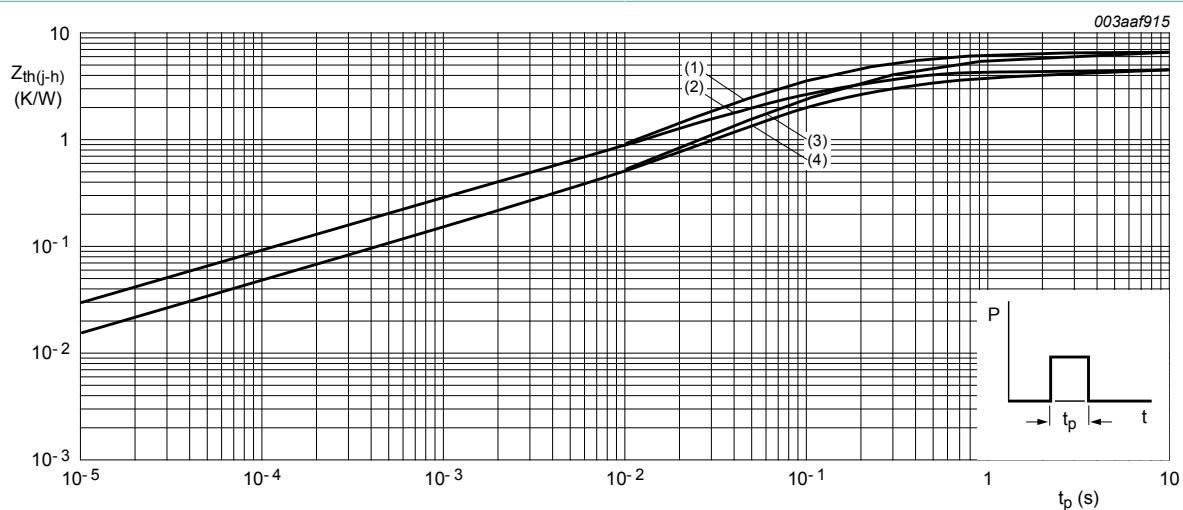


**Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values**

## 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full or half cycle; without heatsink compound; <a href="#">Fig. 6</a>	-	-	6.5	K/W
		full or half cycle; with heatsink compound; <a href="#">Fig. 6</a>	-	-	4.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	55	-	K/W



- (1) Unidirectional (half cycle) without heatsink compound
- (2) Unidirectional (half cycle) with heatsink compound
- (3) Bidirectional (full cycle) without heatsink compound
- (4) Bidirectional (full cycle) with heatsink compound

Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse duration

## 9. Isolation characteristics

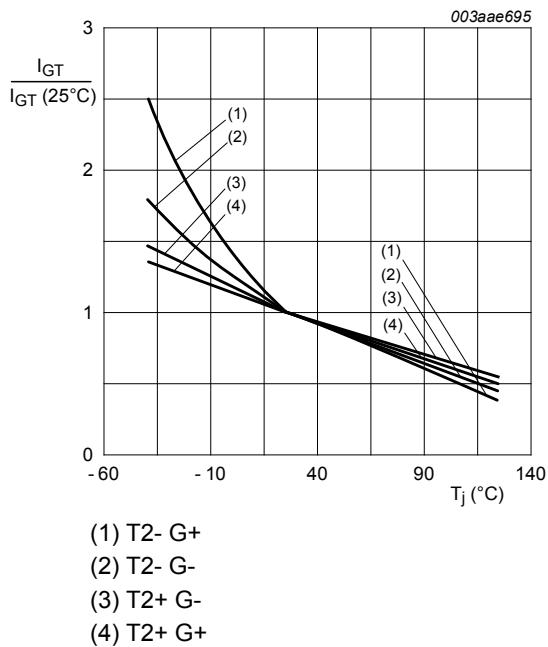
Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free ; $50 \text{ Hz} \leq f \leq 60 \text{ Hz}$ ; $\text{RH} \leq 65 \%$ ; $T_h = 25^\circ\text{C}$	-	-	2500	V
$C_{isol}$	isolation capacitance	from main terminal 2 to external heatsink ; $f = 1 \text{ MHz}$ ; $T_h = 25^\circ\text{C}$	-	10	-	pF

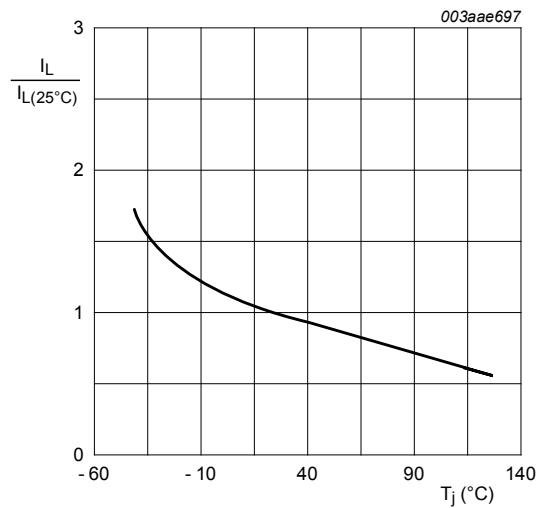
## 10. Characteristics

Table 7. Characteristics

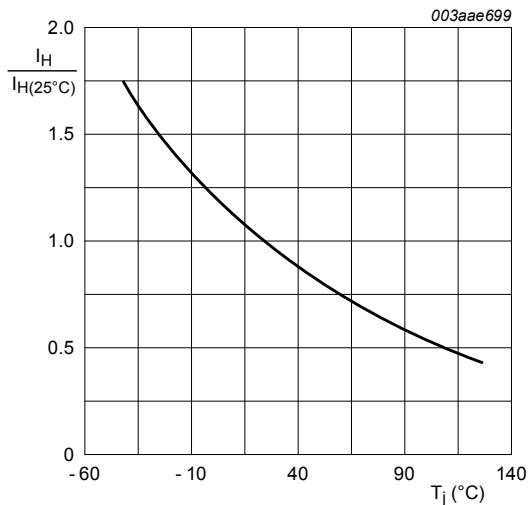
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Static characteristics</b>							
I <sub>GT</sub>	gate trigger current	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2+ G+; T <sub>j</sub> = 25 °C; <a href="#">Fig. 7</a>		-	2.5	10	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2+ G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 7</a>		-	4	10	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2- G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 7</a>		-	5	10	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2- G+; T <sub>j</sub> = 25 °C; <a href="#">Fig. 7</a>		-	11	20	mA
I <sub>L</sub>	latching current	V <sub>D</sub> = 12 V; I <sub>G</sub> = 0.1 A; T2+ G+; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>		-	3	25	mA
		V <sub>D</sub> = 12 V; I <sub>G</sub> = 0.1 A; T2+ G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>		-	14	35	mA
		V <sub>D</sub> = 12 V; I <sub>G</sub> = 0.1 A; T2- G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>		-	3	25	mA
		V <sub>D</sub> = 12 V; I <sub>G</sub> = 0.1 A; T2- G+; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>		-	4	35	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 9</a>		-	2.5	20	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 10 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>		-	1.3	1.65	V
V <sub>GT</sub>	gate trigger voltage	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>		-	0.7	1	V
		V <sub>D</sub> = 400 V; I <sub>T</sub> = 0.1 A; T <sub>j</sub> = 125 °C; <a href="#">Fig. 11</a>		0.25	0.4	-	V
I <sub>D</sub>	off-state current	V <sub>D</sub> = 600 V; T <sub>j</sub> = 125 °C		-	0.1	0.5	mA
<b>Dynamic characteristics</b>							
dV <sub>D</sub> /dt	rate of rise of off-state voltage	V <sub>DM</sub> = 402 V; T <sub>j</sub> = 125 °C; (V <sub>DM</sub> = 67% of V <sub>DRM</sub> ); exponential waveform; gate open circuit		-	50	-	V/μs
t <sub>gt</sub>	gate-controlled turn-on time	I <sub>TM</sub> = 12 A; V <sub>D</sub> = 600 V; I <sub>G</sub> = 0.1 A; dI <sub>G</sub> /dt = 5 A/μs		-	2	-	μs



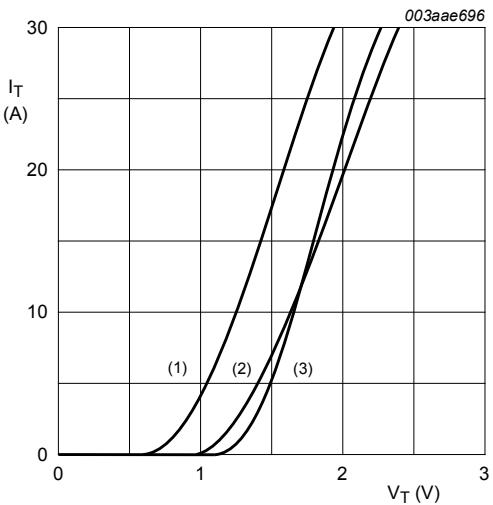
**Fig. 7. Normalized gate trigger current as a function of junction temperature**



**Fig. 8. Normalized latching current as a function of junction temperature**



**Fig. 9. Normalized holding current as a function of junction temperature**



**Fig. 10. On-state current as a function of on-state voltage**

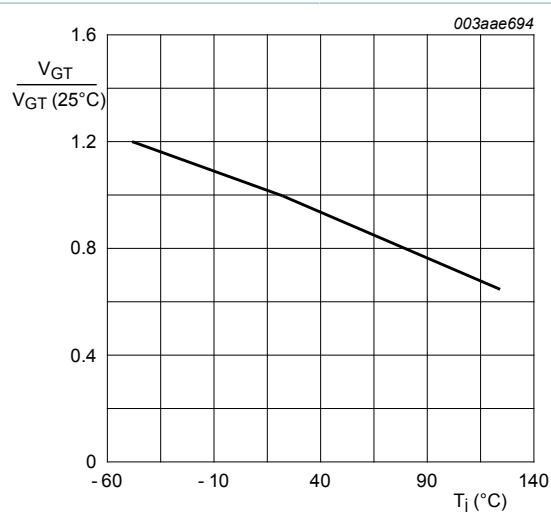
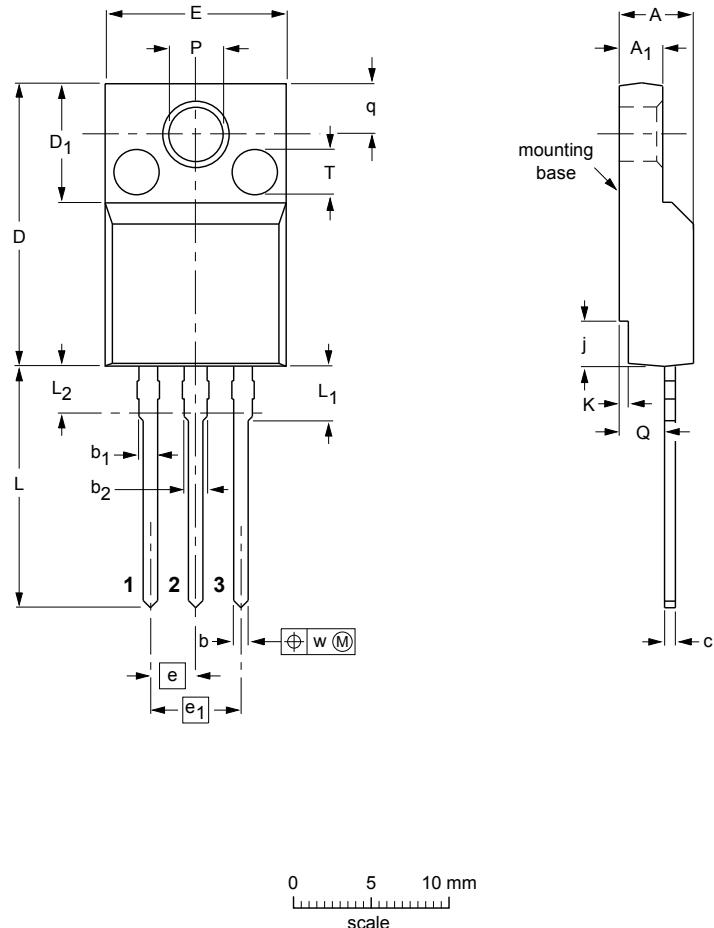


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

## 11. Package outline

Plastic single-ended package; isolated heatsink mounted;  
1 mounting hole; 3-lead TO-220 'full pack'

SOT186A



### DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	b <sub>2</sub>	c	D	D <sub>1</sub>	E	e	e <sub>1</sub>	j	K	L	L <sub>1</sub>	L <sub>2</sub> <sup>(1)</sup> max.	P	Q	q	T <sup>(2)</sup>	w
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3	2.54	5.08	2.7	0.6	14.4	3.30	3	3.2	2.6	3.0	2.5	0.4
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7	2.54	5.08	1.7	0.4	13.5	2.79	3.0	3.0	2.3	2.6	2.5	0.4

### Notes

1. Terminal dimensions within this zone are uncontrolled.
2. Both recesses are # 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3-lead TO-220F				-02-04-09-06-02-14

Fig. 12. Package outline TO-220F (SOT186A)

## 12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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