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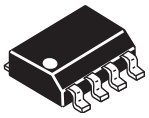
RoHS

Local Interconnect Network (LIN) Enhanced Physical Interface with Selectable Slew-Rate

33661

LIN PHYSICAL INTERFACE



EF SUFFIX (PB-FREE)
98ASB42564B
8-PIN SOICN

Local interconnect network (LIN) is a serial communication protocol designed to support automotive networks in conjunction with controller area network (CAN). As the lowest level of a hierarchical network, LIN enables cost-effective communication with sensors and actuators when all the features of CAN are not required. This device is powered by SMARTMOS technology.

The 33661 is a physical layer component dedicated to automotive LIN sub-bus applications. It offers slew-rate selection for optimized operation at 10 kbps and 20 kbps, fast baud rate (above 100 kbps) for test and programming modes, excellent radiated emission performance, and safe behavior in the event of LIN bus short-to-ground or LIN bus leakage during low power mode.

The 33661 is compatible with LIN Protocol Specification 2.0.

ORDERING INFORMATION		
Device (For Tape and Reel, add an R2 Suffix)	**Temperature Range (T_A)**	**Package**
MC33661PEF	-40 to 125°C	8 SOICN

Features

- Operational from V_{SUP} 6.0 V to 18 V DC, functional up to 27 V DC, and handles 40 V during load dump
- Active bus waveshaping offering excellent radiated emission performance
- 5.0 kV ESD on LIN bus pin
- 30 kΩ internal pull-up resistor
- LIN bus short-to-ground or high leakage in Sleep mode
- -18 V to +40 V DC voltage at LIN pin
- 8.0 μA in Sleep mode
- Local and remote wake-up capability reported by INH and RXD pins
- 5.0 V and 3.3 V compatible digital inputs without any external components required

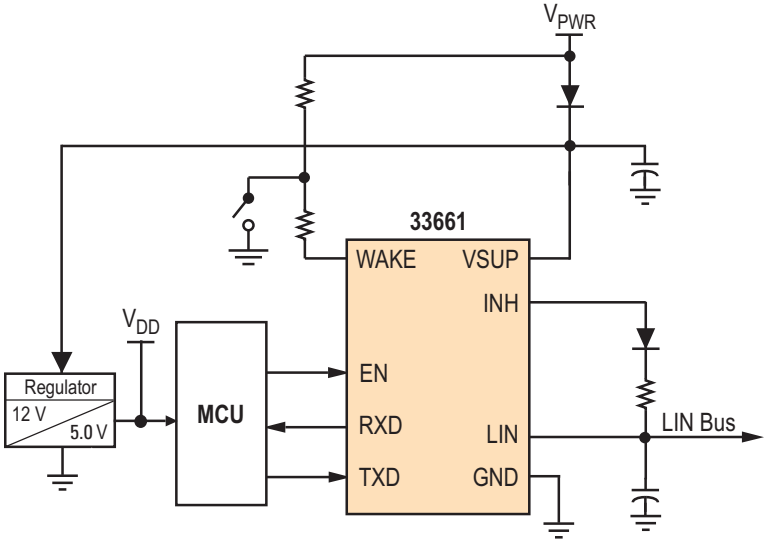


Figure 1. 33661 Simplified Application Diagram

INTERNAL BLOCK DIAGRAM

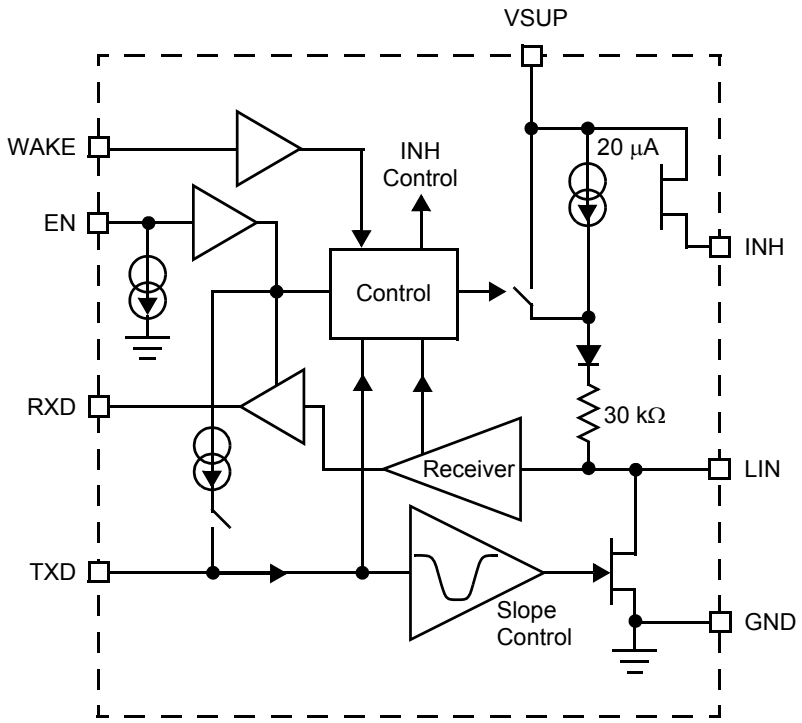


Figure 2. 33661 Simplified Internal Block Diagram

PIN CONNECTIONS

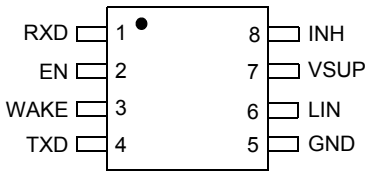


Figure 3. 33661 8-SOICN Pin Connections

Table 1. 33661 8-SOICN Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page page 12.

Pin	Pin Name	Formal Name	Definition
1	RXD	Data Output	MCU interface that reports the state of the LIN bus voltage.
2	EN	Enable Control	Controls the operation mode of the interface.
3	WAKE	Wake Input	High-voltage input used to wake-up the device from Sleep mode.
4	TXD	Data Input	MCU interface to control the state of the LIN output.
5	GND	Ground	Device ground pin.
6	LIN	LIN Bus	Bidirectional pin that represents the single-wire bus transmitter and receiver.
7	VSUP	Power Supply	Device power supply pin.
8	INH	Inhibit Output	This pin can have two main functions: controlling an external switchable voltage regulator having an inhibit input or driving a bus external resistor in the master node application.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage	V_{SUP}		V
Continuous Supply Voltage		27	
Transient Voltage (Load Dump)		40	
WAKE DC and Transient Voltage (Through a 33 kΩ Serial Resistor)	V_{WAKE}	-18 to 40	V
Logic Voltage (RXD, TXD, EN Pins)	V_{LOG}	-0.3 to 5.5	V
LIN Bus Voltage	V_{BUS}		V
DC Voltage		-18 to 40	
Transient (Coupled Through 1.0 nF Capacitor)		-150 to 100	
INH Voltage/Current			
DC Voltage	V_{INH}	-0.3 to V_{SUP} + 0.3	V
DC Current	I_{INH}	40	mA
ESD Voltage [1]	V_{ESD1}		V
Human Body Model			
All Pins		±2000	
LIN Pin with Respect to Ground		±5000	
Machine Model	V_{ESD2}	±200	
THERMAL RATINGS			
Operating Temperature			°C
Ambient	T_A	-40 to 125	
Junction	T_J	-40 to 150	
Storage Temperature	T_{STG}	-55 to 150	°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	150	°C/W
Peak Package Reflow Temperature During Reflow [2], [3]	T_{PPRT}	Note 3	°C
Thermal Shutdown Temperature	T_{SHUT}	150 to 200	°C
Thermal Shutdown Hysteresis Temperature	T_{HYST}	8.0 to 20	°C

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 220 pF, R_{ZAP} = 0 Ω).
2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
3. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VSUP PIN (DEVICE POWER SUPPLY)					
Supply Voltage	V_{SUP}				V
Nominal DC		7.0	13.5	18.0	
Functional DC, $T_A \geq 25$ °C		6.0	—	—	
Supply Current in Sleep Mode					µA
$V_{SUP} \leq 13.5$ V, Recessive State	I_{S1}	—	8.0	12	
13.5 V < V_{SUP} < 1.0 V	I_{S2}	—	—	200	
$V_{SUP} \leq 13.5$ V, Dominant State or Shorted to GND	I_{S3}	—	300	—	
Supply Current in Normal, Slow, or Fast Mode					MA
Bus Recessive, Excluding INH Output Current	$I_{S(REC)}$	—	4.0	6.0	
Bus Dominant, Total Bus Load >500 Ω, Excluding INH Output Current	$I_{S(DOM)}$	—	6.0	8.0	
RXD OUTPUT PIN (LOGIC)					
Low Level Output Voltage	V_{OL}				V
$I_{IN} \leq 1.5$ mA		0.0	—	0.9	
High Level Output Voltage	V_{OH}				V
V_{EN} = 5.0 V, $I_{OUT} \leq 250$ µA		4.25	—	5.25	
V_{EN} = 3.3 V, $I_{OUT} \leq 250$ µA		3.0	—	3.5	
TXD INPUT PIN (LOGIC)					
Low Level Input Voltage	V_{IL}	—	—	1.2	V
High Level Input Voltage	V_{IH}	2.5	—	—	V
Input Threshold Voltage Hysteresis	V_{INHYST}	100	300	800	mV
Pull-up Current Source	I_{PU}				µA
V_{EN} = 5.0 V, 1.0 V < V_{TXD} < 3.5 V		-60	-35	-20	
EN INPUT PIN (LOGIC)					
Low Level Input Voltage	V_{IL}	—	—	1.2	V
High Level Input Voltage	V_{IH}	2.5	—	—	V
Input Voltage Threshold Hysteresis	V_{INHYST}	100	300	800	mV
Low Level Input Current	I_{IL}				µA
V_{IN} = 1.0 V		5.0	20	30	
High Level Input Current	I_{IH}				µA
V_{IN} = 4.0 V		—	20	40	

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PIN (VOLTAGE EXPRESSED VERSUS V_{SUP} VOLTAGE)					
Low Level Bus Voltage (Dominant State) External Bus Pull-up 500 Ω	V_{DOM}	— 	— 	1.4 	V
High Level Bus Voltage (Recessive State) TXD HIGH, I_{OUT} = 1.0 μA	V_{REC}	V_{SUP} - 1.0 	— 	— 	V
Internal Pull-up Resistor to VSUP (Normal mode)	R_{PU}	20	30	47	kΩ
Internal Pull-up Current Source (Sleep mode)	I_{PU}	—	20	—	μA
Overcurrent Shutdown Threshold	I_{OV-CUR}	50	75	150	mA
Leakage Current to GND Recessive State, 8.0 V ≤ V_{SUP} ≤ 18 V, 8.0 V ≤ V_{LIN} ≤ 18 V GND Disconnected, V_{GND} = V_{SUP}, V_{LIN} at -18 V VSUP Disconnected, V_{LIN} at +18 V	I_{LEAK}	 0 -1.0 —	 3.0 — 1.0	 20 1.0 10	 μA mA μA
LIN Receiver, Low Level Input Voltage TXD HIGH, RXD LOW	V_{LINL}	0.0 V_{SUP}	—	0.4 V_{SUP}	V
LIN Receiver, High Level Input Voltage TXD HIGH, RXD HIGH	V_{LINH}	0.6 V_{SUP}	—	V_{SUP}	V
LIN Receiver Threshold Center (V_{LINH} - V_{LINL}) / 2	V_{LINTH}	0.475 V_{SUP}	0.5 V_{SUP}	0.525 V_{SUP}	V
LIN Receiver Input Voltage Hysteresis V_{LINH} - V_{LINL}	$V_{LINHYST}$	—	—	0.175 V_{SUP}	V
LIN Wake-up Threshold Voltage	V_{LINWU}	—	0.5 V_{SUP}	—	V
INH OUTPUT PIN					
Driver ON Resistance (Normal mode)	INH_{ON}	—	35	70	Ω
Leakage Current (Sleep mode) 0.0 V < V_{INH} < V_{SUP}	I_{LEAK}	0	—	5.0	μA
WAKE INPUT PIN					
Typical Wake-up Threshold Voltage (EN = 0 V, 7.0 V ≤ V_{SUP} ≤ 18 V) (5) HIGH-to-LOW Transition LOW-to-HIGH Transition	V_{WUTH}	 0.3 V_{SUP} 0.4 V_{SUP}	 0.43 V_{SUP} 0.55 V_{SUP}	 0.55 V_{SUP} 0.65 V_{SUP}	V
Wake-up Threshold Voltage Hysteresis	V_{WUHYST}	0.1 V_{SUP}	0.16 V_{SUP}	0.2 V_{SUP}	V
WAKE Input Current V_{WAKE} < 27 V	I_{WU}	—	1.0	5.0	μA

Notes

4. This parameter is guaranteed by design; however, it is not production tested.
5. When V_{SUP} > 18 V, the wake-up voltage thresholds remain identical to the wake-up thresholds at 18 V.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN OUTPUT TIMING CHARACTERISTICS FOR NORMAL MODE					
Dominant Propagation Delay Time TXD to LIN (6)					µs
Measurement Threshold (50% TXD to 58.1% V_{SUP})	t_{DOM}(MIN)	—	—	50	
Measurement Threshold (50% TXD to 28.4% V_{SUP})	t_{DOM}(MAX)	—	—	50	
Recessive Propagation Delay Time TXD to LIN (6)					µs
Measurement Threshold (50% TXD to 42.2% V_{SUP})	t_{REC}(MIN)	—	—	50	
Measurement Threshold (50% TXD to 74.4% V_{SUP})	t_{REC}(MAX)	—	—	50	
Propagation Delay Time Symmetry					µs
t_{DOM}(MIN) to t_{REC}(MAX)	dt_1	-10.44	—	8.12	
t_{DOM}(MAX) to t_{REC}(MIN)	dt_2	-10.44	—	8.12	
LIN OUTPUT TIMING CHARACTERISTICS FOR SLOW MODE					
Dominant Propagation Delay Time TXD to LIN (6)					µs
Measurement Threshold (50% TXD to 61.6% V_{SUP})	t_{DOM}(MIN)	—	—	100	
Measurement Threshold (50% TXD to 25.1% V_{SUP})	t_{DOM}(MAX)	—	—	100	
Recessive Propagation Delay Time TXD to LIN (6)					µs
Measurement Threshold (50% TXD to 38.9% V_{SUP})	t_{REC}(MIN)	—	—	100	
Measurement Threshold (50% TXD to 77.8% V_{SUP})	t_{REC}(MAX)	—	—	100	
Propagation Delay Time Symmetry					µs
t_{DOM}(MIN) to t_{REC}(MAX)	dt_{1S}	-21.88	—	17.44	
t_{DOM}(MAX) to t_{REC}(MIN)	dt_{2S}	-21.88	—	17.44	
LIN OUTPUT DRIVER FAST MODE					
LIN Fast Slew Rate (Programming Mode)	dv/dt fast				V/µs
Fast Slew Rate		—	15	—	
LIN PIN					
Over-current Shutdown Delay Time (7)	$t_{OV-DELAY}$	—	10	—	µs
LIN RECEIVER CHARACTERISTICS					
Receiver Dominant Propagation Delay Time (8)	t_{RL}				µs
LIN LOW to RXD LOW		—	3.5	6.0	
Receiver Recessive Propagation Delay Time (8)	t_{RH}				µs
LIN HIGH to RXD HIGH		—	3.5	6.0	
Receiver Propagation Delay Time Symmetry	t_{R-SYM}				µs
t_{RL} - t_{RH}		-2.0	—	2.0	

Notes

6. 7.0 V ≤ V_{SUP} ≤ 18 V. Bus load R_0 and C_0: 1.0 nF/1.0 kΩ, 6.8 nF/660 Ω, 10 nF/500 Ω.
7. This parameter is guaranteed by design; however, it is not production tested.
8. Measured between LIN signal threshold V_{LINL} or V_{LINH} and 50% of RXD signal.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SLEEP MODE AND WAKE-UP TIMINGS					
EN Pin Wake-up Time [9]	t_{LWUE}	—	5.0	15	µs
WAKE Pin Filter Time [10]	t_{WF}	10	—	70	µs
LIN Pin Wake-up Filter Time (LIN Bus Wake-Up) [11]	t_{WUF}	40	70	120	µs
Sleep Mode Delay Time [12] EN HIGH-to-LOW	t_{SD}	50	—	—	µs
Delay for INH Turning off When Device Enters in Sleep Mode [16], [17] EN HIGH-to-LOW and INH HIGH-to-LOW	t_{SD_INH}	—	—	50	µs
Delay Time Between EN and TXD for Mode Selection [13], [14]	t_{D_MS}	5.0	—	—	µs
Delay Time Between First TXD after Device Mode Selection [13], [14]	t_{D_COM}	50	—	—	µs
FAST BAUD RATE TIMING					
Delay Entering Fast Baud Rate Using Toggle Function [15] EN LOW to EN HIGH	t_1	—	—	35	µs
Delay on EN Pin Resetting Fast Baud Rate to Previous Baud Rate [15] EN LOW to EN HIGH	t_2	—	—	5.0	µs

Notes
9. See Figures 7 and 8, 10.
10. See Figures 9 and 10, 10.
11. See Figures 11 and 12, 11.
12. See Figure 14a, 11.
13. See Figures 7 through 12, pp. 10–11.
14. This parameter is guaranteed by design; however, it is not production tested.
15. See Figure 13, 11.
16. No capacitor is connected to the INH pin. Measurement is done between the EN HIGH-to-LOW transition at 80% of INH voltage.
17. See Figure 14b, 11.

TIMING DIAGRAMS

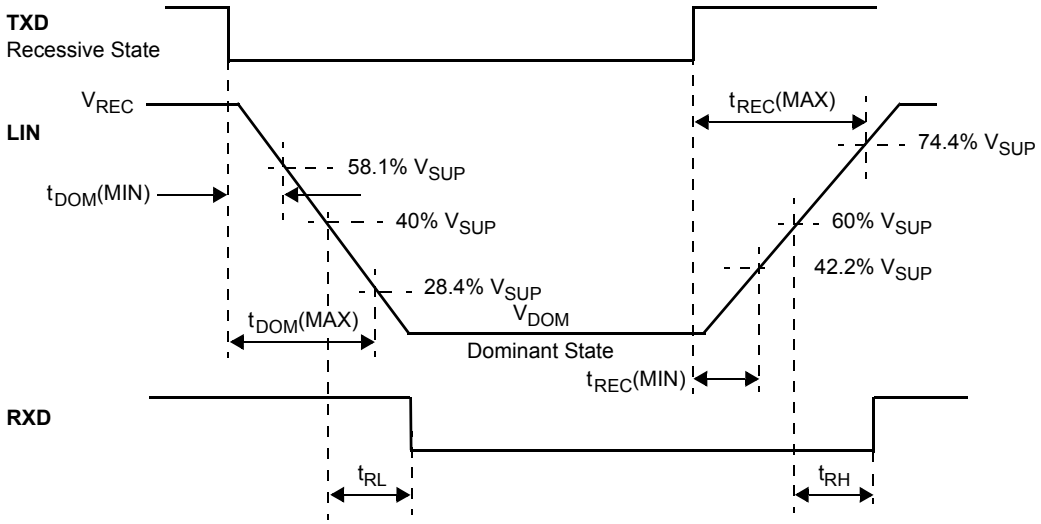


Figure 4. Normal Mode Bus Timing Characteristics

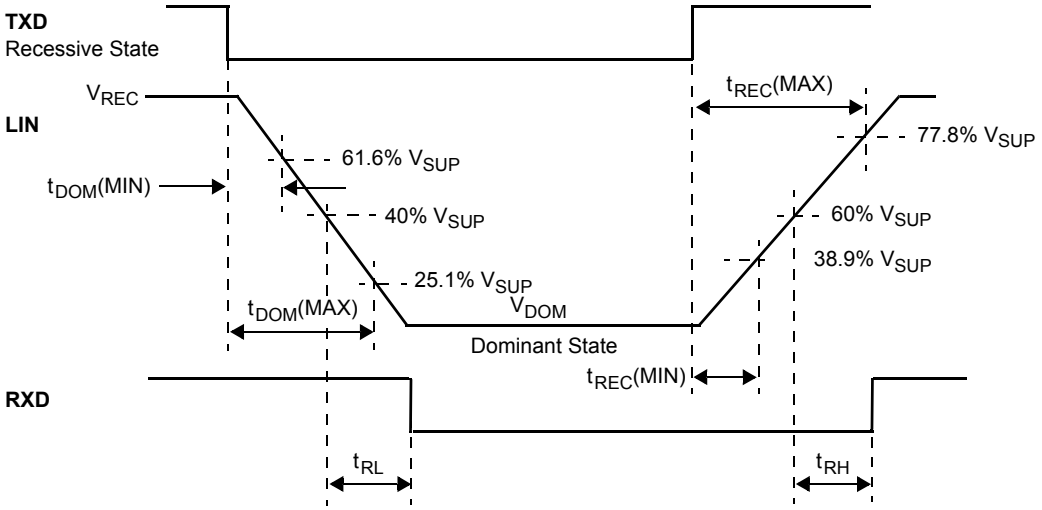
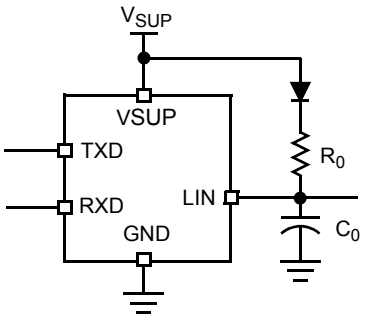


Figure 5. Slow Mode Bus Timing Characteristics



Note R_0 and C_0: 1.0 kΩ/1.0 nF, 660 Ω/6.8 nF, and 500 Ω/10 nF.

Figure 6. Test Circuit for Timing Measurements

FUNCTIONAL DIAGRAMS

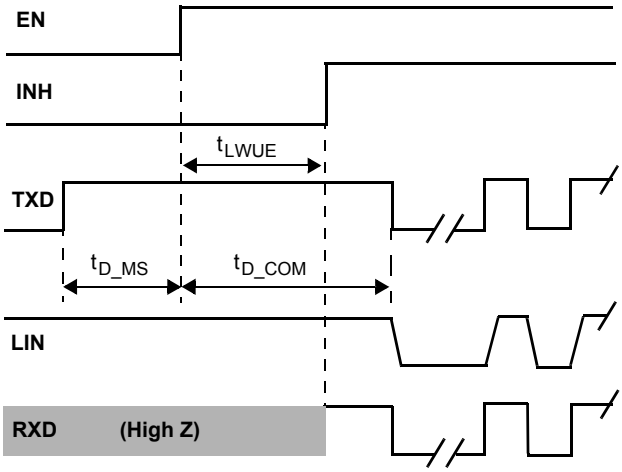


Figure 7. EN Pin Wake-up and Normal Baud Rate Selection (1.0 kbps to 20 kbps)

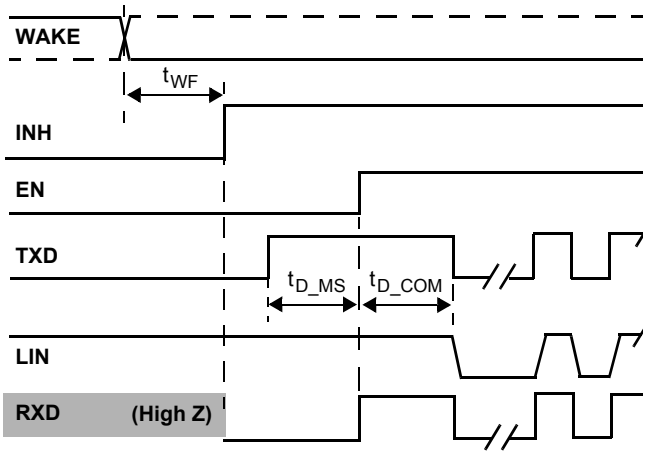


Figure 9. WAKE Pin Wake-up and Normal Baud Rate Selection (1.0 kbps to 20 kbps)

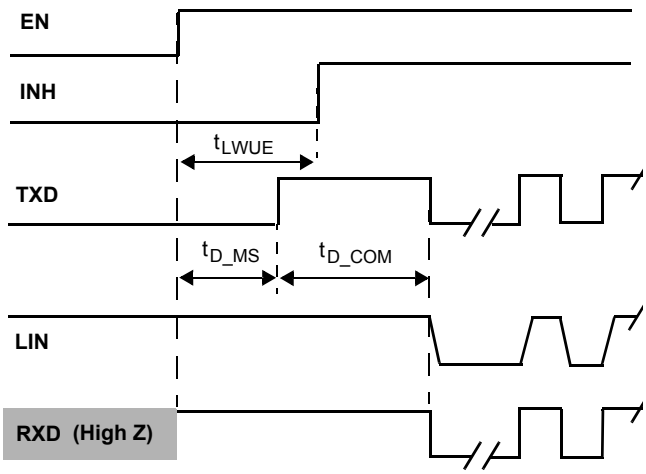


Figure 8. EN Pin Wake-up and Slow Baud Rate Selection (1.0 kbps to 10 kbps)

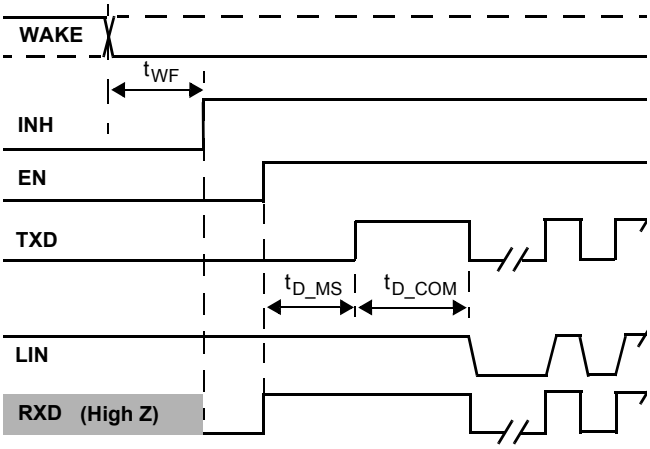


Figure 10. WAKE Pin Wake-up and Slow Baud Rate Selection (1.0 kbps to 10 kbps)

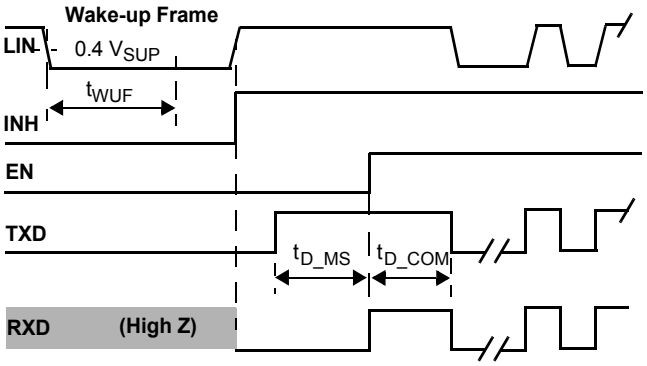


Figure 11. LIN Bus Wake-up and Normal Baud Rate Selection (1.0 kbps to 20 kbps)

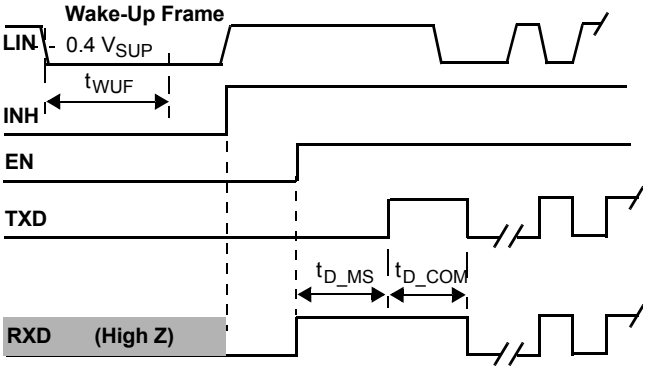


Figure 12. LIN Bus Wake-up and Slow Baud Rate Selection (1.0 kbps to 10 kbps)

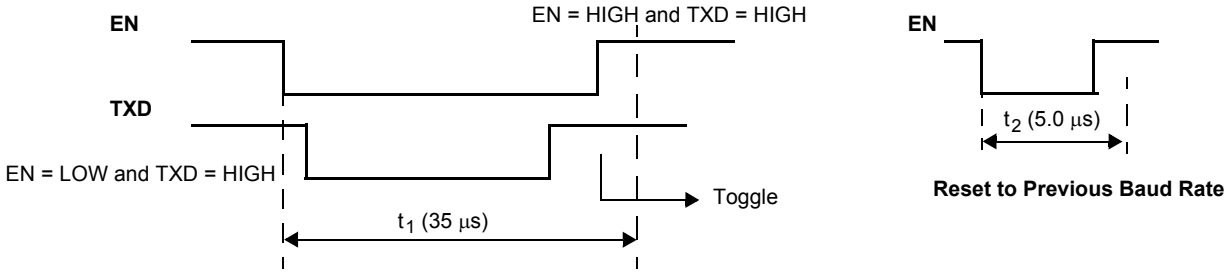


Figure 13. Fast Baud Rate Selection (Toggle Function)

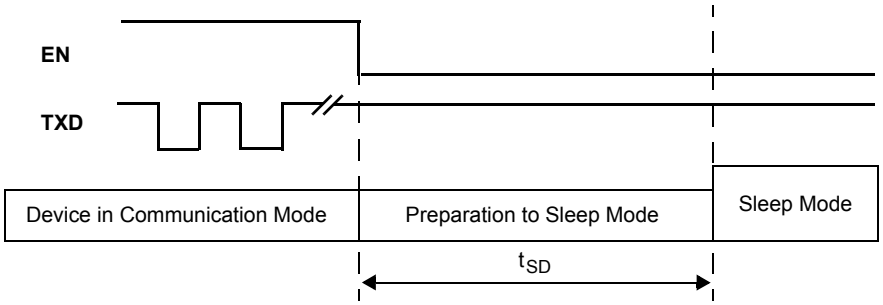


Figure 14a

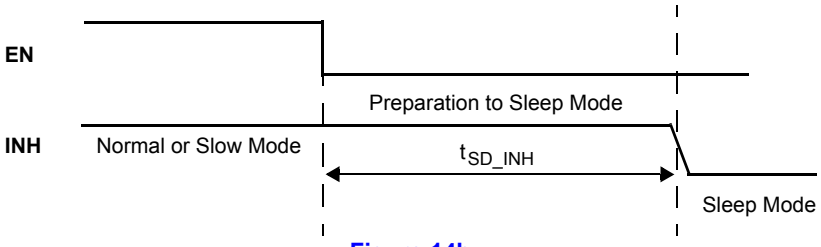


Figure 14b

Figure 14. Sleep Mode Enter

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33661 is a Physical Layer component dedicated to automotive LIN sub-bus applications.

The 33661 features include slew rate selection for optimized operation at 10 kbps and 20 kbps, fast baud rate for test and programming modes, excellent radiated emission performance, and safe behavior in case of LIN bus short-to-ground or LIN bus leakage during low power mode.

Digital inputs are 5.0 V and 3.3 V compatible without any external component required.

The INH output may be used to control an external voltage regulator or to drive a LIN bus pull-up resistor.

FUNCTIONAL PIN DESCRIPTION

POWER SUPPLY PIN (VSUP)

The VSUP supply pin is the power supply pin for the 33661. The pin is connected to a battery through a serial diode for reverse battery protection. The DC operating voltage is from 7.0 V to 27 V. This pin sustains standard automotive voltage conditions such as 27 V DC during jump-start conditions and 40 V during load dump. Supply current in the Sleep mode is typically 8.0 μA.

GROUND PIN (GND)

In case of a ground disconnection at the module level, the 33661 does not have significant current consumption on the LIN bus pin when in the recessive state. (Less than 100 μA is sourced from LIN bus pin, which creates 100 mV drop voltage from the 1.0 kΩ LIN bus pull-up resistor.)

LIN BUS PIN (LIN)

This I/O pin represents the single-wire bus transmitter and receiver.

Transmitter Characteristics

The LIN driver is a low-side MOSFET with internal overcurrent thermal shutdown. An internal pullup resistor with a serial diode structure is integrated so no external pullup components are required for the application in a slave node. An additional pullup resistor of 1.0 kΩ must be added when the device is used in the master node.

Voltage can go from -18 V to 40 V without current other than the pull-up resistance. The LIN pin exhibits no reverse current from the LIN bus line to VSUP, even in the event of GND shift or V_{PWR} disconnection.

The transmitter has two slew rate selections: 20 kbps (normal slew rate) and 10 kbps (slow slew rate). The slow slew rate can be used to improve radiated emissions.

Receiver Characteristics

The receiver thresholds are ratiometric with the device supply pin.

DATA INPUT PIN (TXD)

The TXD input pin is the MCU interface to control the state of the LIN output. When TXD is LOW, LIN output is LOW; when TXD is HIGH, the LIN output transistor is turned OFF. The threshold is 3.3 V and 5.0 V compatible. The baud rate selection (normal or Slow mode) is done at device wake-up by the state of the TXD pin prior to a HIGH level at the EN pin (see Figures 7 through 12).

DATA OUTPUT PIN (RXD)

The RXD output pin is the MCU interface, which reports the state of the LIN bus voltage. LIN HIGH (recessive) is reported by a high-voltage on RXD; LIN LOW (dominant) is reported by a low-voltage on RXD. The RXD output structure is a CMOS-type push-pull output stage.

The low level is fixed. The high level is dependant on the EN voltage. If EN is set at 3.3 V, RXD V_{OH} is 3.3 V. If EN is set at 5.0 V, RXD V_{OH} is 5.0 V.

In the Sleep mode, RXD is high impedance. When a wake-up event is recognized from WAKE pin or from the LIN bus pin, RXD is pulled LOW to report the wake-up event. An external pull-up resistor may be needed.

ENABLE INPUT PIN (EN)

The EN input pin controls the operation mode of the interface. If EN = 1, the interface is in Normal mode, with transmission path from TXD to LIN and from LIN to RXD both active. The threshold is 3.3 V and 5.0 V compatible. The high level at EN defines the V_{OH} at RXD. The Sleep mode is entered by setting EN LOW while TXD is HIGH. Sleep mode is active after the t_{SD} filter time (see Figure 14).

INHIBIT OUTPUT PIN (INH)

The INH output pin may have two main functions. It may be used to control an external switchable voltage regulator having an inhibit input. The high drive capability also allows it to drive the bus external resistor in the master node application. This is illustrated in Figures 18 and 19.

In Sleep mode, INH is turned OFF. If a voltage regulator inhibit input is connected to INH, the regulator will be disabled. If the master node pull-up resistor is connected to INH, the pull-up resistor will be disabled from the LIN bus.

WAKE INPUT PIN (WAKE)

The WAKE pin is a high-voltage input used to wake-up the device from the Sleep mode. WAKE is usually connected to an external switch in the application. The typical wake thresholds are $V_{SUP}/2$.

The WAKE pin has a special design structure and allows wake-up from both High-to-Low or Low-to-High transitions. When entering into Sleep mode, the LIN monitors the state of the WAKE pin and stores it as a reference state. The opposite state of this reference state will be the wake-up event used by the device to enter again into Normal mode.

An internal filter is implemented (40 μs typical filtering time delay). WAKE pin input structure exhibits a high-impedance, with extremely low input current when voltage at this pin is below 14 V. When voltage at the WAKE pin exceeds 14 V, input current starts to sink into the device. A serial resistor should be inserted in order to limit the input current mainly during transient pulses. Recommended resistor value is 33 kΩ.

Important The WAKE pin should *not* be left open. If the wake-up function is not used, WAKE should be connected to ground to avoid false wake-up.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

As described in the following, and as depicted in Figure 15 and Table 5, the 33661 has two operational modes, Normal and Sleep. Normal mode may be adjusted to improve radiated emissions by changing the slew rate of the LIN bus output to Fast or Slow mode. In addition, there are two transitional modes: Awake mode, which allows the device to go in Normal or Slow mode, and Wait Slow mode, which is a temporary state before the device enters the Slow mode.

NORMAL MODE

In the Normal mode, the 33661 has slew rate and timing compatible with the LIN protocol specification, and operates from 1.0 kbps to 20 kbps. This mode is selected after Sleep mode by setting the TXD pin High prior to setting EN from Low to High. Once Normal mode is selected, it is impossible to select the Slow mode unless the 33661 is set into Sleep mode.

Slow Mode

In the Slow mode, the slew rate is around half the normal slew rate, and bus speed operation ranges from 1.0 kbps to 10 kbps. The radiated emission is significantly reduced compared to the already excellent emission level of the Normal mode. Slow mode is entered after Sleep mode by setting the TXD pin Low prior to setting EN from Low to High. Once the Slow mode is selected, it is impossible to select the Normal mode unless the device is set to Sleep mode.

Fast Mode

In the Fast mode, the slew rate is around 10 times faster than the Normal mode. This allows very fast data transmission (>100 kbps)—for instance, for electronic control unit (ECU) tests and microcontroller program download. The bus pull-up resistor might be reduced to ensure a correct RC time constant in line with the high baud rate used.

Fast mode can be selected from either Normal or Slow mode. Fast mode is entered via a special sequence (called toggle function) as follows: TXD and EN pins set Low, then TXD pulled High, and at the EN pin Low-to-High transition, the device enters into the Fast Baud rate. The duration of this sequence must be less than 35 µs. The toggle function is described in Figure 13. Once in the Fast mode, two different procedures will bring the device back to the previously selected mode (Normal or Slow):

- The toggle function already described.
- A glitch on EN where t_2 < 5.0 µs also resets the device to the previously selected mode (Normal or Slow) (Figure 13).

SLEEP MODE

In the Sleep mode, the transmission path is disabled and the 33661 is in Low Power mode. Supply current from VSUP is very low. Wake-up can occur from LIN bus activity from node internal wake-up through the EN pin and from the WAKE input pin.

In the Sleep mode, the 33661 has an internal 20 µA pull-up source to VSUP. This avoids the high current path from the battery to ground in the event the bus is shorted to ground. (Refer to succeeding paragraphs describing wake-up behavior.)

DEVICE POWER-UP (AWAKE TRANSITIONAL MODE)

At power-up (V_{SUP} rises from zero), the 33661 automatically switches to the Awake transitional mode. It switches the INH pin to High state and RXD to Low state. The MCU of the application will then confirm Normal or Slow mode by setting the TXD and EN pins appropriately.

DEVICE WAKE-UP EVENTS

The 33661 can be awakened from Sleep mode by three wake-up events:

- Remote wake-up via LIN bus activity
- Internal node wake-up via the EN pin
- Toggling the WAKE pin

Remote Wake from LIN Bus (Awake Transitional Mode)

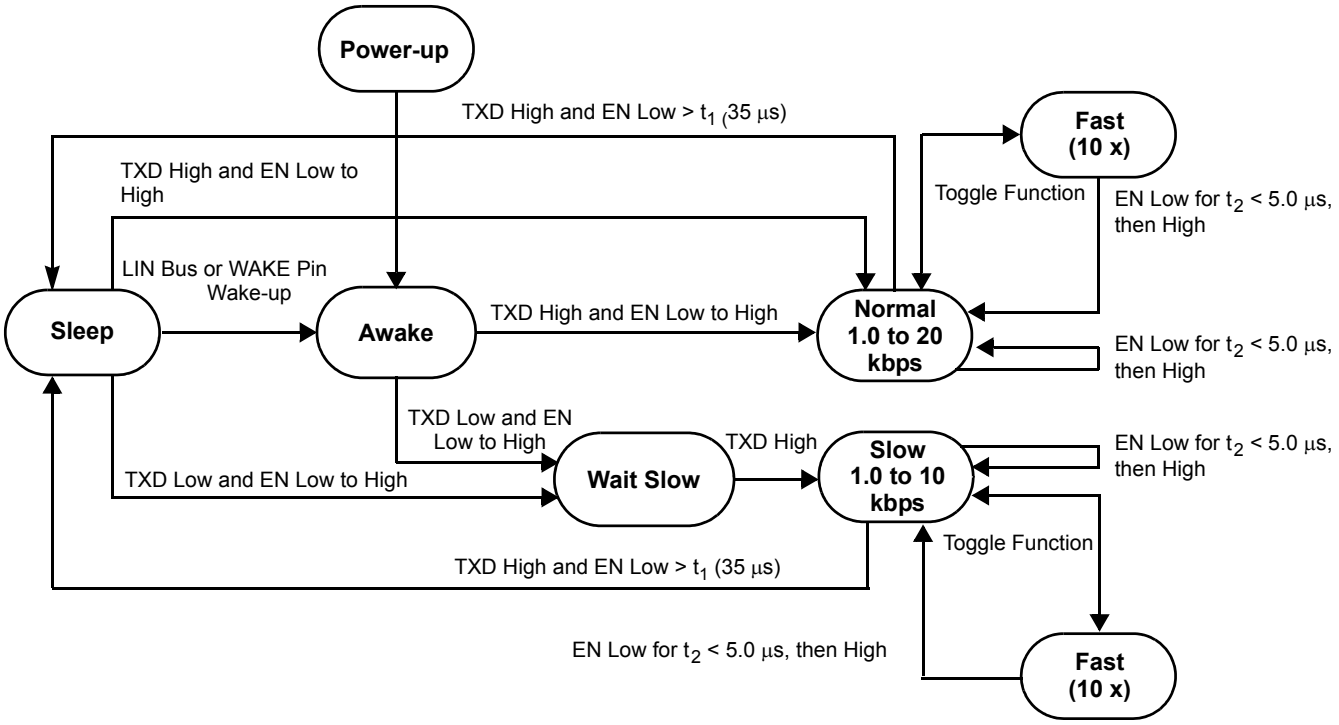
The LIN bus wake-up is recognized by a recessive-to-dominant transition, followed by a dominant level with a duration greater than 70 µs, followed by a dominant-to-recessive transition. This is illustrated in Figures 11 and 12. Once the wake-up is detected, the 33661 enters the Awake Transitional mode, with INH High and RXD pulled Low.

Wake-up from Internal Node Activity (Normal or Wait Slow Mode)

The 33661 can wake-up by internal node activity through a Low-to-High transition of the EN pin. When EN is switched from Low-to-High, the device is awakened and enters either the Normal or the Wait Slow transitional mode depending on the level of TXD input. The MCU must set the TXD pin LOW or HIGH prior to waking up the device through the EN pin.

Wake-up from WAKE Pin (Awake Transitional Mode)

If the WAKE input pin is toggled, the 33661 enters the Awake transitional mode, with INH High and RXD pulled Low.



Note Refer to Table 5 for explanation.

Figure 15. Operational and Transitional Modes State Diagram

Table 5. Explanation of Operational and Transitional Modes State Diagram

Operational/ Transitional	LIN	INH	EN	TXD	RXD
Sleep Mode	Recessive state, driver off. 20 µA pull-up current source.	Low	Low	X	High-impedance. High if external pull-up to V_{DD}.
Awake	Recessive state, driver off. 30 kΩ pull-up active.	High	Low	X	Low. If external pull-up, High-to-Low transition reports wake-up.
Normal Mode	Driver active. 30 kΩ pull-up active. Slew rate normal (20 kbps).	High	High	High to enter Normal mode. Once in Normal mode: Low to drive LIN bus in dominant, High to drive LIN bus in recessive.	Report LIN bus level: • Low LIN bus dominant • High LIN bus recessive
Wait Slow	Recessive state. Driver off. 30 kΩ pull-up active.	High	High	Low	High
Slow	Driver active. 30 kΩ pull-up active. Slew rate slow (10 kbps).	High	High	Low to enter Slow mode. Once in Slow mode: Low to drive LIN bus in dominant, High to drive LIN bus in recessive.	Report LIN bus level: • Low LIN bus dominant • High LIN bus recessive
Fast	Driver active. 30 kΩ pull-up active. Slew rate fast (>100 kbps).	High	High	Low to drive LIN bus in dominant, High to drive LIN bus in recessive.	Report LIN bus level: • Low LIN bus dominant • High LIN bus recessive

X = Don't care.

ELECTROMAGNETIC COMPATIBILITY

RADIATED EMISSION IN NORMAL AND SLOW MODES

The 33661 has been tested for radiated emission performances. Figures 16 and 17 show the results in the frequency range 100 kHz to 2.0 MHz. Test conditions are in accordance with CISPR25 recommendations, bus length of 1.5 meters, device loaded with 10 nF and 500 Ω bus impedance.

Figure 16 displays the results when the device is set in the Normal mode, optimized for baud rate up to 20 kbps. Figure 17 displays the results when the device is set in the Slow mode, optimized for baud rate up to 10 kbps. The level of emissions is significantly reduced compared to the already excellent level of the Normal mode.

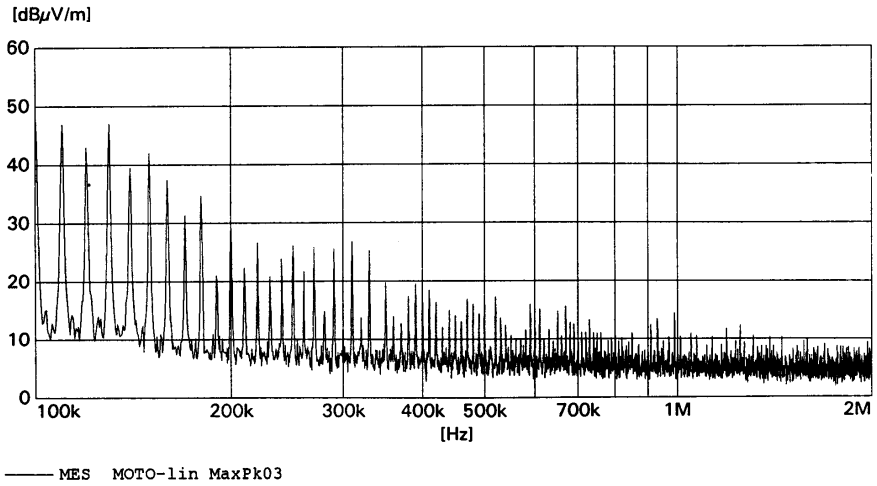


Figure 16. Radiated Emission in Normal Mode

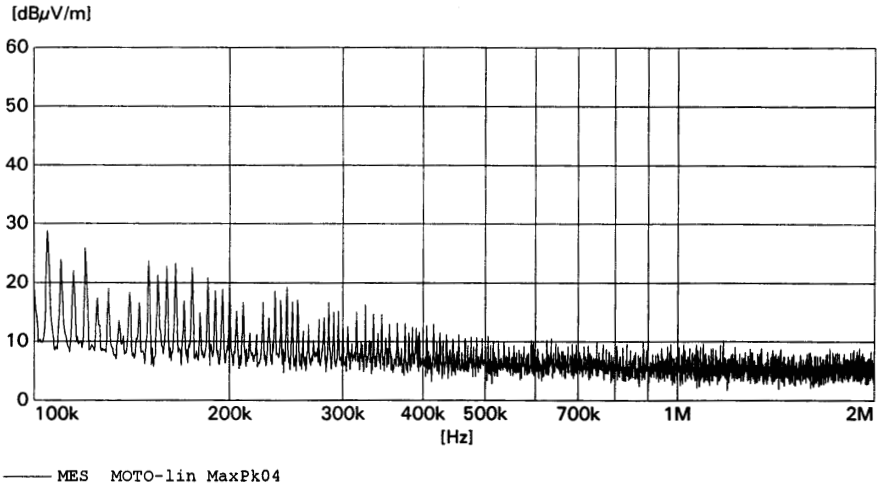


Figure 17. Radiated Emission in Slow Mode

TYPICAL APPLICATIONS

The 33661 can be configured in several applications. Figures 18 and 19 show master and slave node applications.

An additional pull-up resistor of 1.0 kΩ in series with a diode must be added when the device is used in the master node.

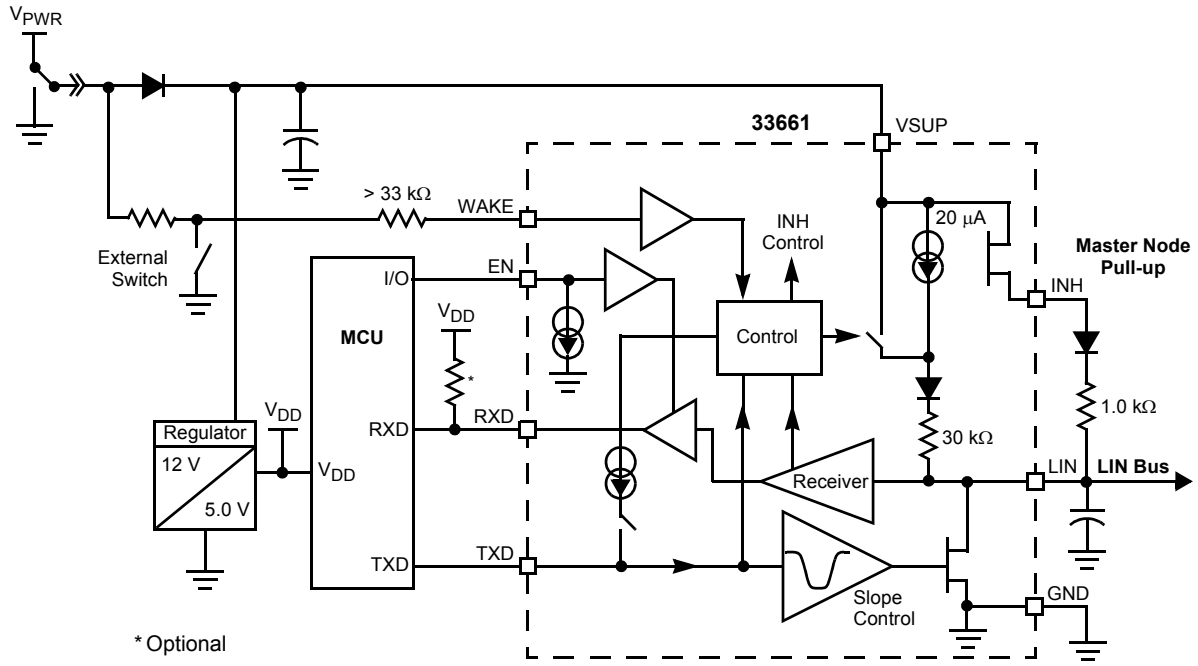


Figure 18. Master Node Typical Application

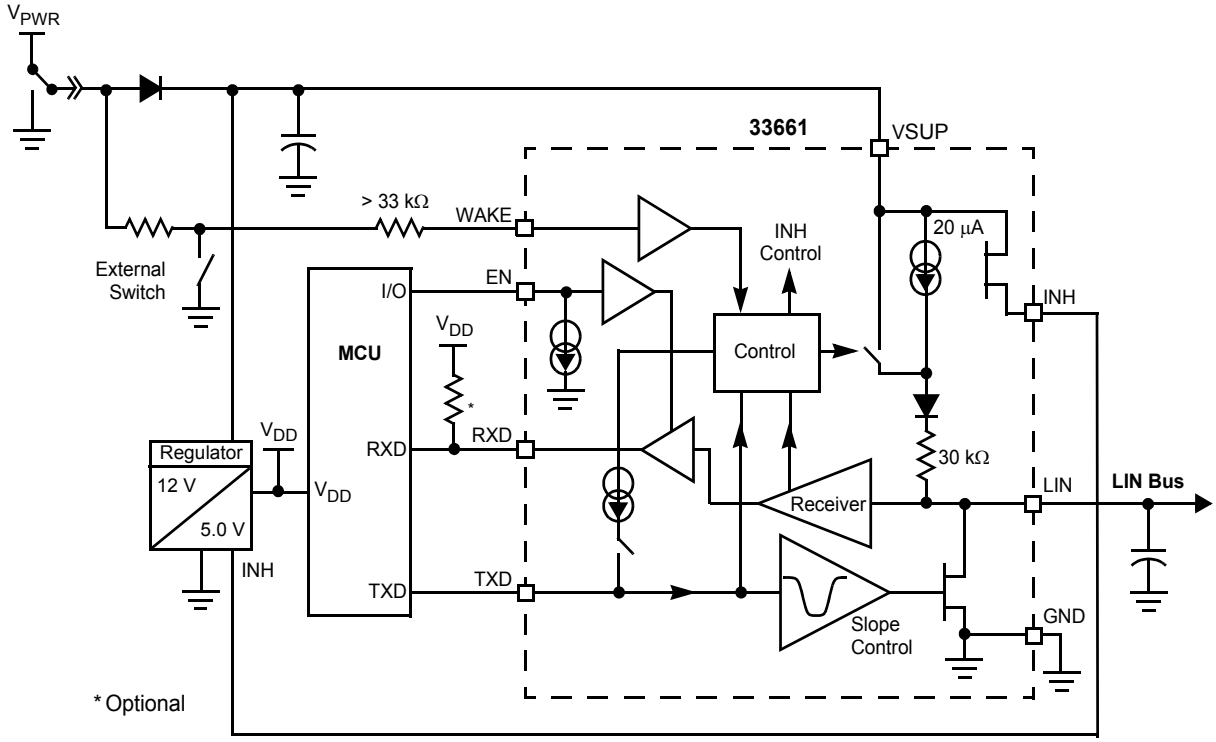
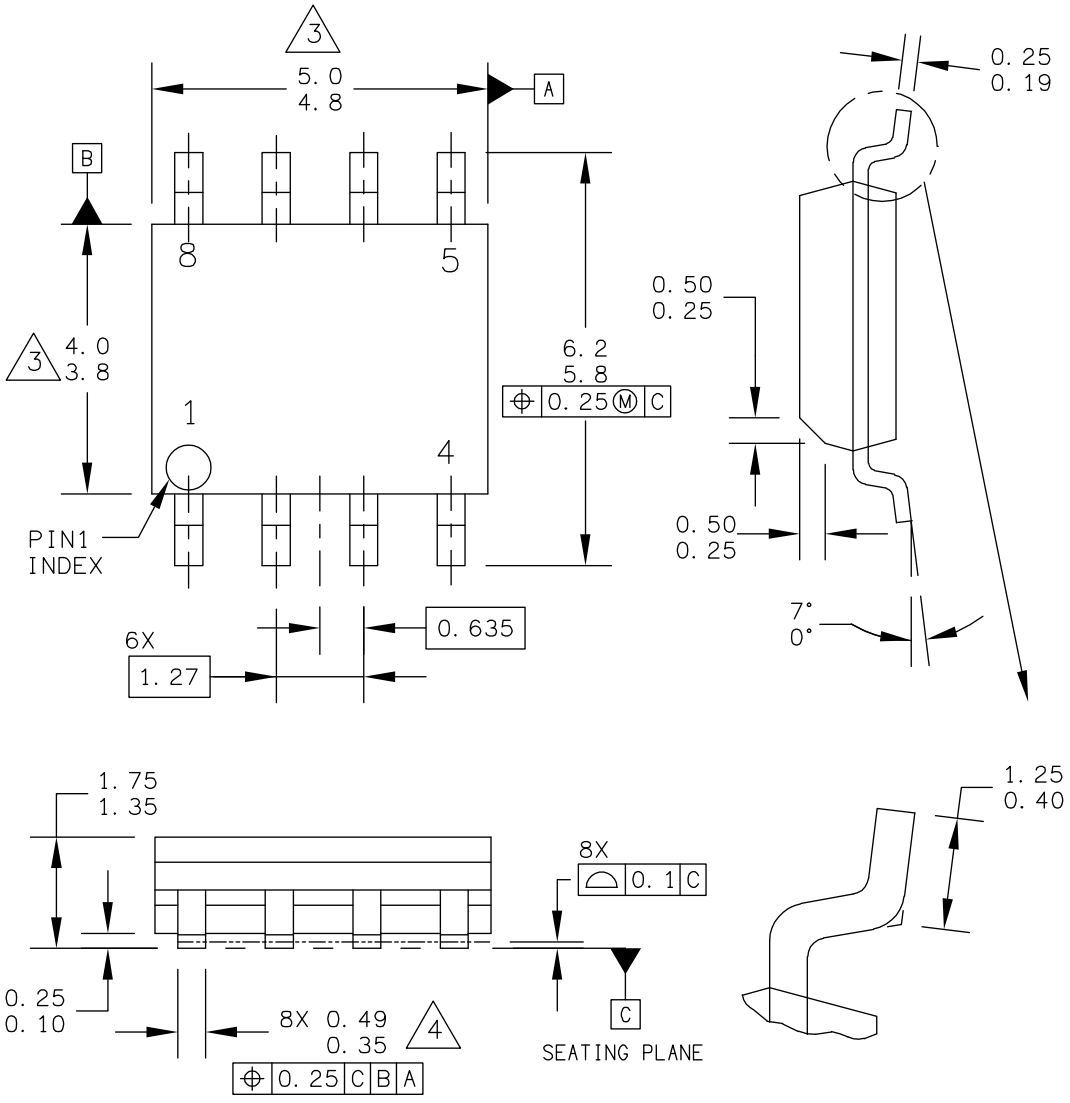


Figure 19. Slave Node Typical Application

PACKAGING

PACKAGE DIMENSIONS

Important For the most current revision of the package, visit www.freescale.com and do a keyword search on the 98ASB42564B drawing number below.Dimensions shown are provided for reference ONLY.



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TITLE: 8LD SOIC NARROW BODY	DOCUMENT NO: 98ASB42564B	REV: V
	CASE NUMBER: 751-07	20 NOV 2007
	STANDARD: JEDEC MS-012AA	

EF SUFFIX (PB-FREE)
8-PIN SOIC NARROW BODY
98ASB42564B
ISSUE V

33661

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42564B	REV: V
8LD SOIC NARROW BODY	CASE NUMBER: 751–07	20 NOV 2007
	STANDARD: JEDEC MS–012AA	

EF SUFFIX (PB-FREE)
8-PIN SOIC NARROW BODY
98ASB42564B
ISSUE V

33661

REFERENCE DOCUMENTS

Table 6. Reference Documents

Title	Literature Number
Local Interconnect Network (LIN) Physical Interface: Difference Between MC33399 and MC33661	EB215

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
5.0	10/2006	• Implemented Revision History page • Updated the Freescale format and style • Added MCZ33661EF/R2 to the part number Ordering Information
6.0	11/2006	• Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from MAXIMUM RATINGS 4. Added note with instructions from www.freescale.com.
7.0	2/2012	• Updated Freescale format and package drawing. No content was altered. • Updated ordering information. Removed MC33661D/R2 and MCZ33662EF/R2, and replaced with MC33661PEF/R2.
	4/2012	• Corrected the definition of LIN • Updated Freescale form and style
8.0	4/2013	• Change T_{STG} to -55 to 150 • Revised back page. Updated document properties. Added SMARTMOS sentence to first paragraph.

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