

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74AC166P, TC74AC166F

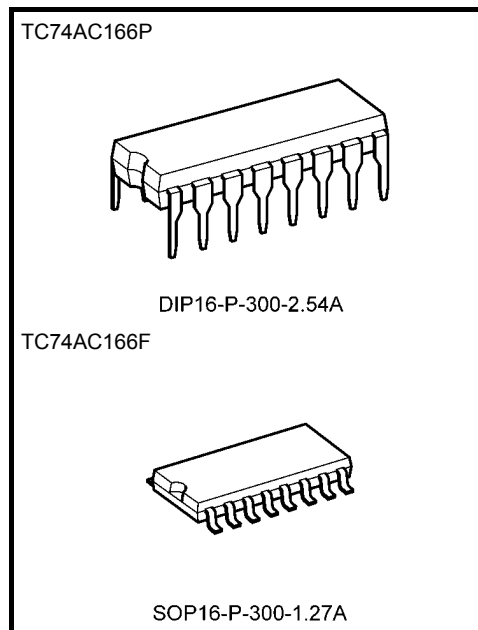
8-Bit Shift Register (P-IN, S-OUT)

The TC74AC166 is an advanced high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8-bit shift register with a gated clock input and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/LOAD input. When the SHIFT/LOAD input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting on each clock pulse. When held low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high transition of the clock pulse. The CLOCK-INHIBIT input should be shifted high only while the CLOCK input is held high. A direct clear input overrides all other inputs, including the clock, and sets all the flip-flops to zero. Functional details are shown in the truth table and the timing charts.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

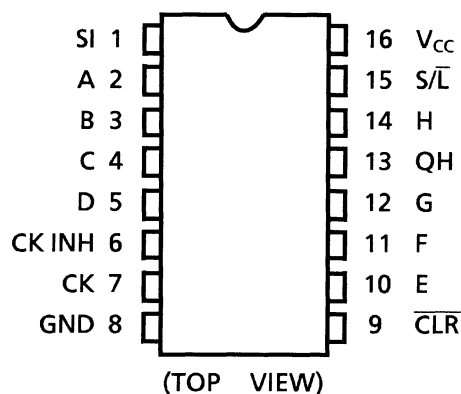


| | |
|-------------------|-----------------|
| Weight | |
| DIP16-P-300-2.54A | : 1.00 g (typ.) |
| SOP16-P-300-1.27A | : 0.18 g (typ.) |

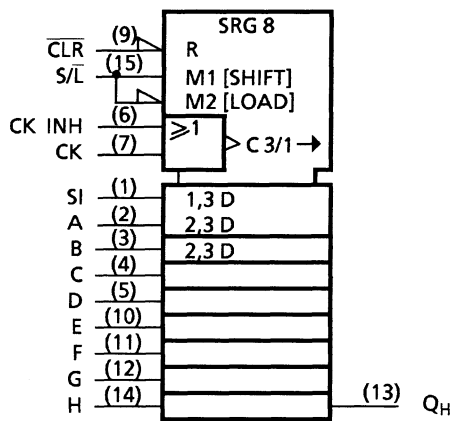
Features

- High speed: $f_{max} = 170$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 8$ μ A (max) at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 24$ mA (min)
Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Wide operating voltage range: $V_{CC}(\text{opr}) = 2$ to 5.5 V
- Pin and function compatible with 74HC166

Pin Assignment



IEC Logic Symbol



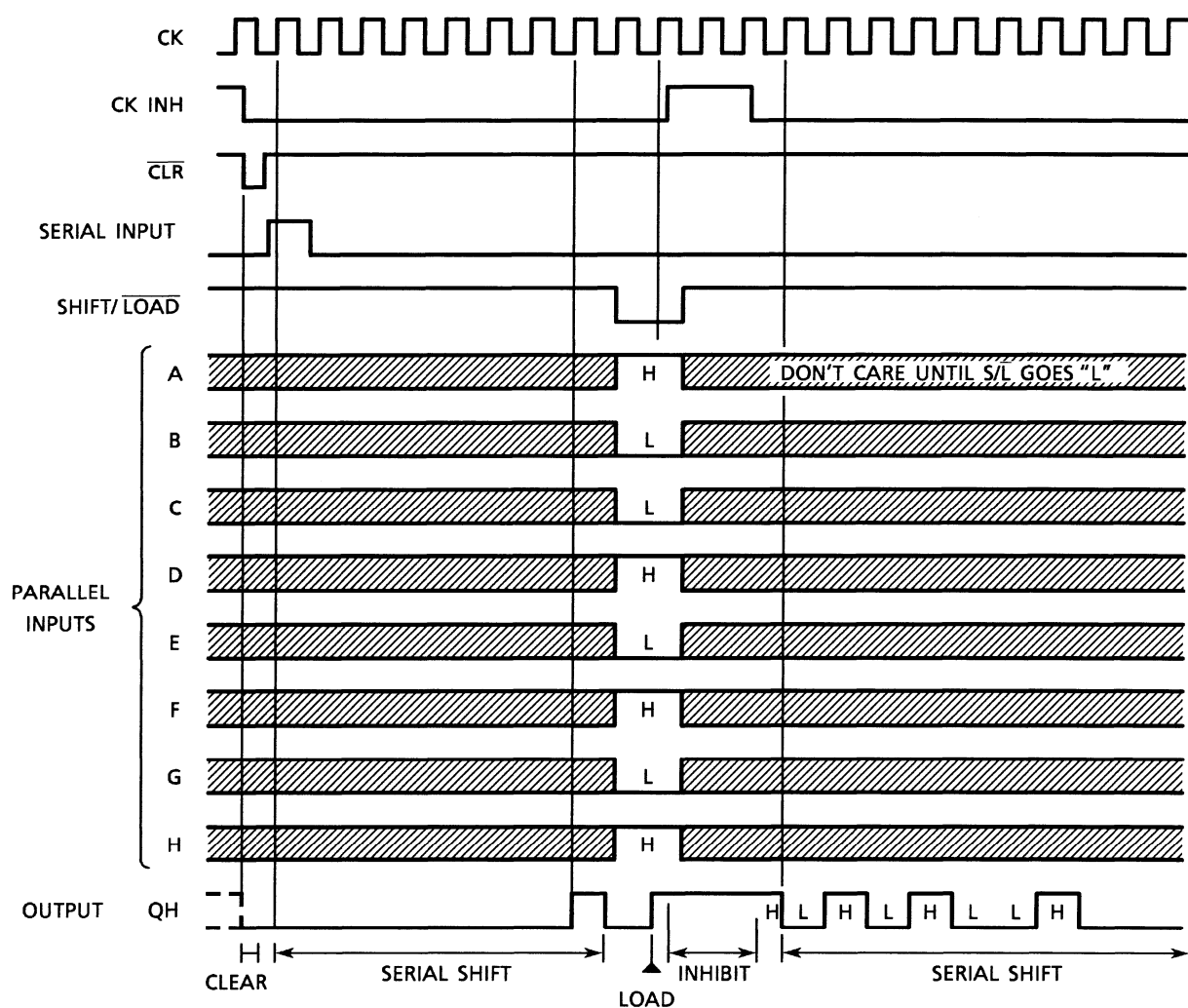
Truth Table

| Inputs | | | | | | Internal Output | | Output |
|--------|------------|---------|----|-----------|------------------|-----------------|-----|--------|
| CLR | SHIFT/LOAD | CK INH. | CK | SERIAL IN | PARALLEL A.....H | QA | QB | QH |
| L | X | X | X | X | X | L | L | L |
| H | X | X | | X | X | No Change | | |
| H | L | L | | X | a.....h | a | b | h |
| H | H | L | | H | X | H | QAn | QGn |
| H | H | L | | L | X | L | QAn | QGn |
| H | X | H | X | X | X | No Change | | |

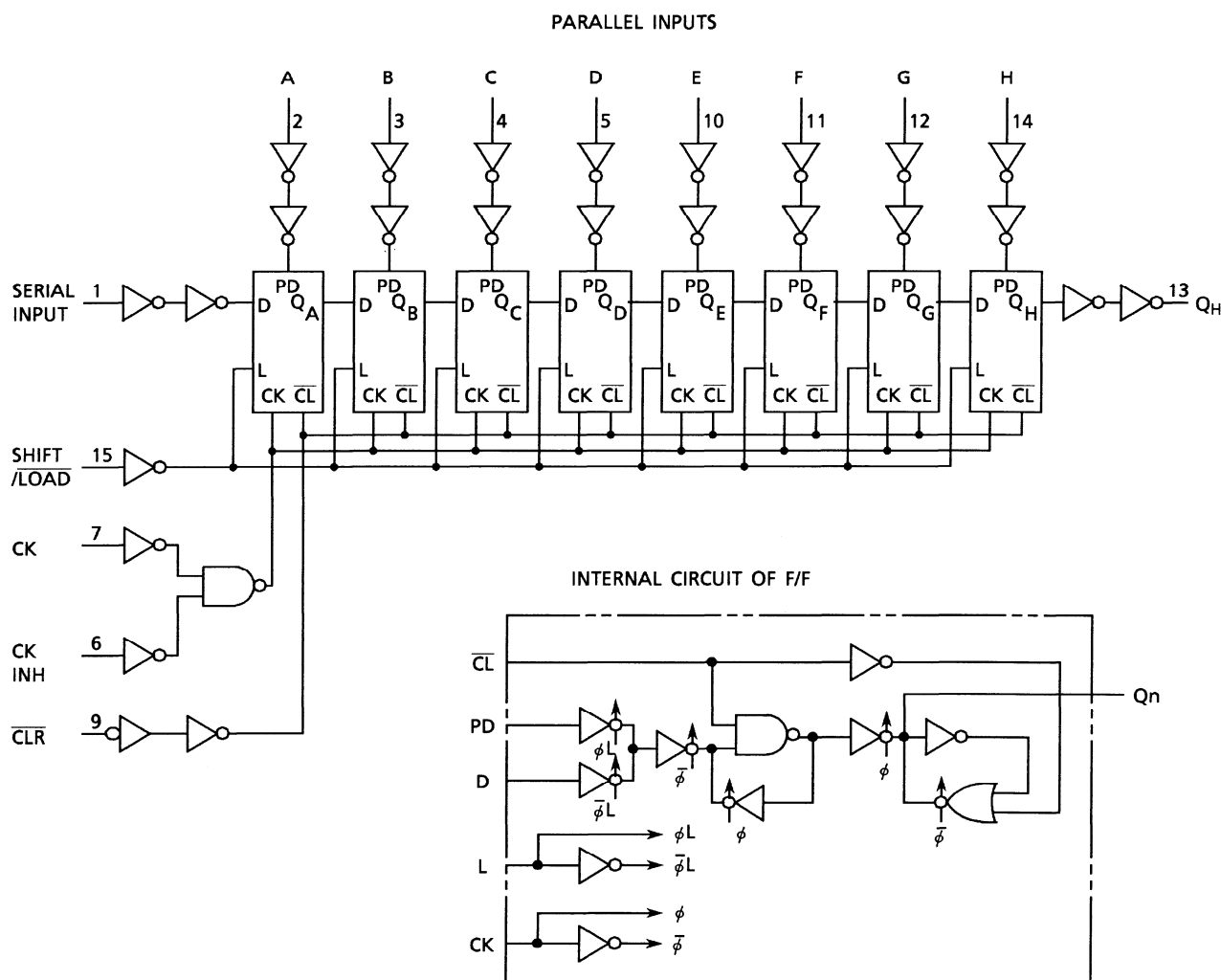
X: Don't care

a.....h: The level of steady state input voltage at inputs A through H respectively

Timing Chart



System Diagram



Absolute Maximum Ratings (Note 1)

| Characteristics | Symbol | Rating | Unit |
|-----------------------------|-----------|------------------------------|--------------------|
| Supply voltage range | V_{CC} | -0.5 to 7.0 | V |
| DC input voltage | V_{IN} | -0.5 to $V_{CC} + 0.5$ | V |
| DC output voltage | V_{OUT} | -0.5 to $V_{CC} + 0.5$ | V |
| Input diode current | I_{IK} | ± 20 | mA |
| Output diode current | I_{OK} | ± 50 | mA |
| DC output current | I_{OUT} | ± 50 | mA |
| DC V_{CC} /ground current | I_{CC} | ± 100 | mA |
| Power dissipation | P_D | 500 (DIP) (Note 2)/180 (SOP) | mW |
| Storage temperature | T_{stg} | -65 to 150 | $^{\circ}\text{C}$ |

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of -10 mW/ $^{\circ}\text{C}$ should be applied up to 300 mW.

Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
|--------------------------|-----------|---|------|
| Supply voltage | V_{CC} | 2.0 to 5.5 | V |
| Input voltage | V_{IN} | 0 to V_{CC} | V |
| Output voltage | V_{OUT} | 0 to V_{CC} | V |
| Operating temperature | T_{opr} | -40 to 85 | °C |
| Input rise and fall time | dt/dV | 0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V) | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

| Characteristics | Symbol | Test Condition | | V _{CC} (V) | Ta = 25°C | | | Ta = -40 to 85°C | | Unit |
|---------------------------|-----------------|--|--|------------------------|----------------------|-------------|----------------------|----------------------|----------------------|------|
| | | | | | Min | Typ. | Max | Min | Max | |
| High-level input voltage | V _{IH} | — | | 2.0 3.0 5.5 | 1.50 2.10 3.85 | — — — | — — — | 1.50 2.10 3.85 | — — — | V |
| Low-level input voltage | V _{IL} | — | | 2.0 3.0 5.5 | — — — | — — — | 0.50 0.90 1.65 | — — — | 0.50 0.90 1.65 | V |
| High-level output voltage | V _{OH} | V _{IN} = V _{IH} or V _{IL} | I _{OH} = -50 μA | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | 3.0 | 2.9 | 3.0 | — | 2.9 | — | |
| | | | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | |
| | | | I _{OH} = -4 mA I _{OH} = -24 mA I _{OH} = -75 mA (Note) | 3.0 | 2.58 | — | — | 2.48 | — | |
| | | | | 4.5 | 3.94 | — | — | 3.80 | — | |
| Low-level output voltage | V _{OL} | V _{IN} = V _{IH} or V _{IL} | I _{OL} = 50 μA | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | | 3.0 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | I _{OL} = 12 mA I _{OL} = 24 mA I _{OL} = 75 mA (Note) | 3.0 | — | — | 0.36 | — | 0.44 | |
| | | | | 4.5 | — | — | 0.36 | — | 0.44 | |
| Input leakage current | I _{IN} | V _{IN} = V _{CC} or GND | | 5.5 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent supply current | I _{CC} | V _{IN} = V _{CC} or GND | | 5.5 | — | — | 8.0 | — | 80.0 | μA |

Note: This spec indicates the capability of driving 50 Ω transmission lines.
One output should be tested at a time for a 10 ms maximum duration.

Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$)

| Characteristics | Symbol | Test Condition | V _{CC} (V) | Ta = 25°C Limit | Ta = -40 to 85°C Limit | Unit |
|---|------------------------|----------------|---------------------|--------------------|---------------------------|------|
| | | | | | | |
| Minimum pulse width (CK) | t_W (H) t_W (L) | — | 3.3 ± 0.3 | 7.0 | 7.0 | ns |
| | | | 5.0 ± 0.5 | 5.0 | 5.0 | |
| Minimum pulse width ($\overline{\text{CLR}}$) | t_W (L) | — | 3.3 ± 0.3 | 8.0 | 8.0 | ns |
| | | | 5.0 ± 0.5 | 5.0 | 5.0 | |
| Minimum set-up time (SI, PI) | t_s | — | 3.3 ± 0.3 | 8.0 | 8.0 | ns |
| | | | 5.0 ± 0.5 | 4.0 | 4.0 | |
| Minimum set-up time (S/\overline{L}) | t_s | — | 3.3 ± 0.3 | 7.0 | 7.0 | ns |
| | | | 5.0 ± 0.5 | 4.0 | 4.0 | |
| Minimum hold time (SI, PI) | t_h | — | 3.3 ± 0.3 | 0.5 | 0.5 | ns |
| | | | 5.0 ± 0.5 | 0.5 | 0.5 | |
| Minimum hold time (S/\overline{L}) | t_h | — | 3.3 ± 0.3 | 1.0 | 1.0 | ns |
| | | | 5.0 ± 0.5 | 1.0 | 1.0 | |
| Minimum removal time ($\overline{\text{CLR}}$) | t_{rem} | — | 3.3 ± 0.3 | 4.0 | 4.0 | ns |
| | | | 5.0 ± 0.5 | 1.5 | 1.5 | |

AC Characteristics (C_L = 50 pF, R_L = 500 Ω, input: $t_r = t_f = 3 \text{ ns}$)

| Characteristics | Symbol | Test Condition | Ta = 25°C | | | Ta = -40 to 85°C | | Unit |
|--|--------------------------------------|----------------|---------------------|-----|------|------------------|-----|------|
| | | | V _{CC} (V) | Min | Typ. | Max | Min | Max |
| Propagation delay time (CK-QH) | t_{pLH} t_{pHL} | — | 3.3 ± 0.3 | — | 9.4 | 16.1 | 1.0 | 18.3 |
| | | | 5.0 ± 0.5 | — | 6.6 | 10.0 | 1.0 | 11.4 |
| Propagation delay time ($\overline{\text{CLR}}$ -QH) | t_{pHL} | — | 3.3 ± 0.3 | — | 9.2 | 15.2 | 1.0 | 17.4 |
| | | | 5.0 ± 0.5 | — | 6.4 | 9.6 | 1.0 | 10.9 |
| Maximum clock frequency | f_{max} | — | 3.3 ± 0.3 | 55 | 105 | — | 55 | — |
| | | | 5.0 ± 0.5 | 90 | 150 | — | 90 | — |
| Input capacitance | C _{IN} | — | — | — | 5 | 10 | — | 10 |
| Power dissipation capacitance | C _{PD} (Note) | — | — | — | 67 | — | — | — |

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

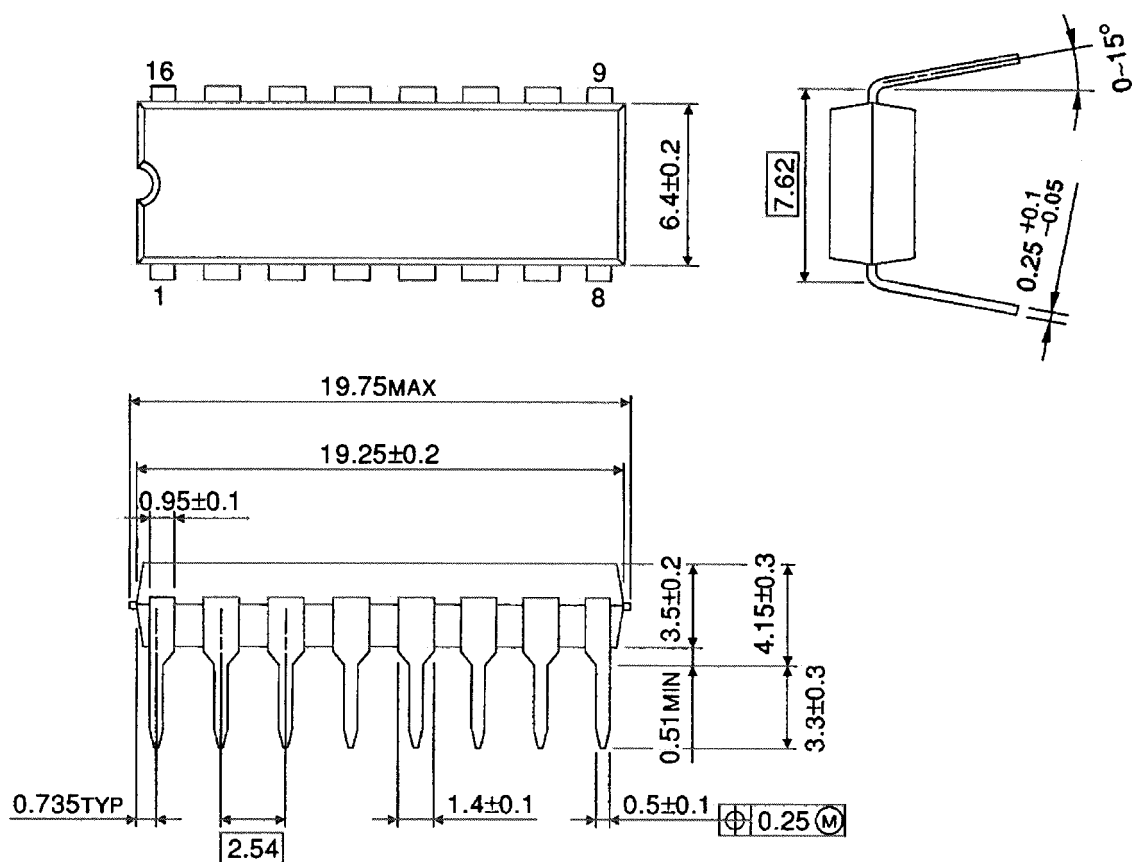
Average operating current can be obtained by the equation:

$$I_{\text{CC}} (\text{opr}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}$$

Package Dimensions

DIP16-P-300-2.54A

Unit : mm

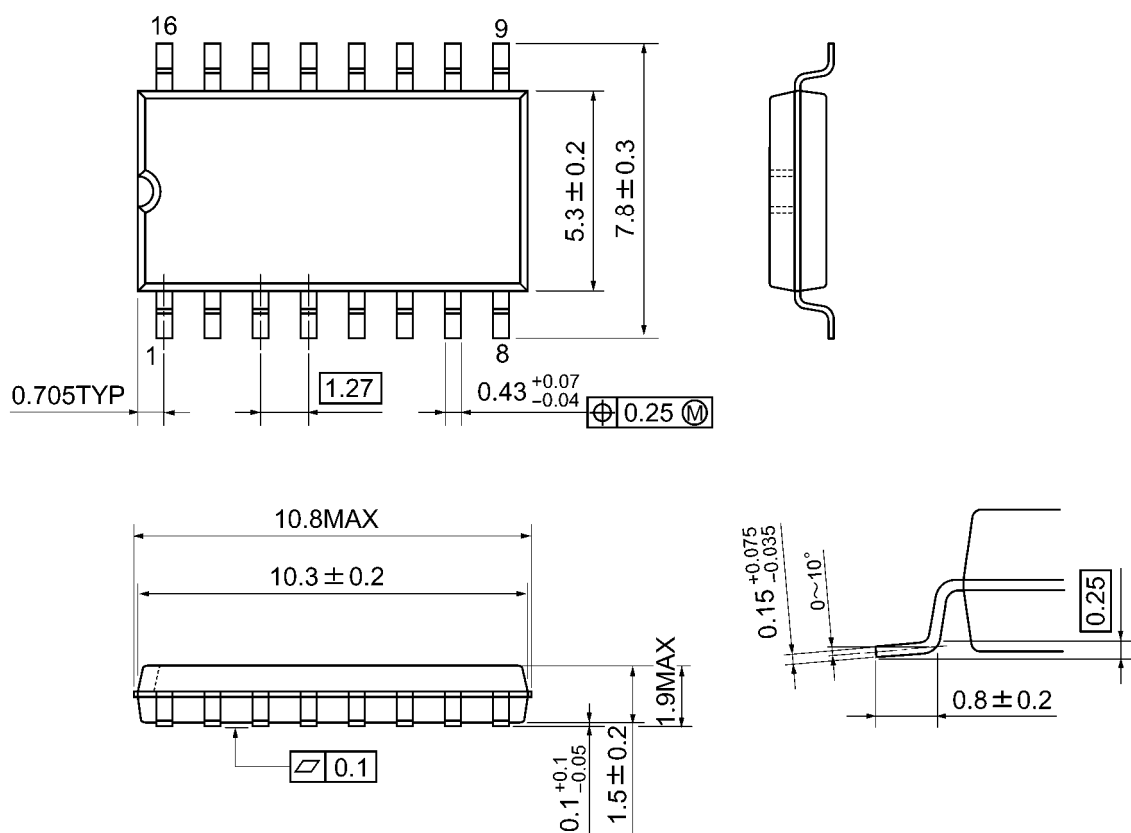


Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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