



16-BIT, 1.25 MSPS, PSEUDO-BIPOLAR, FULLY DIFFERENTIAL INPUT, MICRO POWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH PARALLEL INTERFACE

FEATURES

- Pseudo-Bipolar, Fully Differential Input, $-V_{REF}$ to V_{REF}
- 16-Bit NMC at 1.25 MSPS
- ± 2 LSB INL Max, $-1/+1.25$ LSB DNL
- 90 dB SNR, -95 dB THD at 100 kHz Input
- Zero Latency
- Internal 4.096 V Reference
- High-Speed Parallel Interface
- Single 5 V Analog Supply
- Wide I/O Supply: 2.7 V to 5.25 V
- Low Power: 155 mW at 1.25 MHz Typ
- Pin Compatible With ADS8412/8402
- 48-Pin TQFP Package

APPLICATIONS

- DWDM
- Instrumentation
- High-Speed, High-Resolution, Zero Latency Data Acquisition Systems
- Transducer Interface
- Medical Instruments
- Communications

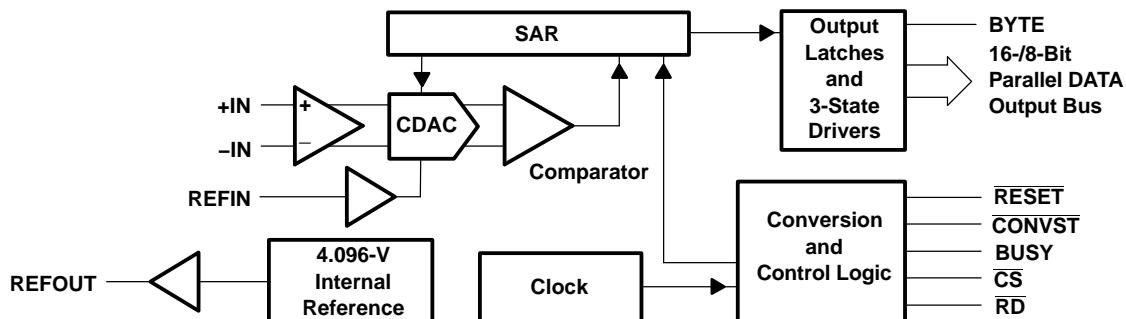
DESCRIPTION

The ADS8406 is a 16-bit, 1.25 MHz A/D converter with an internal 4.096-V reference. The device includes a 16-bit capacitor-based SAR A/D converter with inherent sample and hold. The ADS8406 offers a full 16-bit interface and an 8-bit option where data is read using two 8-bit read cycles.

The ADS8406 has a pseudo-bipolar, fully differential input. It is available in a 48-lead TQFP package and is characterized over the industrial -40°C to 85°C temperature range.

High Speed SAR Converter Family

Type/Speed	500 kHz	580 kHz	750 MHz	1.25 MHz	2 MHz	3 MHz	4 MHz
18 Bit Pseudo-Diff	ADS8383	ADS8381					
16 Bit Pseudo-Diff			ADS8371	ADS8401	ADS8411		
				ADS8405			
16 Bit Pseudo Bipolar, Fully Differential				ADS8402	ADS8412		
				ADS8406			
14 Bit Pseudo-Diff				ADS7890 (S)		ADS7891	
12 Bit Pseudo-Diff							ADS7881



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS8406I	−4 to +4	−2 to +2	15	48 Pin TQFP	PFB	−40°C to 85°C	ADS8406IPFBT	Tape and reel 250
							ADS8406IPFBR	Tape and reel 1000
ADS8406IB	−2 to +2	−1 to +1.25	16	48 Pin TQFP	PFB	−40°C to 85°C	ADS8406IBPFBT	Tape and reel 250
							ADS8406IBPFBR	Tape and reel 1000

(1) For the most current specifications and package information, refer to our website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

			UNIT
Voltage	+IN to AGND		−0.4 V to +VA + 0.1 V
	−IN to AGND		−0.4 V to +VA + 0.1 V
Voltage range	+VA to AGND		−0.3 V to 7 V
	+VBD to BDGND		−0.3 V to 7 V
	+VA to +VBD		−0.3 V to 2.55 V
Digital input voltage to BDGND			−0.3 V to +VBD + 0.3 V
Digital output voltage to BDGND			−0.3 V to +VBD + 0.3 V
T _A	Operating free-air temperature range		−40°C to 85°C
T _{stg}	Storage temperature range		−65°C to 150°C
Junction temperature (T _J max)			150°C
TQFP package	Power dissipation		(T _J Max - T _A)/θ _{JA}
	θ _{JA} thermal impedance		86°C/W
Lead temperature, soldering	Vapor phase (60 sec)		215°C
	Infrared (15 sec)		220°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SPECIFICATIONS

TA = -40°C to 85°C, +VA = 5 V, +VBD = 3 V or 5 V, Vref = 4.096 V, fSAMPLE = 1.25 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
ANALOG INPUT							
Full-scale input voltage ⁽¹⁾		+IN – (–IN)		-Vref	Vref	V	
Absolute input voltage		+IN	-0.2	Vref + 0.2		V	
		-IN	-0.2	Vref + 0.2			
Input capacitance				25		pF	
Input leakage current				0.5		nA	
SYSTEM PERFORMANCE							
Resolution				16		Bits	
No missing codes	ADS8406I		15			Bits	
	ADS8406IB		16				
INL	ADS8406I		-4	±2	4	LSB	
	ADS8406IB		-2	±1	2		
DNL	ADS8406I		-2	±1	2	LSB	
	ADS8406IB		-1	±0.5	1.25		
EO	ADS8406I		-2.5	±1	2.5	mV	
	ADS8406IB		-1.5	±0.5	1.5	mV	
EG	ADS8406I		-0.12		0.12	%FS	
	ADS8406IB		-0.098		0.098		
CMRR	Common mode rejection ratio		At dc (0.2 V around Vref/2)	80		dB	
	+IN – (–IN) = 1 V _{pp} at 1 MHz			80			
PSRR	DC Power supply rejection ratio		At 7FFFh output code, +VA = 4.75 V to 5.25 V, Vref = 4.096 V ⁽⁴⁾		2	LSB	
SAMPLING DYNAMICS							
Conversion time				500	650	ns	
Acquisition time				150		ns	
Throughput rate					1.25	MHz	
Aperture delay				2		ns	
Aperture jitter				25		ps	
Step response				100		ns	
Overvoltage recovery				100		ns	
DYNAMIC CHARACTERISTICS							
THD	Total harmonic distortion ⁽⁶⁾		V _{IN} = 8 V _{pp} at 100 kHz	-95		dB	
			V _{IN} = 8 V _{pp} at 500 kHz	-90			
SNR	Signal-to-noise ratio		V _{IN} = 8 V _{pp} at 100 kHz	90		dB	
SINAD	Signal-to-noise + distortion		V _{IN} = 8 V _{pp} at 100 kHz	88		dB	
SFDR	Spurious free dynamic range		V _{IN} = 8 V _{pp} at 100 kHz	95		dB	
			V _{IN} = 8 V _{pp} at 500 kHz	93			
-3dB Small signal bandwidth				5		MHz	
EXTERNAL VOLTAGE REFERENCE INPUT							
Reference voltage at REFIN, Vref				2.5	4.096	4.2	V
Reference resistance ⁽⁷⁾					500		kΩ

(1) Ideal input span, does not include gain or offset error.

(2) LSB means least significant bit.

(3) This is endpoint INL, not best fit.

(4) Measured relative to an ideal full-scale input [+IN – (–IN)] of 8.192 V.

(5) This specification does not include the internal reference voltage error and drift.

(6) Calculated on the first nine harmonics of the input frequency.

(7) Can vary ±20%.

SPECIFICATIONS (continued)

$T_A = -40^\circ\text{C}$ to 85°C , $+VA = 5\text{ V}$, $+VBD = 3\text{ V}$ or 5 V , $V_{\text{ref}} = 4.096\text{ V}$, $f_{\text{SAMPLE}} = 1.25\text{ MHz}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
INTERNAL REFERENCE OUTPUT						
Internal reference start-up time	From 95% ($+VA$) with 1- μF storage capacitor			120	ms	
V_{ref}	$I_{\text{OUT}} = 0$	4.065	4.096	4.13	V	
Source current	Static load			10	μA	
Line regulation	$+VA = 4.75$ to 5.25 V		0.6		mV	
Drift	$I_{\text{OUT}} = 0$		36		PPM/ $^\circ\text{C}$	
DIGITAL INPUT/OUTPUT						
Logic family — CMOS						
V_{IH}	$I_{\text{IH}} = 5\text{ }\mu\text{A}$		$+VBD - 1$	$+VBD + 0.3$	V	
V_{IL}	$I_{\text{IL}} = 5\text{ }\mu\text{A}$		-0.3	0.8		
V_{OH}	$I_{\text{OH}} = 2$ TTL loads		$+VBD - 0.6$	$+VBD$		
V_{OL}	$I_{\text{OL}} = 2$ TTL loads		0	0.4		
Data format — 2's complement						
POWER SUPPLY REQUIREMENTS						
Power supply voltage	$+VBD$		2.7	3	5.25	V
	$+VA$		4.75	5	5.25	V
Supply current, $+VA^{(8)}$		$f_s = 1.25\text{ MHz}$		31	34	mA
P_D	Power dissipation ⁽⁸⁾	$f_s = 1.25\text{ MHz}$		155	170	mW
TEMPERATURE RANGE						
T_A	Operating free-air temperature		-40	85	$^\circ\text{C}$	

(8) This includes only $+VA$ current. $+VBD$ current is typically 1 mA with 5-pF load capacitance on output pins.

TIMING CHARACTERISTICS

All specifications typical at -40°C to 85°C , $+\text{VA} = +\text{VBD} = 5\text{ V}$ ⁽¹⁾⁽²⁾⁽³⁾

PARAMETER	MIN	TYP	MAX	UNIT
t_{CONV} Conversion time	500	650		ns
t_{ACQ} Acquisition time	150			ns
t_{pd1} $\overline{\text{CONVST}}$ low to $\overline{\text{BUSY}}$ high		40		ns
t_{pd2} Propagation delay time, end of conversion to $\overline{\text{BUSY}}$ low		5		ns
t_{w1} Pulse duration, $\overline{\text{CONVST}}$ low	20			ns
t_{su1} Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low	0			ns
t_{w2} Pulse duration, $\overline{\text{CONVST}}$ high	20			ns
$\overline{\text{CONVST}}$ falling edge jitter		10		ps
t_{w3} Pulse duration, $\overline{\text{BUSY}}$ signal low	Min(t_{ACQ})			ns
t_{w4} Pulse duration, $\overline{\text{BUSY}}$ signal high	610			ns
t_{h1} Hold time, First data bus data transition ($\overline{\text{RD}}$ low, or $\overline{\text{CS}}$ low for read cycle, or BYTE input changes) after $\overline{\text{CONVST}}$ low	40			ns
t_{d1} Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low (or $\overline{\text{BUSY}}$ low to $\overline{\text{RD}}$ low when $\overline{\text{CS}} = 0$)	0			ns
t_{su2} Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high	0			ns
t_{w5} Pulse duration, $\overline{\text{RD}}$ low time	50			ns
t_{en} Enable time, $\overline{\text{RD}}$ low (or $\overline{\text{CS}}$ low for read cycle) to data valid		20		ns
t_{d2} Delay time, data hold from $\overline{\text{RD}}$ high	0			ns
t_{d3} Delay time, BYTE rising edge or falling edge to data valid	2	20		ns
t_{w6} Pulse duration, $\overline{\text{RD}}$ high	20			ns
t_{w7} Pulse duration, $\overline{\text{CS}}$ high time	20			ns
t_{h2} Hold time, last $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) rising edge to $\overline{\text{CONVST}}$ falling edge	50			ns
t_{su3} Setup time, BYTE transition to $\overline{\text{RD}}$ falling edge	0			ns
t_{h3} Hold time, BYTE transition to $\overline{\text{RD}}$ falling edge	0			ns
t_{dis} Disable time, $\overline{\text{RD}}$ high ($\overline{\text{CS}}$ high for read cycle) to 3-stated data bus		20		ns
t_{d5} Delay time, end of conversion to MSB data valid		10		ns
t_{su4} Byte transition setup time, from BYTE transition to next BYTE transition	50			ns
t_{d6} Delay time, $\overline{\text{CS}}$ rising edge to $\overline{\text{BUSY}}$ falling edge	50			ns
t_{d7} Delay time, $\overline{\text{BUSY}}$ falling edge to $\overline{\text{CS}}$ rising edge	50			ns
$t_{\text{su(AB)}}$ Setup time, from the falling edge of $\overline{\text{CONVST}}$ (used to start the valid conversion) to the next falling edge of $\overline{\text{CONVST}}$ (when $\overline{\text{CS}} = 0$ and $\overline{\text{CONVST}}$ used to abort) or to the next falling edge of $\overline{\text{CS}}$ (when $\overline{\text{CS}}$ is used to abort)	60	500		ns
t_{su5} Setup time, falling edge of $\overline{\text{CONVST}}$ to read valid data (MSB) from current conversion	MAX(t_{CONV}) + MAX(t_{d5})			ns
t_{h4} Hold time, data (MSB) from previous conversion hold valid from falling edge of $\overline{\text{CONVST}}$		MIN(t_{CONV})		ns

(1) All input signals are specified with $t_r = t_f = 5\text{ ns}$ (10% to 90% of $+V_{\text{BD}}$) and timed from a voltage level of $(V_{\text{IL}} + V_{\text{IH}})/2$.

(2) See timing diagrams.

(3) All timings are measured with 20-pF equivalent loads on all data bits and $\overline{\text{BUSY}}$ pins.

TIMING CHARACTERISTICS

All specifications typical at -40°C to 85°C , $+\text{VA} = 5\text{ V}$, $+\text{VBD} = 3\text{ V}$ ⁽¹⁾⁽²⁾⁽³⁾

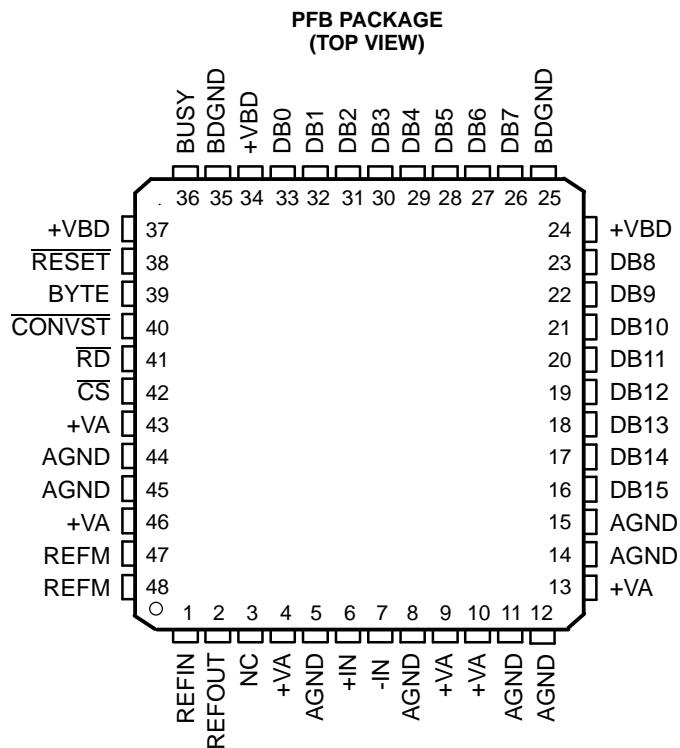
PARAMETER	MIN	TYP	MAX	UNIT
t_{CONV} Conversion time	500	650		ns
t_{ACQ} Acquisition time	150			ns
t_{pd1} $\overline{\text{CONVST}}$ low to $\overline{\text{BUSY}}$ high		50		ns
t_{pd2} Propagation delay time, end of conversion to $\overline{\text{BUSY}}$ low		10		ns
t_{w1} Pulse duration, $\overline{\text{CONVST}}$ low	20			ns
t_{su1} Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low	0			ns
t_{w2} Pulse duration, $\overline{\text{CONVST}}$ high	20			ns
$\overline{\text{CONVST}}$ falling edge jitter		10		ps
t_{w3} Pulse duration, $\overline{\text{BUSY}}$ signal low	Min(t_{ACQ})			ns
t_{w4} Pulse duration, $\overline{\text{BUSY}}$ signal high	610			ns
t_{h1} Hold time, first data bus transition ($\overline{\text{RD}}$ low, or $\overline{\text{CS}}$ low for read cycle, or BYTE or BUS 16/16 input changes) after $\overline{\text{CONVST}}$ low	40			ns
t_{d1} Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low (or $\overline{\text{BUSY}}$ low to $\overline{\text{RD}}$ low when $\overline{\text{CS}} = 0$)	0			ns
t_{su2} Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high	0			ns
t_{w5} Pulse duration, $\overline{\text{RD}}$ low	50			ns
t_{en} Enable time, $\overline{\text{RD}}$ low (or $\overline{\text{CS}}$ low for read cycle) to data valid		30		ns
t_{d2} Delay time, data hold from $\overline{\text{RD}}$ high	0			ns
t_{d3} Delay time, BYTE rising edge or falling edge to data valid	2	30		ns
t_{w6} Pulse duration, $\overline{\text{RD}}$ high time	20			ns
t_{w7} Pulse duration, $\overline{\text{CS}}$ high time	20			ns
t_{h2} Hold time, last $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) rising edge to $\overline{\text{CONVST}}$ falling edge	50			ns
t_{su3} Setup time, BYTE transition to $\overline{\text{RD}}$ falling edge	0			ns
t_{h3} Hold time, BYTE transition to $\overline{\text{RD}}$ falling edge	0			ns
t_{dis} Disable time, $\overline{\text{RD}}$ high ($\overline{\text{CS}}$ high for read cycle) to 3-stated data bus		30		ns
t_{d5} Delay time, end of conversion to MSB data valid		20		ns
t_{su4} Byte transition setup time, from BYTE transition to next BYTE transition	50			ns
t_{d6} Delay time, $\overline{\text{CS}}$ rising edge to $\overline{\text{BUSY}}$ falling edge	50			ns
t_{d7} Delay time, $\overline{\text{BUSY}}$ falling edge to $\overline{\text{CS}}$ rising edge	50			ns
$t_{\text{su(AB)}}$ Setup time, from the falling edge of $\overline{\text{CONVST}}$ (used to start the valid conversion) to the next falling edge of $\overline{\text{CONVST}}$ (when $\overline{\text{CS}} = 0$ and $\overline{\text{CONVST}}$ used to abort) or to the next falling edge of $\overline{\text{CS}}$ (when $\overline{\text{CS}}$ is used to abort)	70	500		ns
t_{su5} Setup time, falling edge of $\overline{\text{CONVST}}$ to read valid data (MSB) from current conversion	MAX(t_{CONV}) + MAX(t_{d5})			ns
t_{h4} Hold time, data (MSB) from previous conversion hold valid from falling edge of $\overline{\text{CONVST}}$		MIN(t_{CONV})		ns

(1) All input signals are specified with $t_r = t_f = 5\text{ ns}$ (10% to 90% of $+\text{VBD}$) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

(2) See timing diagrams.

(3) All timings are measured with 20-pF equivalent loads on all data bits and $\overline{\text{BUSY}}$ pins.

PIN ASSIGNMENTS

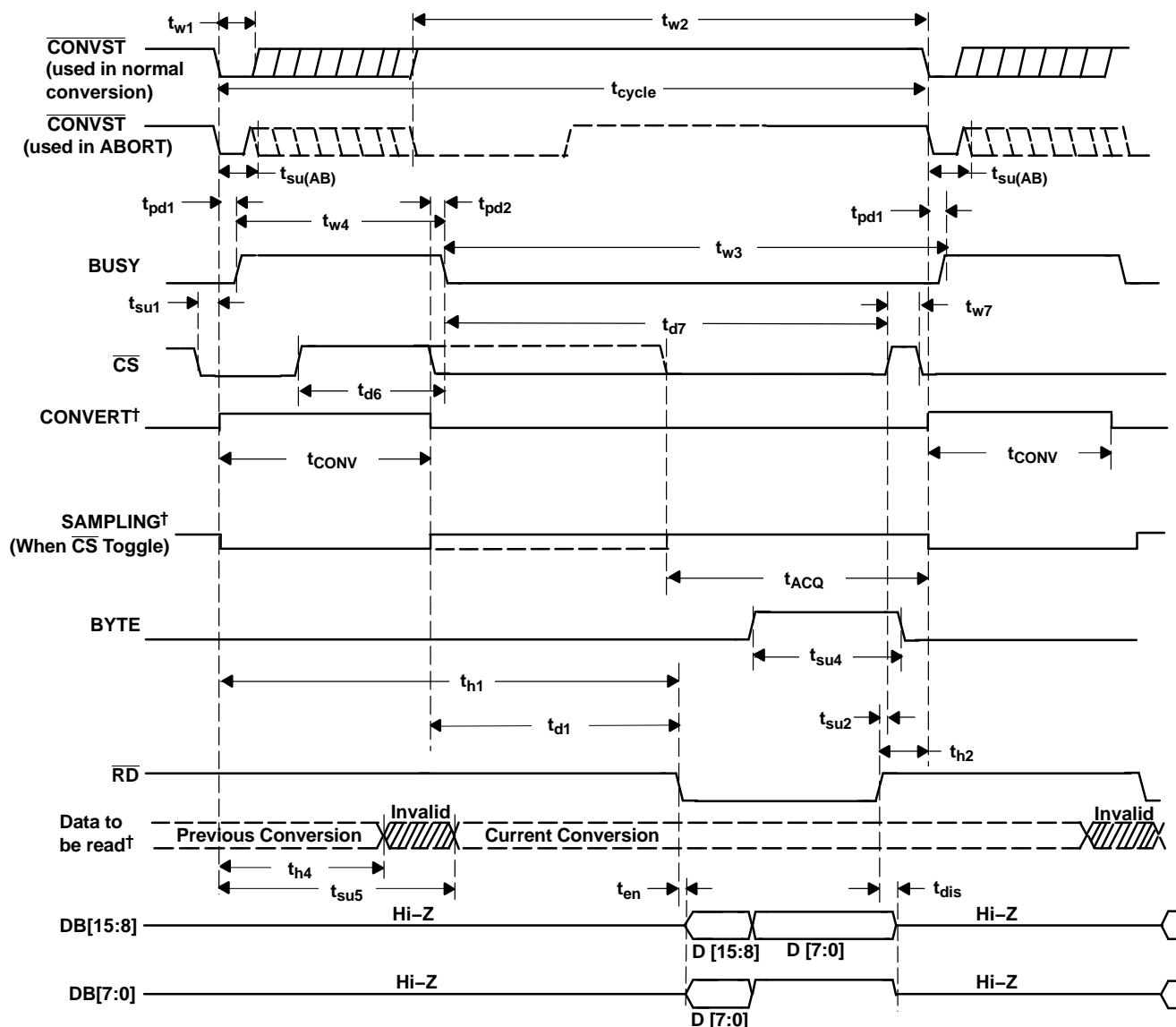


NC - No connection

Terminal Functions

NAME	NO.	I/O	DESCRIPTION		
AGND	5, 8, 11, 12, 14, 15, 44, 45	—	Analog ground		
BGND	25, 35	—	Digital ground for bus interface digital supply		
BUSY	36	O	Status output. High when a conversion is in progress.		
BYTE	39	I	Byte select input. Used for 8-bit bus reading. 0: No fold back 1: Low byte D[7:0] of the 16 most significant bits is folded back to high byte of the 16 most significant pins DB[15:8].		
CONVST	40	I	Convert start. The falling edge of this input ends the acquisition period and starts the hold period.		
CS	42	I	Chip select. The falling edge of this input starts the acquisition period.		
Data Bus			8-Bit Bus		16-Bit Bus
			BYTE = 0	BYTE = 1	BYTE = 0
DB15	16	O	D15 (MSB)	D7	D15 (MSB)
DB14	17	O	D14	D6	D14
DB13	18	O	D13	D5	D13
DB12	19	O	D12	D4	D12
DB11	20	O	D11	D3	D11
DB10	21	O	D10	D2	D10
DB9	22	O	D9	D1	D9
DB8	23	O	D8	D0 (LSB)	D8
DB7	26	O	D7	All ones	D7
DB6	27	O	D6	All ones	D6
DB5	28	O	D5	All ones	D5
DB4	29	O	D4	All ones	D4
DB3	30	O	D3	All ones	D3
DB2	31	O	D2	All ones	D2
DB1	32	O	D1	All ones	D1
DB0	33	O	D0 (LSB)	All ones	D0 (LSB)
-IN	7	I	Inverting input channel		
+IN	6	I	Non inverting input channel		
NC	3	—	No connection		
REFIN	1	I	Reference input		
REFM	47, 48	I	Reference ground		
REFOUT	2	O	Reference output. Add 1- μ F capacitor between the REFOUT pin and REFM pin when internal reference is used.		
RESET	38	I	Current conversion is aborted and output latches are cleared (set to zeros) when this pin is asserted low. RESET works independantly of CS.		
RD	41	I	Synchronization pulse for the parallel output. When CS is low, this serves as the output enable and puts the previous conversion result on the bus.		
+VA	4, 9, 10, 13, 43, 46	—	Analog power supplies, 5-V dc		
+VBD	24, 34, 37	—	Digital power supply for bus		

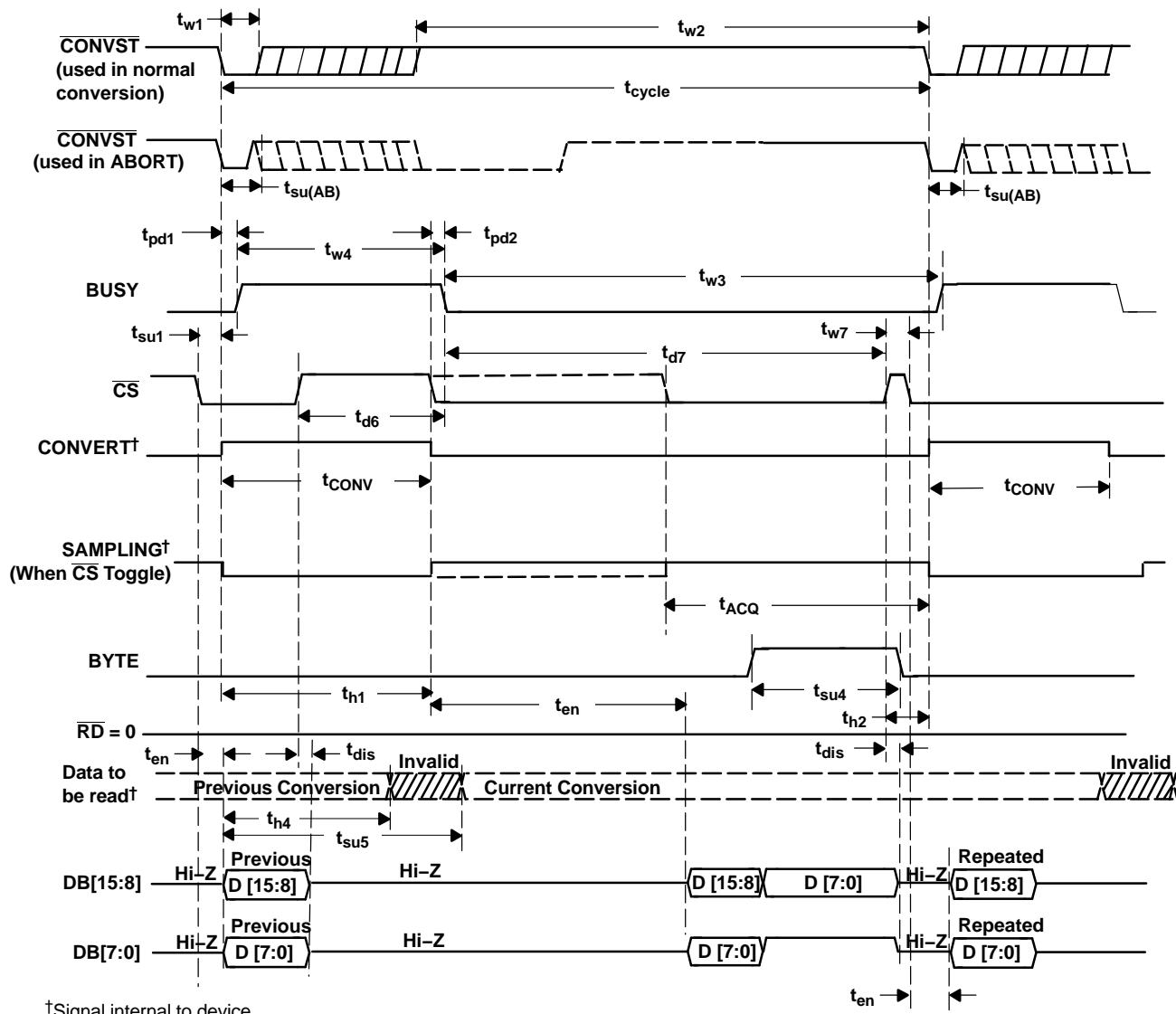
TIMING DIAGRAMS



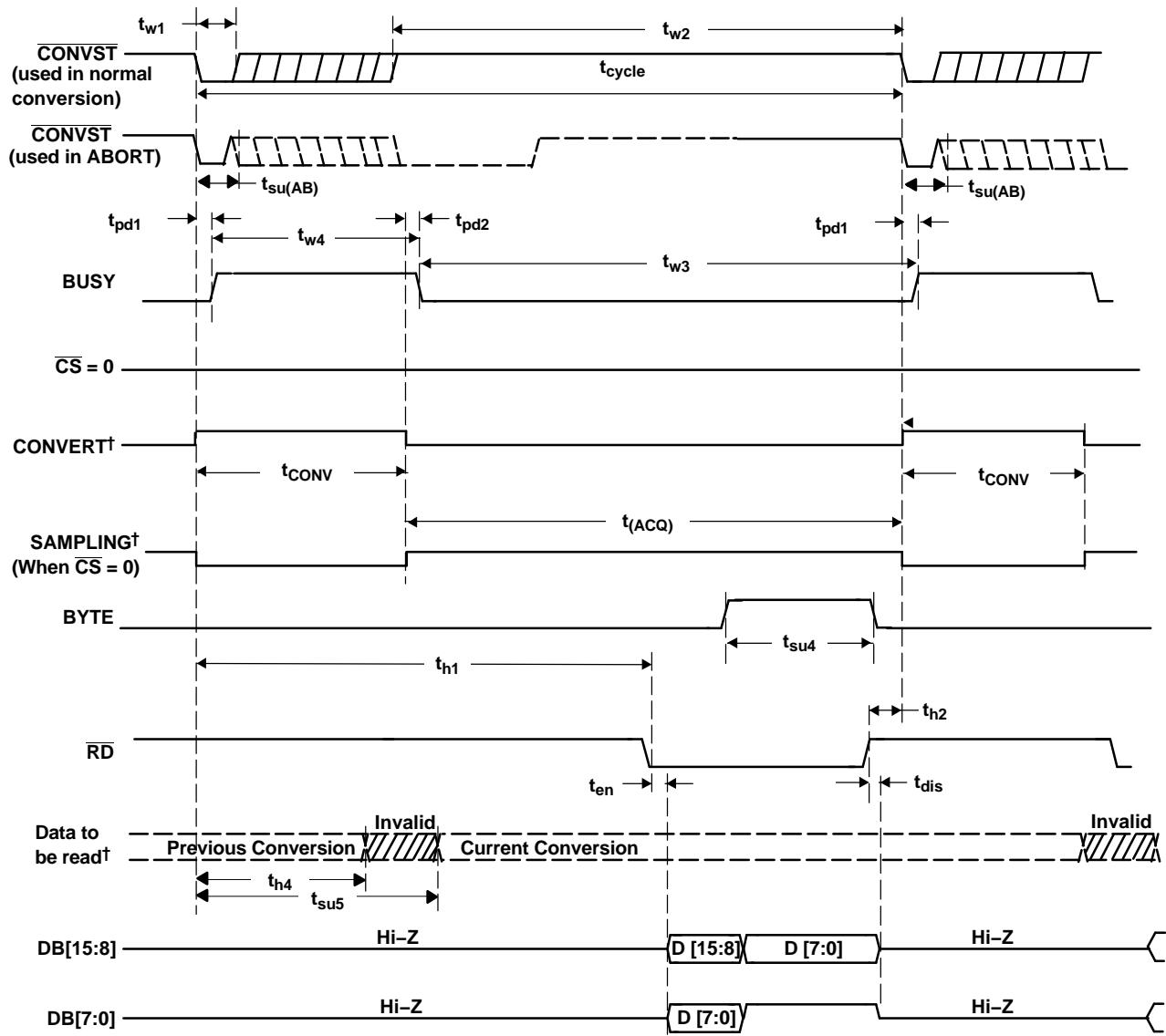
†Signal internal to device

Figure 1. Timing for Conversion and Acquisition Cycles With \overline{CS} and \overline{RD} Toggling

TIMING DIAGRAMS (continued)

Figure 2. Timing for Conversion and Acquisition Cycles With \overline{CS} Toggling, \overline{RD} Tied to BDGND

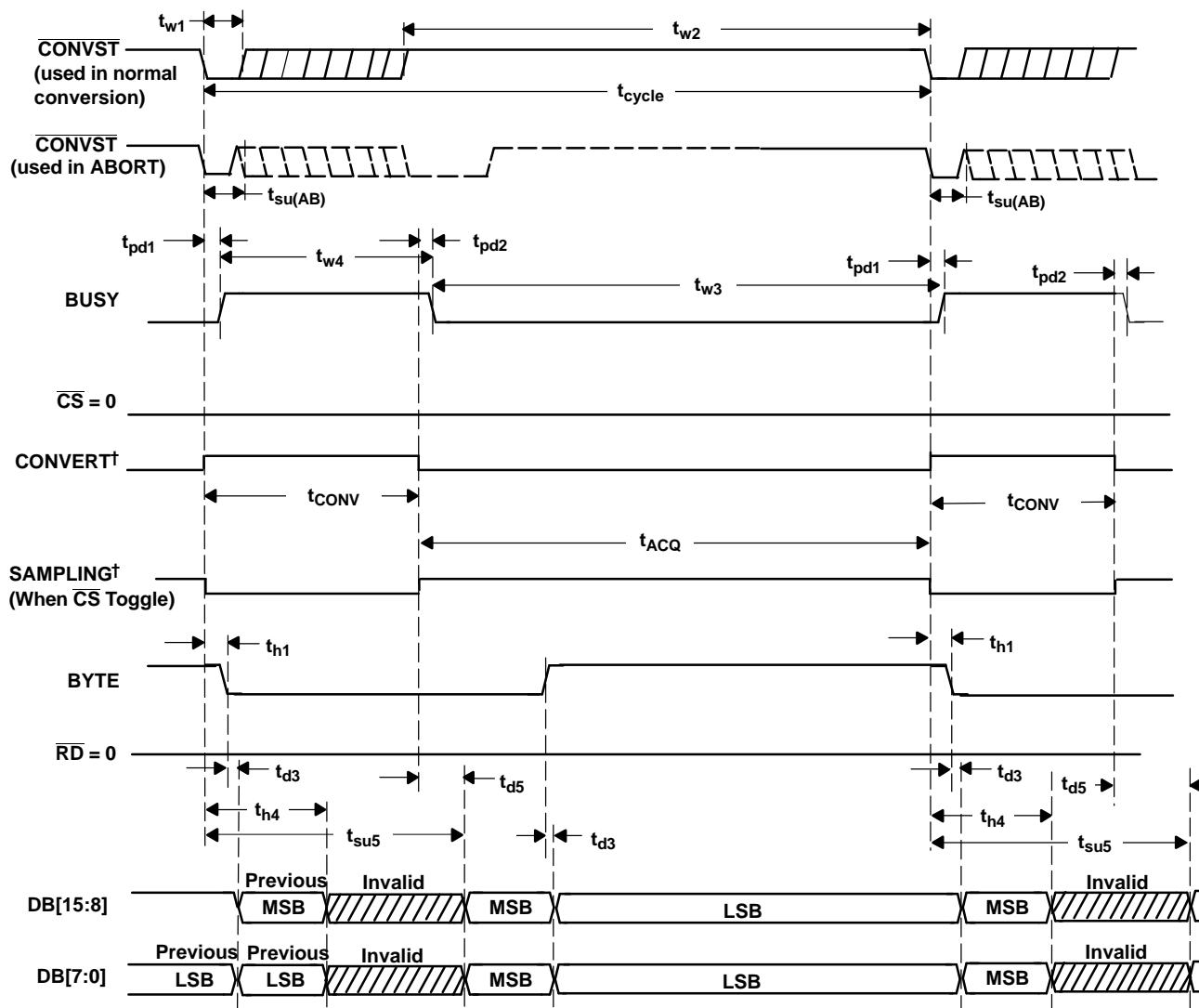
TIMING DIAGRAMS (continued)



†Signal internal to device

Figure 3. Timing for Conversion and Acquisition Cycles With **CS** Tied to **BDGND**, **RD** Toggling

TIMING DIAGRAMS (continued)



†Signal internal to device

Figure 4. Timing for Conversion and Acquisition Cycles With \overline{CS} and \overline{RD} Tied to BDGND—Auto Read

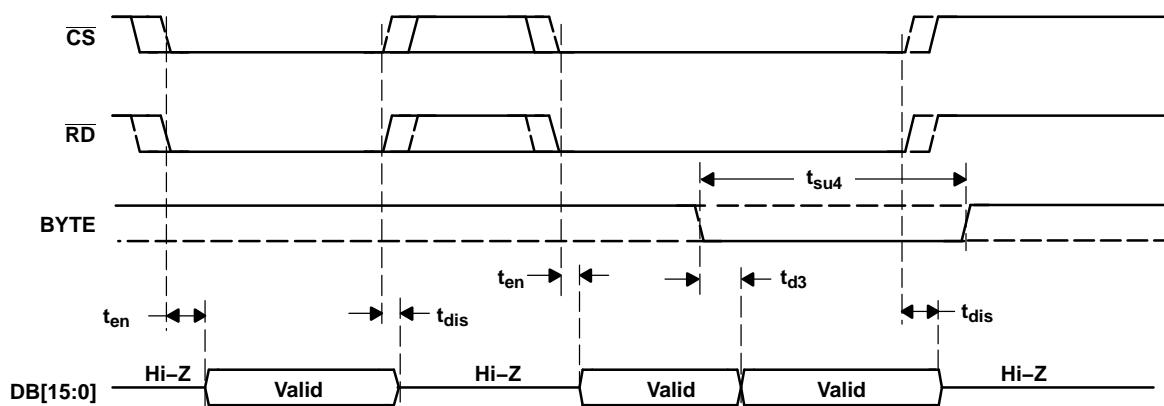


Figure 5. Detailed Timing for Read Cycles

TYPICAL CHARACTERISTICS

At -40°C to 85°C , $+\text{VA} = 5 \text{ V}$, $+\text{VBD} = 5 \text{ V}$, $\text{REFIN} = 4.096 \text{ V}$ (internal reference used) and $f_{\text{sample}} = 1.25 \text{ MHz}$ (unless otherwise noted)

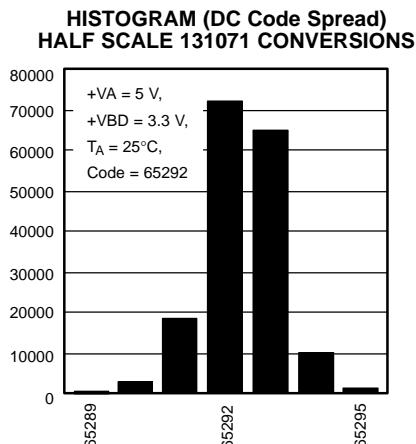


Figure 6.

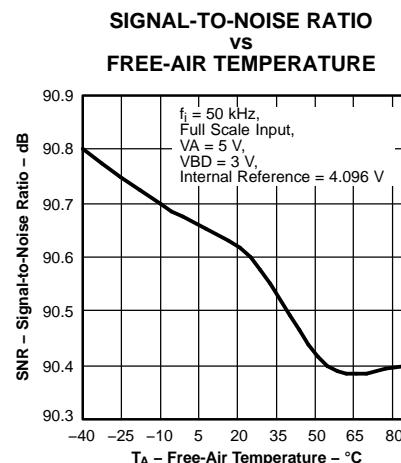


Figure 7.

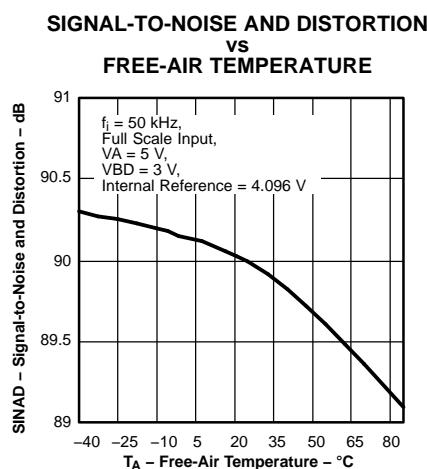


Figure 8.

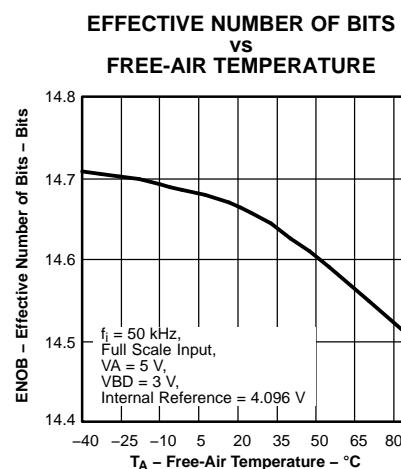


Figure 9.

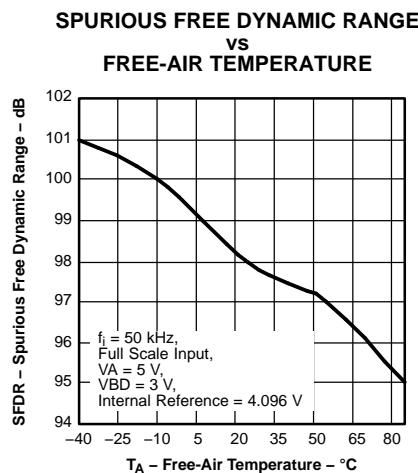
TYPICAL CHARACTERISTICS (continued)


Figure 10.

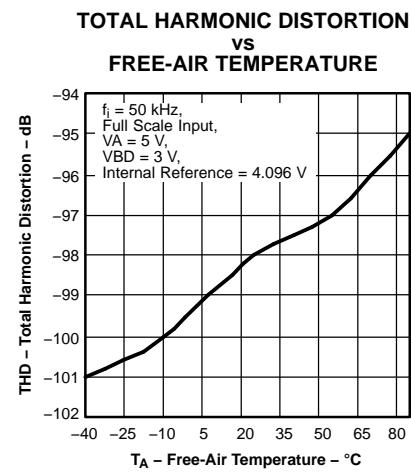


Figure 11.

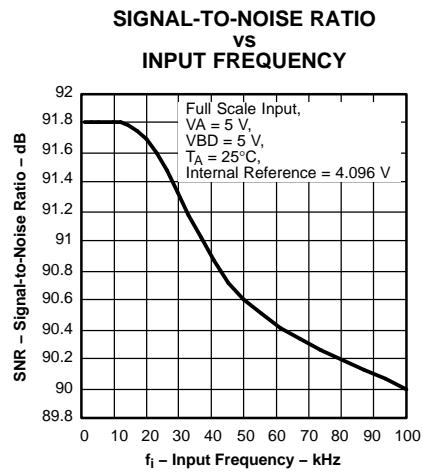


Figure 12.

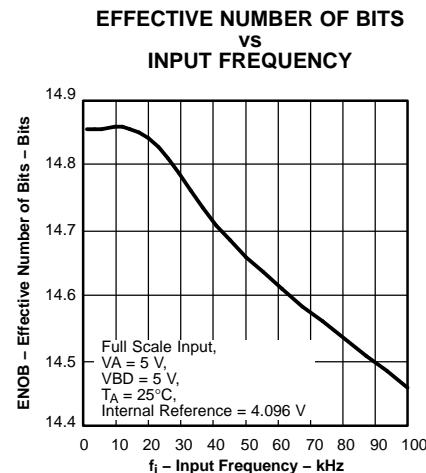


Figure 13.

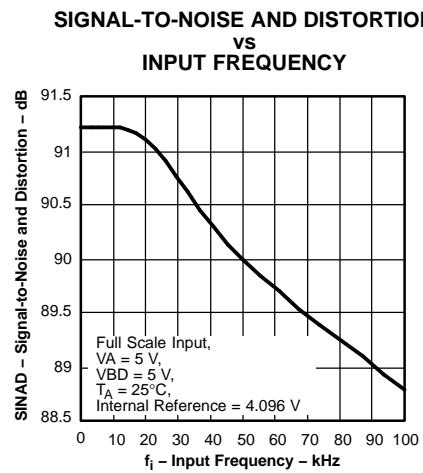


Figure 14.

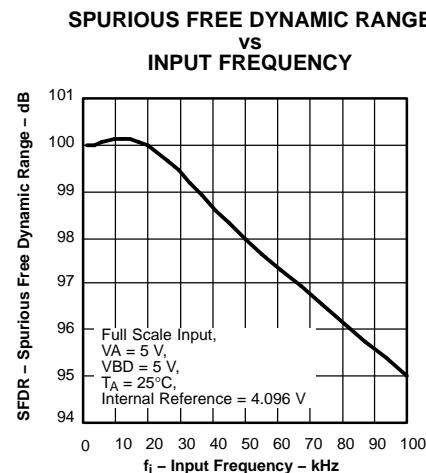


Figure 15.

TYPICAL CHARACTERISTICS (continued)

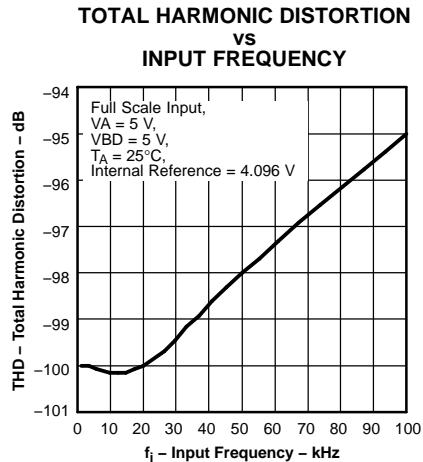


Figure 16.

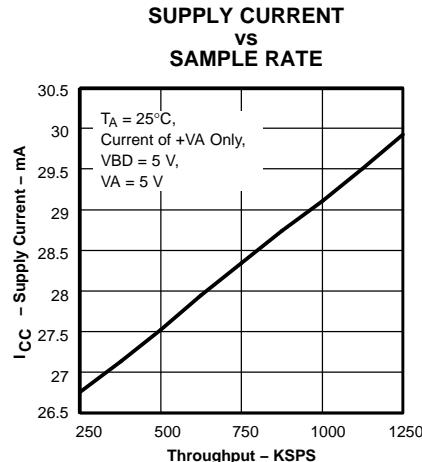


Figure 17.

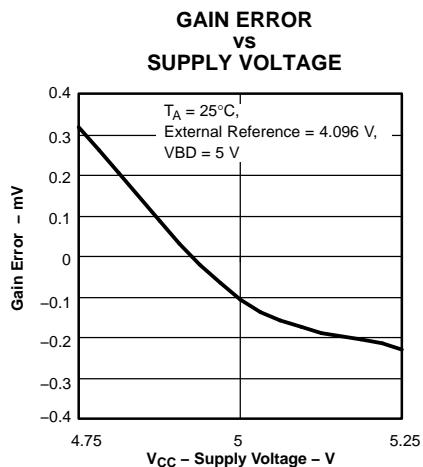


Figure 18.

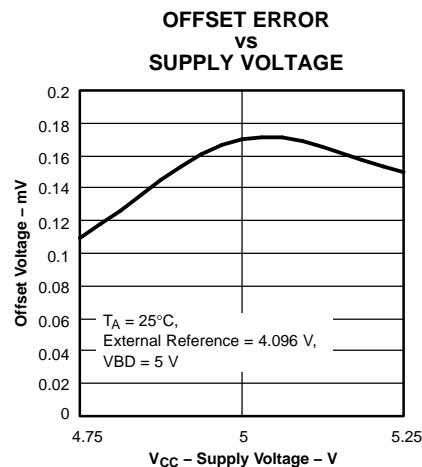


Figure 19.

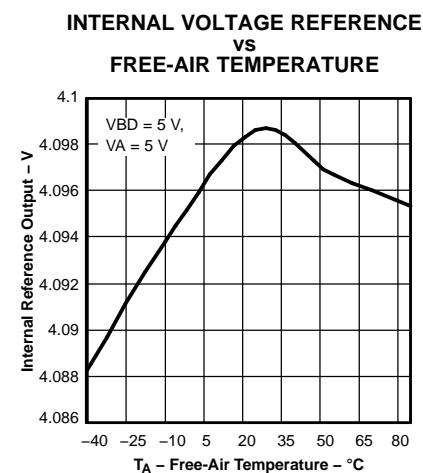


Figure 20.

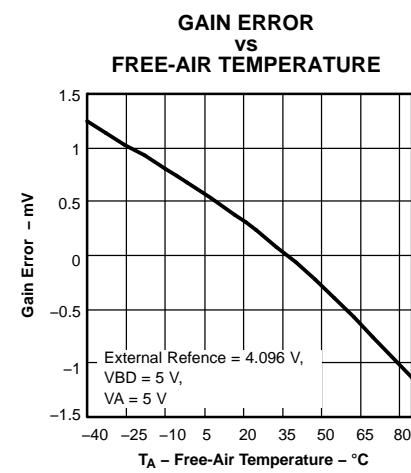


Figure 21.

TYPICAL CHARACTERISTICS (continued)

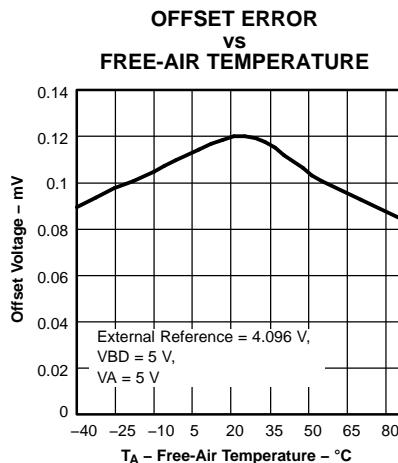


Figure 22.

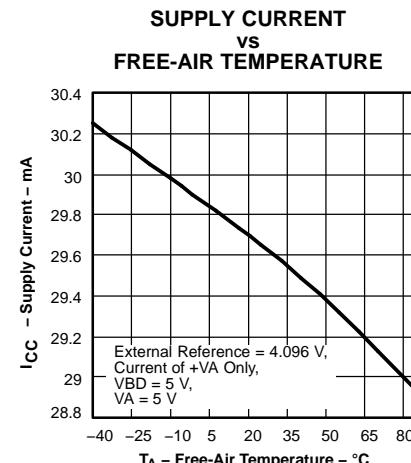


Figure 23.

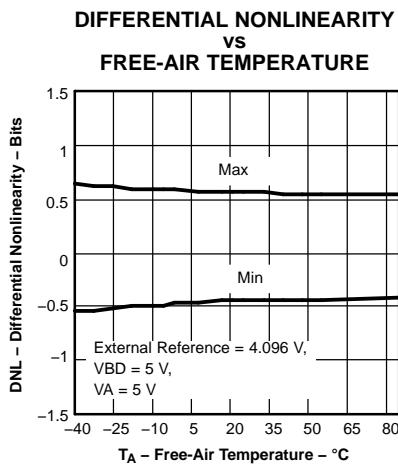


Figure 24.

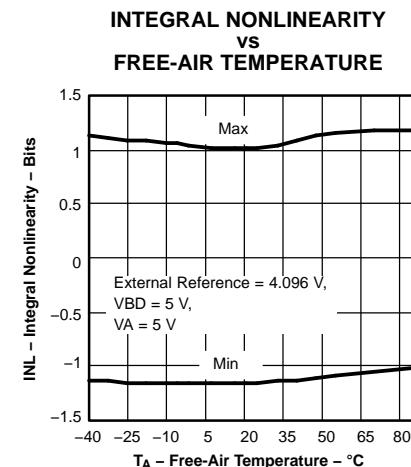


Figure 25.

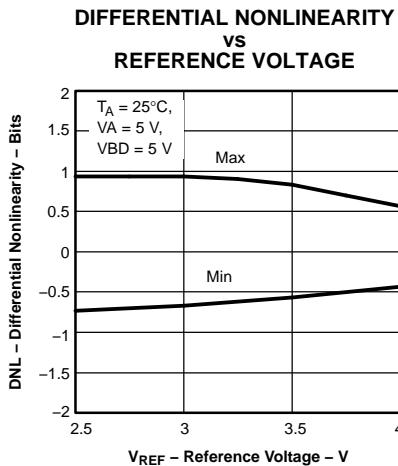


Figure 26.

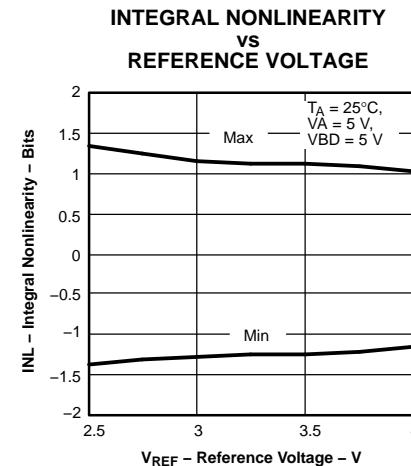


Figure 27.

TYPICAL CHARACTERISTICS (continued)

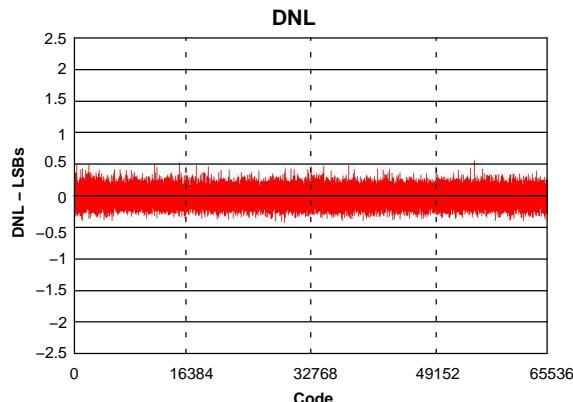


Figure 28.

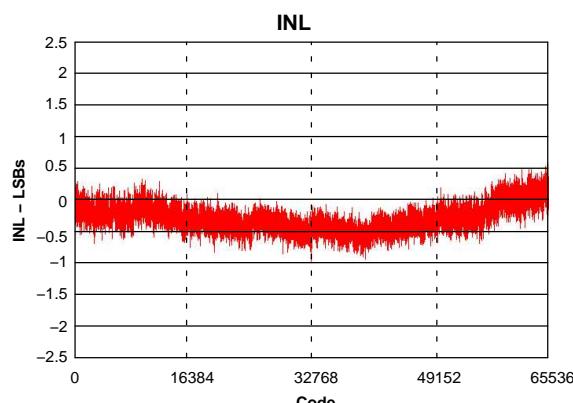


Figure 29.

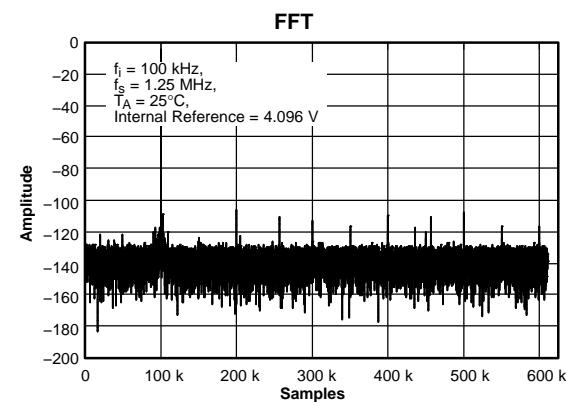


Figure 30.

APPLICATION INFORMATION

MICROCONTROLLER INTERFACING

ADS8406 to 8-Bit Microcontroller Interface

Figure 31 shows a parallel interface between the ADS8406 and a typical microcontroller using the 8-bit data bus. The BUSY signal is used as a falling-edge interrupt to the microcontroller.

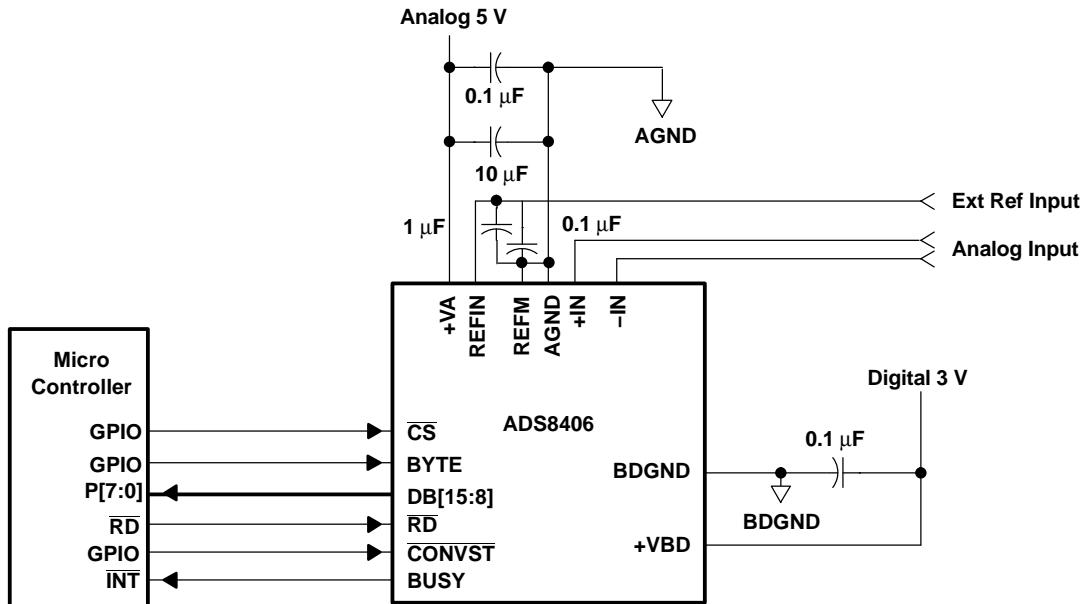


Figure 31. ADS8406 Application Circuitry (using external reference)

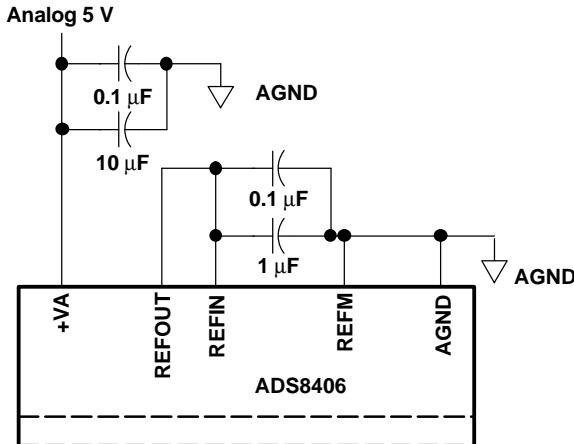


Figure 32. Use Internal Reference

PRINCIPLES OF OPERATION

The ADS8406 is a high-speed successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on charge redistribution, which inherently includes a sample/hold function. See Figure 31 for the application circuit for the ADS8406.

The conversion clock is generated internally. The conversion time of 650 ns is capable of sustaining a 1.25-MHz throughput.

PRINCIPLES OF OPERATION (continued)

The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

REFERENCE

The ADS8406 can operate with an external reference with a range from 2.5 V to 4.2 V. A 4.096-V internal reference is included. When internal reference is used, pin 2 (REFOUT) should be connected to pin 1 (REFIN) with a 0.1- μ F decoupling capacitor and 1- μ F storage capacitor between pin 2 (REFOUT) and pins 47 and 48 (REFM) (see Figure 33). The internal reference of the converter is double buffered. If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the capacitors of the CDAC during conversion. Pin 2 (REFOUT) can be left unconnected (floating) if external reference is used.

ANALOG INPUT

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. Both +IN and –IN inputs have a range of –0.2 V to V_{ref} + 0.2 V. The input span (+IN – (–IN)) is limited to $-V_{ref}$ to V_{ref} .

The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8406 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (25 pF) to an 16-bit settling level within the acquisition time (150 ns) of the device. When the converter goes into the hold mode, the input impedance is greater than 1 G Ω .

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the +IN and –IN inputs and the span (+IN – (–IN)) should be within the limits specified. Outside of these ranges, the converter's linearity may not meet specifications. To minimize noise, low bandwidth input signals with low-pass filters should be used.

Care should be taken to ensure that the output impedance of the sources driving +IN and –IN inputs are matched. If this is not observed, the two inputs could have different settling time. This may result in offset error, gain error and linearity error which varies with temperature and input voltage.

A typical input circuit using TI's THS4503 is shown in Figure 33. Input from a single-ended source may be converted into a differential signal for the ADS8406 as shown in the figure. In case the source itself is differential, then the THS4503 may be used in differential input and differential output modes.

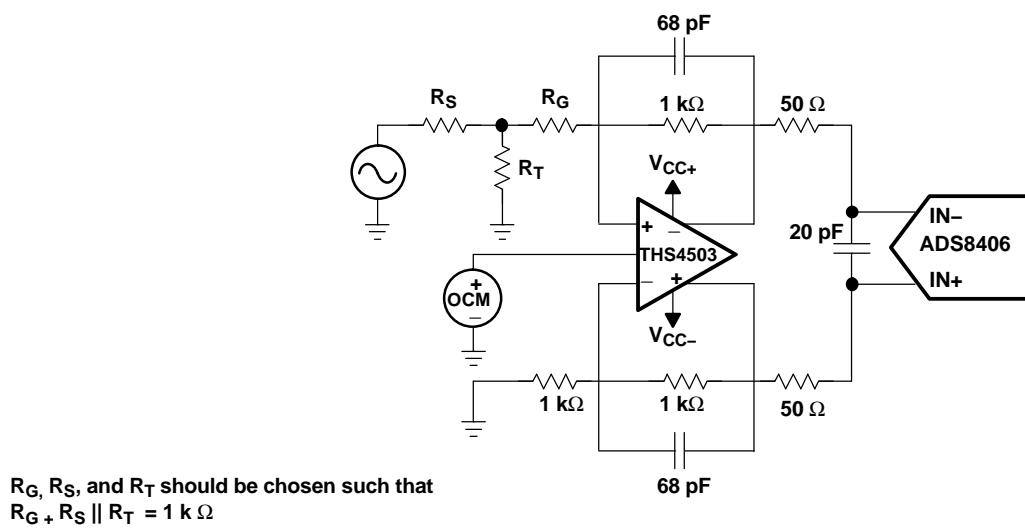


Figure 33. Using the THS4503 With the ADS8406

PRINCIPLES OF OPERATION (continued)

DIGITAL INTERFACE

Timing And Control

See the timing diagrams in the specifications section for detailed information on timing signals and their requirements.

The ADS8406 uses an internal oscillator generated clock which controls the conversion rate and in turn the throughput of the converter. No external clock input is required.

Conversions are initiated by bringing the CONVST pin low for a minimum of 20 ns (after the 20 ns minimum requirement has been met, the CONVST pin can be brought high), while CS is low. The ADS8406 switches from the sample to the hold mode on the falling edge of the CONVST command. A clean and low jitter falling edge of this signal is important to the performance of the converter. The BUSY output is brought high after CONVST goes low. BUSY stays high throughout the conversion process and returns low when the conversion has ended.

Sampling starts as soon as the conversion is over when CS is tied low or starts with the falling edge of CS when BUSY is low.

Both RD and CS can be high during and before a conversion with one exception (CS must be low when CONVST goes low to initiate a conversion). Both the RD and CS pins are brought low in order to enable the parallel output bus with the conversion.

Reading Data

The ADS8406 outputs full parallel data in two's complement format as shown in Table 1. The parallel output is active when CS and RD are both low. There is a minimal quiet zone requirement around the falling edge of CONVST. This is 50 ns prior to the falling edge of CONVST and 40 ns after the falling edge. No data read should be attempted within this zone. Any other combination of CS and RD sets the parallel output to 3-state. BYTE is used for multiword read operations. BYTE is used whenever lower bits of the converter result are output on the higher byte of the bus. Refer to Table 1 for ideal output codes.

Table 1. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT	
		2'S COMPLEMENT	
Full scale range	$2(+V_{ref})$		
Least significant bit (LSB)	$2(+V_{ref})/65536$		
+Full scale	$(+V_{ref}) - 1$ LSB	0111 1111 1111 1111	7FFF
Midscale	0 V	0000 0000 0000 0000	0000
Midscale - 1 LSB	0 V - 1 LSB	1111 1111 1111 1111	FFFF
- Full scale	$(-V_{ref})$	1000 0000 0000 0000	8000

The output data is a full 16-bit word (D15–D0) on DB15–DB0 pins (MSB–LSB) if BYTE is low.

The result may also be read on an 8-bit bus for convenience. This is done by using only pins DB15–DB8. In this case two reads are necessary: the first as before, leaving BYTE low and reading the 8 most significant bits on pins DB15–DB8, then bringing BYTE high. When BYTE is high, the low bits (D7–D0) appear on pins DB15–D8.

These multiword read operations can be done with multiple active RD (toggling) or with RD tied low for simplicity.

Conversion Data Readout

BYTE	DATA READ OUT	
	DB15–DB8 Pins	DB7–DB0 Pins
High	D7–D0	All one's
Low	D15–D8	D7–D0

RESET

RESET is an asynchronous active low input signal (that works independently of \overline{CS}). Minimum \overline{RESET} low time is 25 ns. Current conversion will be aborted no later than 50 ns after the converter is in the reset mode. In addition, all output latches are cleared (set to zero's) after \overline{RESET} . The converter goes back to normal operation mode no later than 20 ns after \overline{RESET} input is brought high.

The converter starts the first sampling period 20 ns after the rising edge of \overline{RESET} . Any sampling period except for the one immediately after a \overline{RESET} is started with the falling edge of the previous BUSY signal or the falling edge of CS , whichever is later.

Another way to reset the device is through the use of the combination of \overline{CS} and \overline{CONVST} . This is useful when the dedicated \overline{RESET} pin is tied to the system reset but there is a need to abort only the conversion in a specific converter. Since the BUSY signal is held high during the conversion, either one of these conditions triggers an internal self-clear reset to the converter just the same as a reset via the dedicated \overline{RESET} pin. The reset does not have to be cleared as for the dedicated \overline{RESET} pin. A reset can be started with either of the two following steps.

- Issue a \overline{CONVST} when \overline{CS} is low and a conversion is in progress. The falling edge of \overline{CONVST} must satisfy the timing as specified by the timing parameter $t_{su(AB)}$ mentioned in the timing characteristics table to ensure a reset. The falling edge of \overline{CONVST} starts a reset. Timing is the same as a reset using the dedicated \overline{RESET} pin except the instance of the falling edge is replaced by the falling edge of \overline{CONVST} .
- Issue a \overline{CS} while a conversion is in progress. The falling edge of \overline{CS} must satisfy the timing as specified by the timing parameter $t_{su(AB)}$ mentioned in the timing characteristics table to ensure a reset. The falling edge of \overline{CS} causes a reset. Timing is the same as a reset using the dedicated \overline{RESET} pin except the instance of the falling edge is replaced by the falling edge of \overline{CS} .

POWER-ON INITIALIZATION

\overline{RESET} is not required after power on. An internal power-on-reset circuit generates the reset. To ensure that all of the registers are cleared, the three conversion cycles must be given to the converter after power on.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8406 circuitry.

As the ADS8406 offers single-supply operation, it is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are at least n windows in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event.

On average, the ADS8406 draws very little current from an external reference, as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1- μ F bypass capacitor and a 1- μ F storage capacitor are recommended from pin 1 (REFIN) directly to pin 48 (REFM). REFM and AGND should be shorted on the same ground plane under the device.

The AGND and BDGND pins should be connected to a clean ground point. In all cases, this should be the analog ground. Avoid connections which are close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

As with the AGND connections, +VA should be connected to a 5-V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. Power to the ADS8406 should be clean and well bypassed. A 0.1- μ F ceramic bypass capacitor should be placed as close to the device as possible. See Table 2 for the placement of the capacitor. In addition, a 1- μ F to 10- μ F capacitor is recommended. In some situations, additional bypassing may be required, such as a 100- μ F electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5-V supply, removing the high frequency noise.

Table 2. Power Supply Decoupling Capacitor Placement

POWER SUPPLY PLANE SUPPLY PINS	CONVERTER ANALOG SIDE	CONVERTER DIGITAL SIDE
Pin pairs that require shortest path to decoupling capacitors	(4,5), (8,9), (10,11), (13,15), (43,44), (45,46)	(24,25), (34, 35)
Pins that require no decoupling	12, 14	37

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS8406IBPFBR	Active	Production	TQFP (PFB) 48	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8406I B
ADS8406IBPFBR.B	Active	Production	TQFP (PFB) 48	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8406I B
ADS8406IBPFBT	Active	Production	TQFP (PFB) 48	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS8406I B
ADS8406IBPFBT.B	Active	Production	TQFP (PFB) 48	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS8406I B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a " ~ " will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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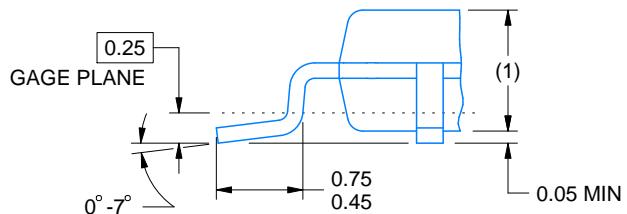
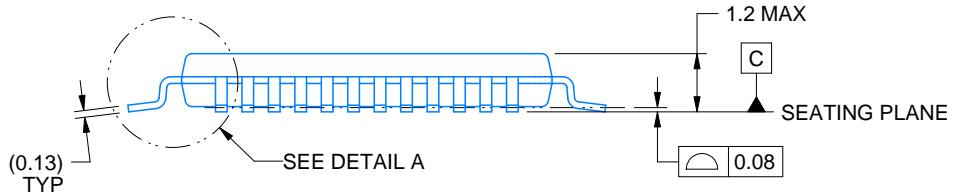
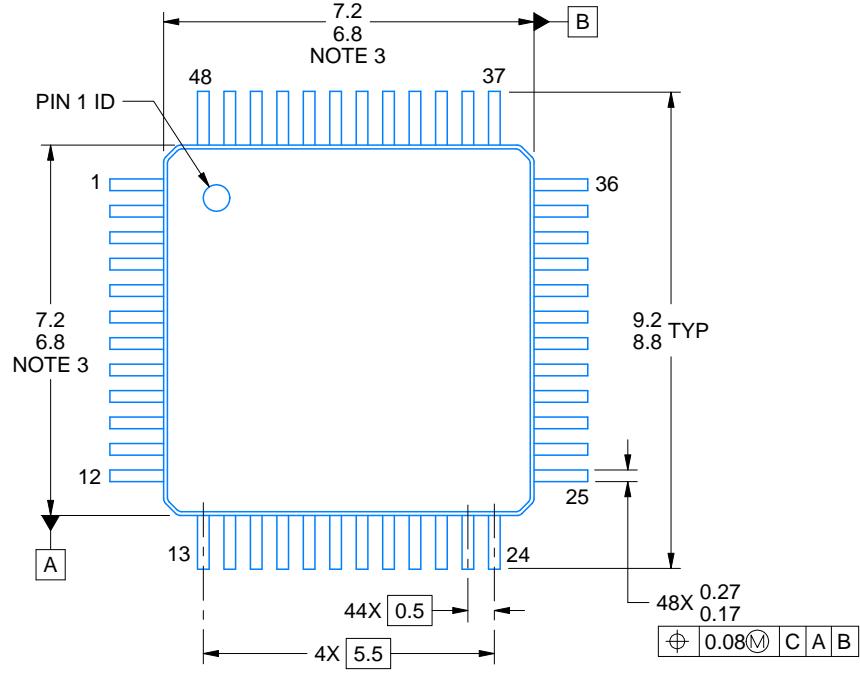
PFB0048A



PACKAGE OUTLINE

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



DETAIL A
TYPICAL

4215157/A 03/2024

NOTES:

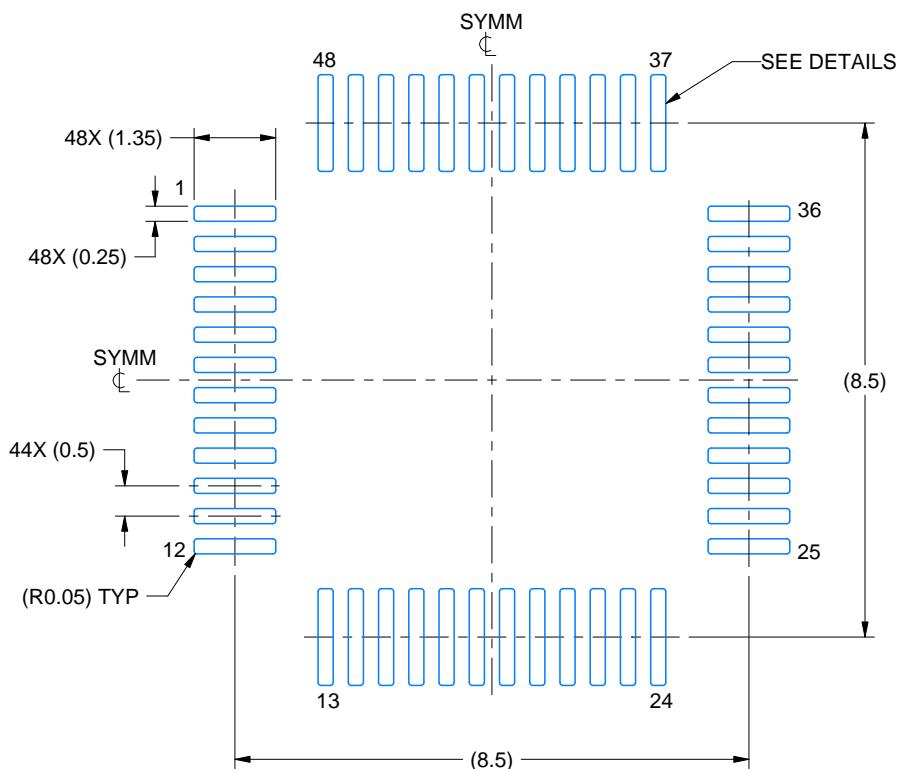
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

PFB0048A

TQFP - 1.2 mm max height

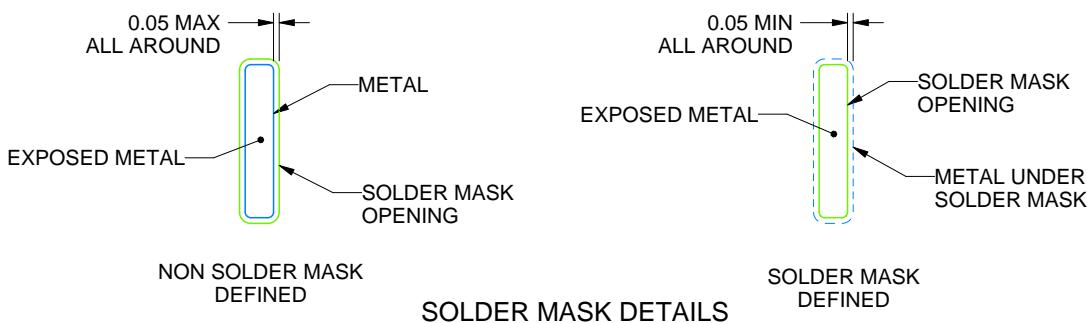
PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE:8X



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NOTES: (continued)

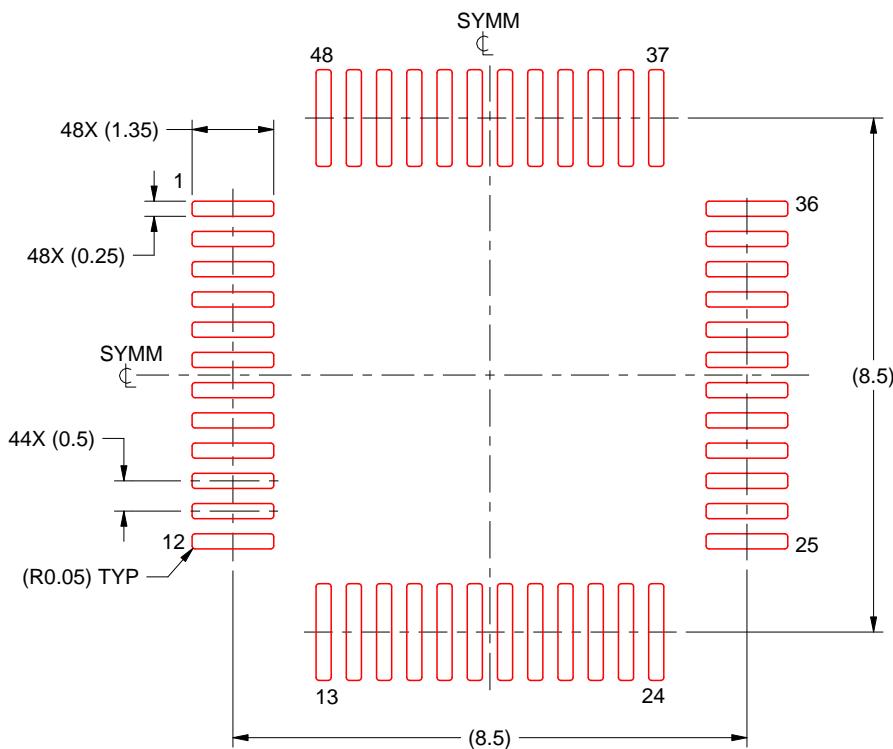
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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