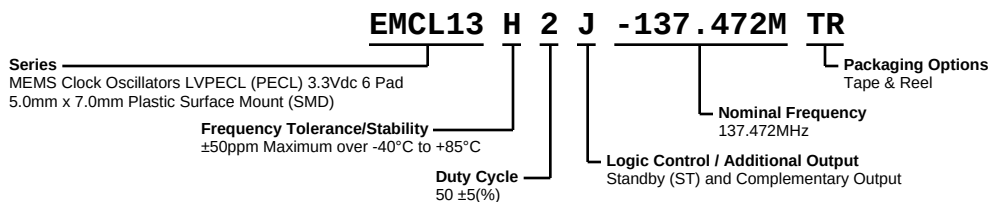


EMCL13H2J-137.472M TR



ELECTRICAL SPECIFICATIONS

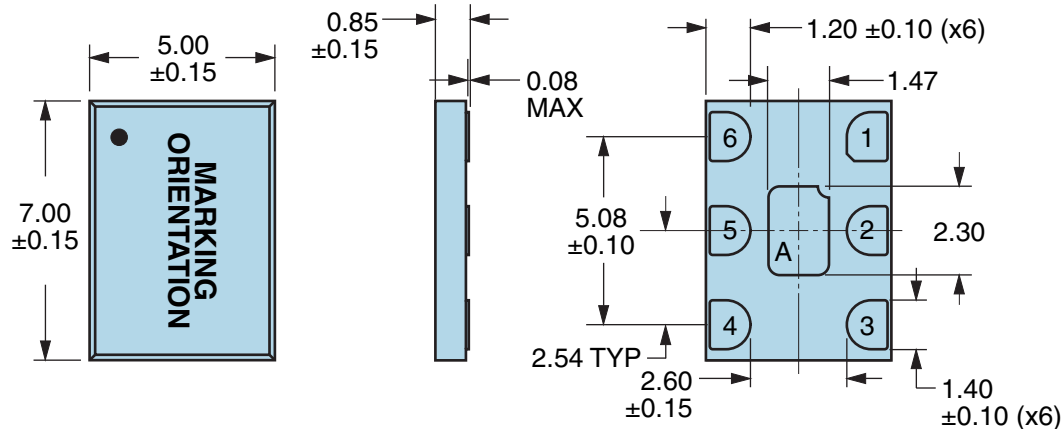
Nominal Frequency	137.472MHz
Frequency Tolerance/Stability	$\pm 50\text{ppm}$ Maximum over -40°C to $+85^{\circ}\text{C}$ (Inclusive of all conditions: Calibration Tolerance at 25°C , Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C , Reflow, Shock, and Vibration)
Aging at 25°C	$\pm 1\text{ppm}$ First Year Maximum
Supply Voltage	$+3.3\text{Vdc} \pm 0.3\text{Vdc}$
Input Current	80mA Maximum (Excluding Load Termination Current)
Output Voltage Logic High (Voh)	Vdd-1.10Vdc Minimum, 2.40Vdc Typical, Vdd-0.70Vdc Maximum
Output Voltage Logic Low (Vol)	Vdd-2.0Vdc Minimum, 1.60Vdc Typical, Vdd-1.40Vdc Maximum
Rise/Fall Time	150pSec Typical, 300pSec Maximum (Measured over 20% to 80% of waveform)
Duty Cycle	$50 \pm 5(\%)$ (Measured at 50% of waveform)
Output Swing (VOpp)	600mVdc Minimum, 800mVdc Typical, 1000mVdc Maximum
Load Drive Capability	50 Ohms into Vdd-2.0Vdc
Output Logic Type	LVPECL
Logic Control / Additional Output	Standby (ST) and Complementary Output
Output Control Input Voltage	Vih of 70% of Vdd Minimum or No Connect to Enable Output and Complementary Output, Vil of 30% of Vdd Maximum to Disable Output and Complementary Output (High Impedance)
Standby Current	30 μA Maximum (Without Load)
Period Jitter (Deterministic)	0.2pSec Typical
Period Jitter (Random)	2.0pSec Typical
Period Jitter (RMS)	1.5pSec Typical, 3.0pSec Maximum
Period Jitter (pk-pk)	20pSec Typical, 25pSec Maximum
RMS Phase Jitter (Fj = 637kHz to 10MHz; Random)	1.6pSec Typical
RMS Phase Jitter (Fj = 1MHz to 20MHz; Random)	1.0pSec Typical
RMS Phase Jitter (Fj = 1.875MHz to 20MHz; Random)	0.5pSec Typical
Start Up Time	10mSec Maximum
Storage Temperature Range	-55°C to $+125^{\circ}\text{C}$

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

ESD Susceptibility	MIL-STD-883, Method 3015, Class 2, HBM 2000V
Flammability	UL94-V0
Mechanical Shock	MIL-STD-883, Method 2002, Condition G, 30,000G
Moisture Resistance	MIL-STD-883, Method 1004
Moisture Sensitivity Level	J-STD-020, MSL 1
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003 (Six I/O Pads on bottom of package only)
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Thermal Shock	MIL-STD-883, Method 1011, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A, 20G

EMCL13H2J-137.472M TR

MECHANICAL DIMENSIONS (all dimensions in millimeters)



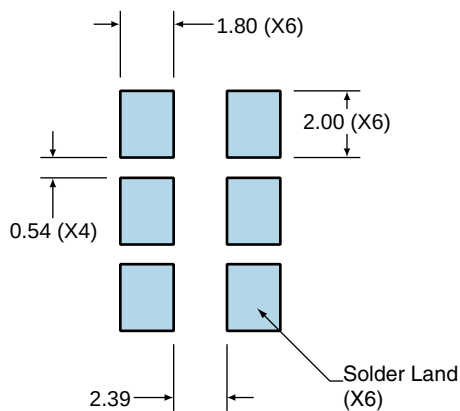
PIN	CONNECTION
1	Standby (ST)
2	No Connect
3	Case Ground
4	Output
5	Complementary Output
6	Supply Voltage

LINE	MARKING
1	XXXX or XXXXX XXXX or XXXXX=Ecliptek Manufacturing Identifier

Note A: Center paddle is connected internally to oscillator ground (Pad 3).

Suggested Solder Pad Layout

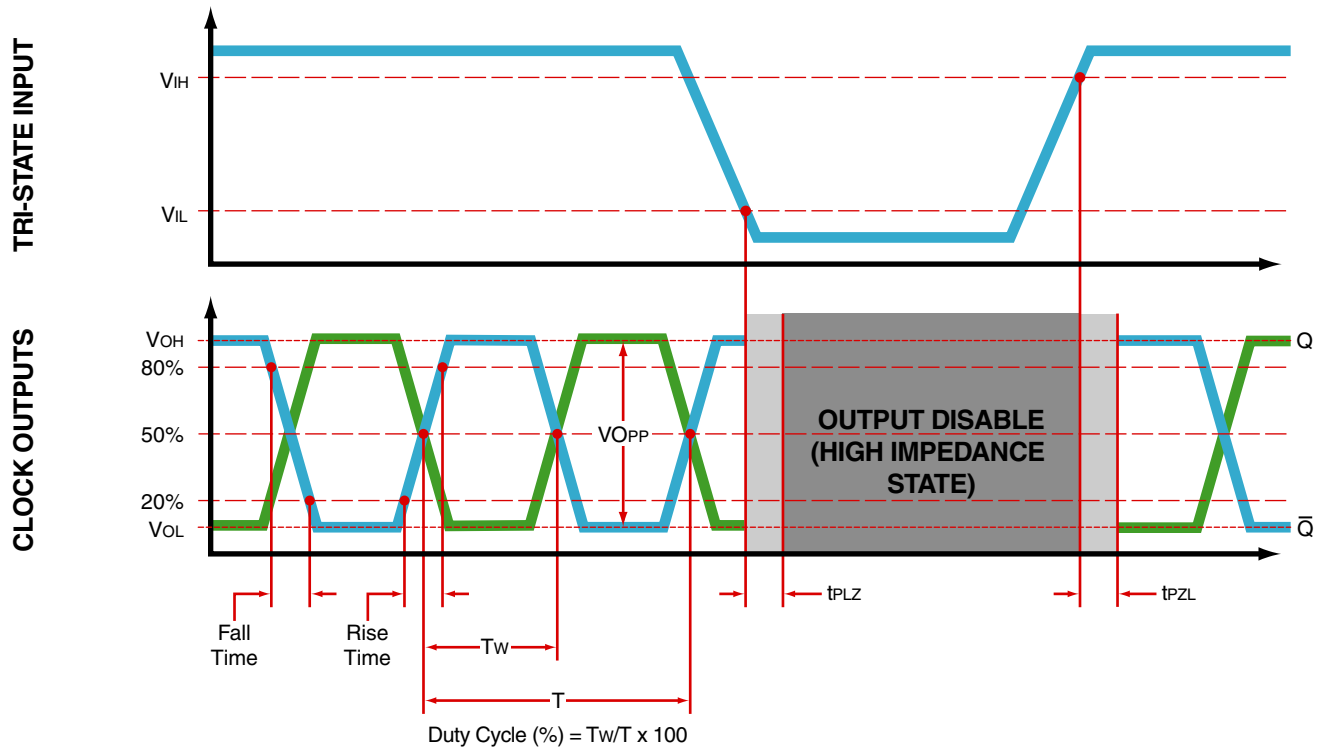
All Dimensions in Millimeters



All Tolerances are ± 0.1

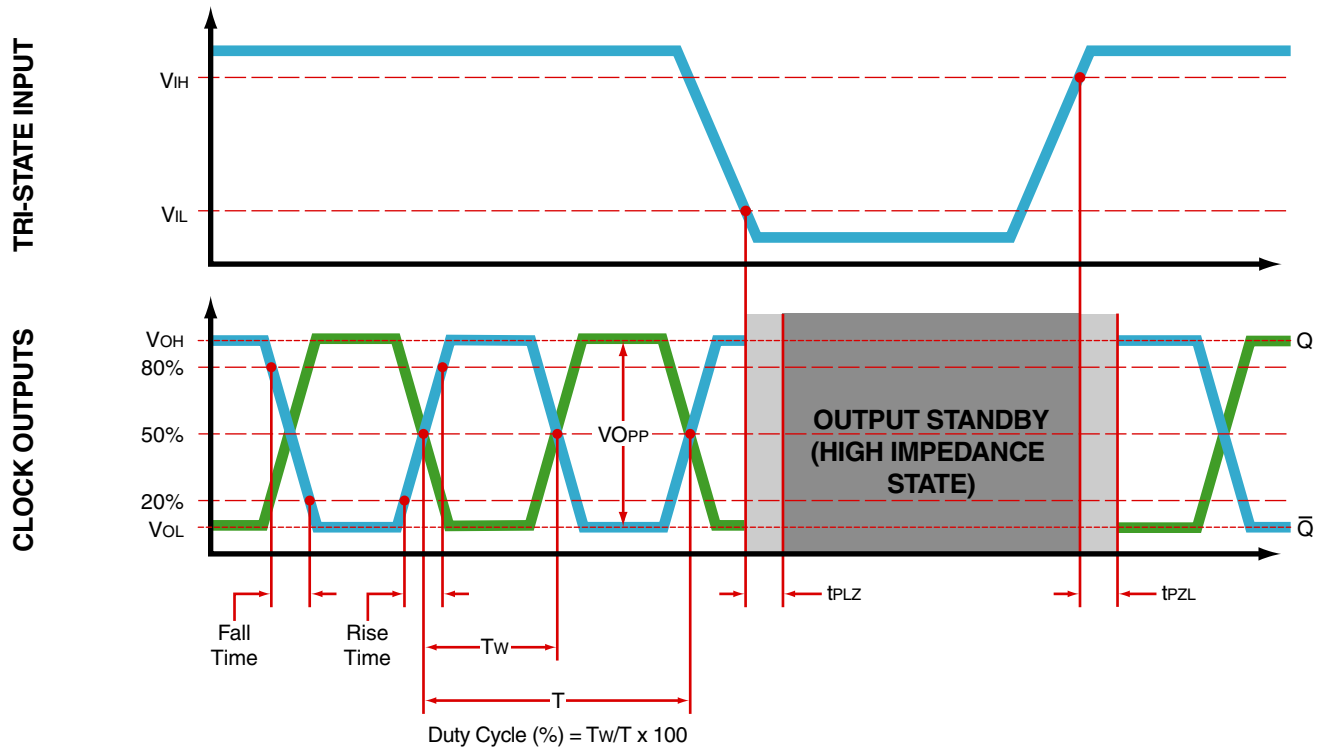
EMCL13H2J-137.472M TR

OUTPUT WAVEFORM & TIMING DIAGRAM



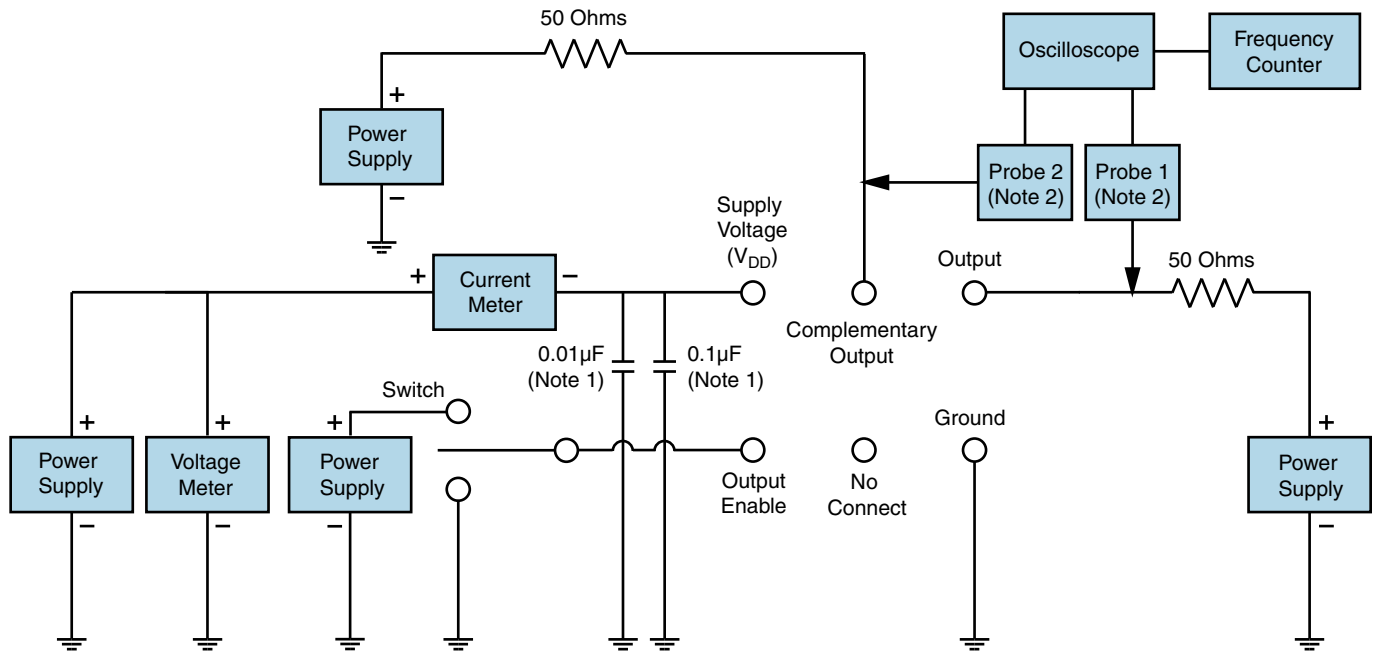
EMCL13H2J-137.472M TR

OUTPUT WAVEFORM & TIMING DIAGRAM



EMCL13H2J-137.472M TR

Test Circuit for Output Enable and Complementary Output



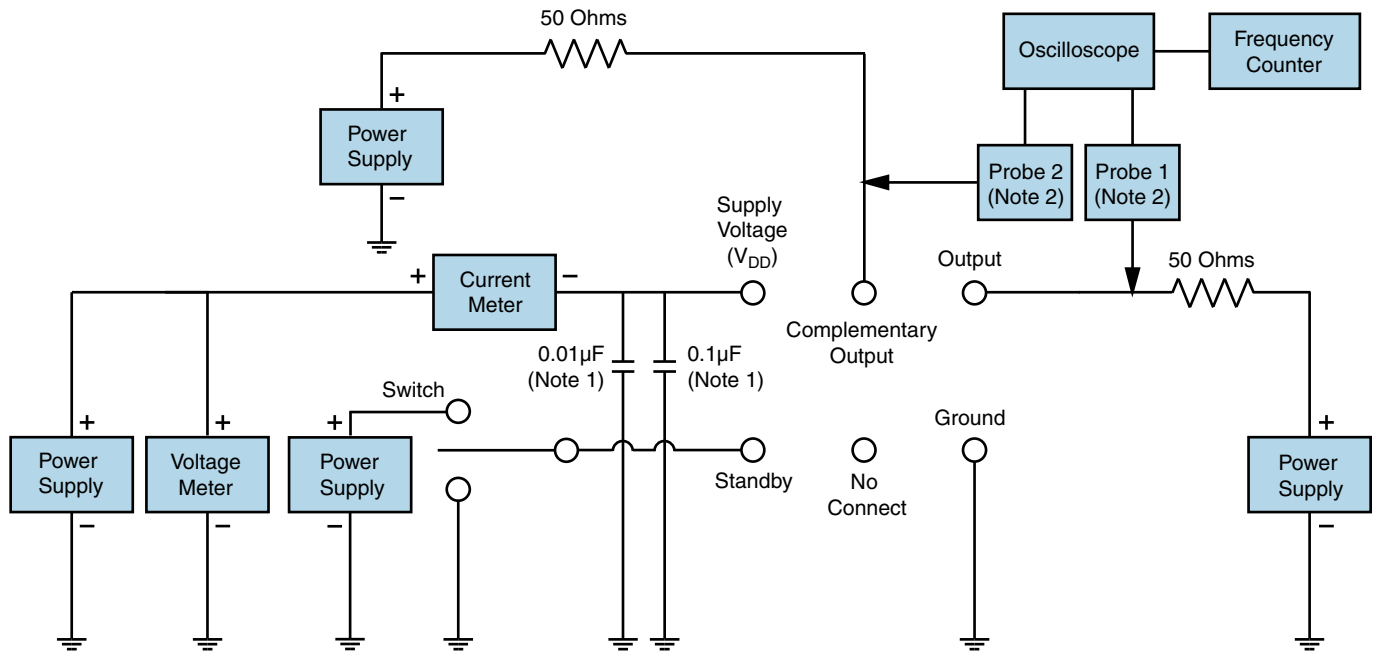
Note 1: An external $0.01\mu\text{F}$ ceramic bypass capacitor in parallel with a $0.1\mu\text{F}$ high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

Note 2: A low capacitance ($<12\text{pF}$), 10X attenuation factor, high impedance ($>10\text{Mohms}$), and high bandwidth ($>500\text{MHz}$) passive probe is recommended.

Note 3: Test circuit PCB traces need to be designed for a characteristic line impedance of 50 ohms.

EMCL13H2J-137.472M TR

Test Circuit for Standby and Complementary Output



Note 1: An external $0.01\mu\text{F}$ ceramic bypass capacitor in parallel with a $0.1\mu\text{F}$ high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

Note 2: A low capacitance ($<12\text{pF}$), 10X attenuation factor, high impedance ($>10\text{Mohms}$), and high bandwidth ($>500\text{MHz}$) passive probe is recommended.

Note 3: Test circuit PCB traces need to be designed for a characteristic line impedance of 50 ohms.

1.50 MIN

22.40 MAX

DIA 40 MIN
Access Hole at
Slot Location

360 MAX

2.50 MIN Width
10 MIN Depth
Tape slot in Core
for Tape Start

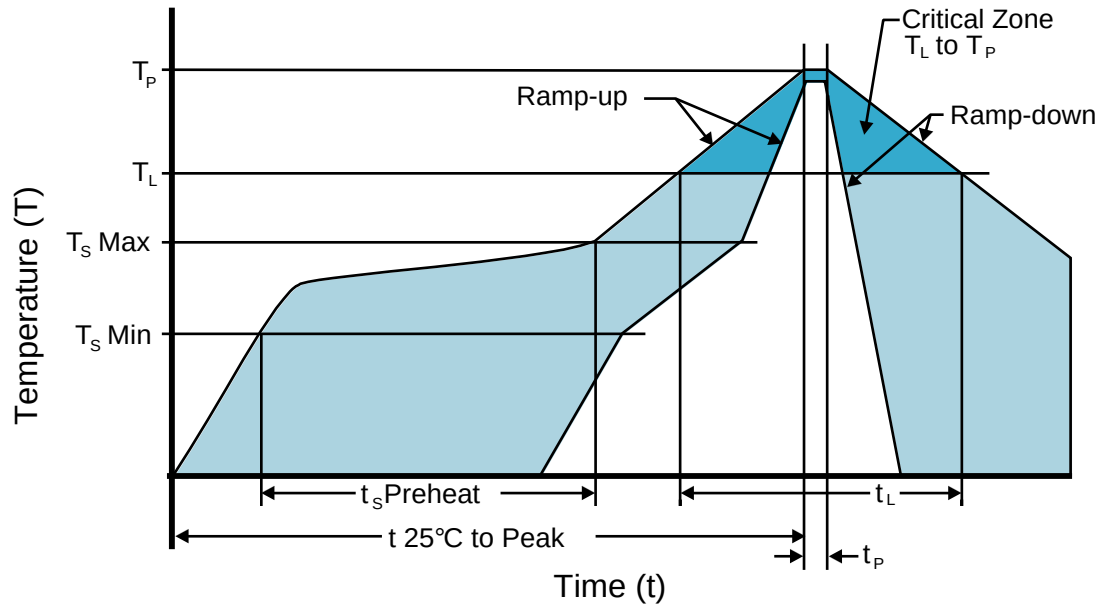
DIA 50 MIN

DIA 20.20 MIN

DIA 13.00 $\pm$ 0.20

16.40 +2.00/-0.00

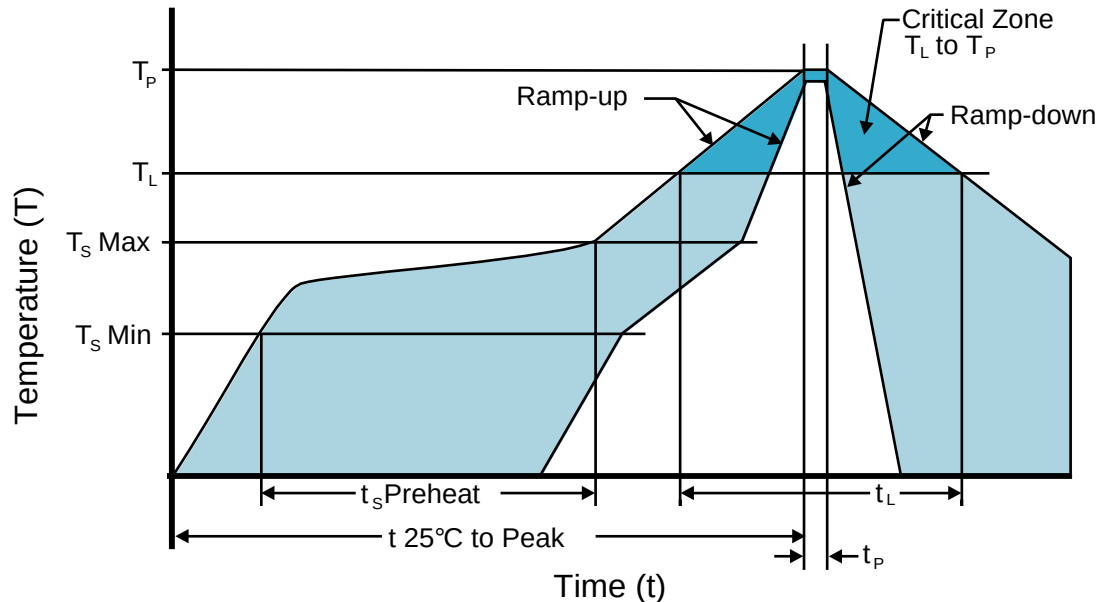
Recommended Solder Reflow Methods



High Temperature Infrared/Convection

T_s MAX to T_L (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (T _s MIN)	150°C
- Temperature Typical (T _s TYP)	175°C
- Temperature Maximum (T _s MAX)	200°C
- Time (t _s MIN)	60 - 180 Seconds
Ramp-up Rate (T_L to T_P)	3°C/second Maximum
Time Maintained Above:	
- Temperature (T _L)	217°C
- Time (t _L)	60 - 150 Seconds
Peak Temperature (T_P)	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature (T_P Target)	250°C +0/-5°C
Time within 5°C of actual peak (t_p)	20 - 40 seconds
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum
Moisture Sensitivity Level	Level 1

Recommended Solder Reflow Methods



Low Temperature Infrared/Convection 240°C

Ts MAX to TL (Ramp-up Rate) 5°C/second Maximum

Preheat

- Temperature Minimum (Ts MIN) N/A
- Temperature Typical (Ts TYP) 150°C
- Temperature Maximum (Ts MAX) N/A
- Time (ts MIN) 60 - 120 Seconds

Ramp-up Rate (TL to Tp) 5°C/second Maximum

Time Maintained Above:

- Temperature (TL) 150°C
- Time (tL) 200 Seconds Maximum

Peak Temperature (Tp) 240°C Maximum

Target Peak Temperature (Tp Target) 240°C Maximum 2 Times / 230°C Maximum 1 Time

Time within 5°C of actual peak (tp) 10 seconds Maximum 2 Times / 80 seconds Maximum 1 Time

Ramp-down Rate 5°C/second Maximum

Time 25°C to Peak Temperature (t) N/A

Moisture Sensitivity Level Level 1

Low Temperature Manual Soldering

185°C Maximum for 10 seconds Maximum, 2 times Maximum.

High Temperature Manual Soldering

260°C Maximum for 5 seconds Maximum, 2 times Maximum.