AN2115
Application note

Designing an application with the L6928, high efficiency monolithic synchronous step-down regulator

Introduction

This application note details the main features and application advantages of the L6928D. After describing how the device works and its main features, a step-by-step design section is provided to aid in the selection of the external components and evaluation of the losses. The performance of the L6928D is expressed in terms of efficiency and thermal results. At the conclusion of this document a few application ideas are provided.

Figure 1. Minimum application board size

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1 Device description

The L6928D is a high efficiency monolithic synchronous step-down regulator capable of delivering up to 800 mA at output voltages from 0.6 V to V_{in} (100% duty cycle). It has been designed using BCDV technology and employs a constant frequency peak current mode as the control loop architecture. The input voltage ranges from 2 V to 5.5 V. Thanks to very low quiescent current (25 µA) and shutdown current (0.2 µA), the device is highly suitable for supplying battery-powered equipment (particularly for those using single lithium-ion cells) such as PDAs and hand-held terminals, DSCs (digital still cameras) and cellular phones. While the switching frequency is internally set at 1.4 MHz, the device can be externally synchronized from 1 MHz to 2 MHz. If this feature is not required, it can operate in low consumption mode (LCM) or low noise mode (LNM), depending on the SYNC pin value. A very low internal reference voltage (0.6 V typ.) allows the device to regulate very low output voltages, in accordance with new microprocessor supply voltage requirements. The very low $R_{DS(on)}$ of the Power MOSFETs ensures high efficiency at high output current. Other beneficial features are UVLO (undervoltage lockout), OVP (overvoltage protection), constant current short circuit protection, PGOOD (power good output) and thermal shutdown. The space saving MSOP8 package, combined with a minimum need for external components, allows for very compact applications.

Figure 2. Minimum size application circuit

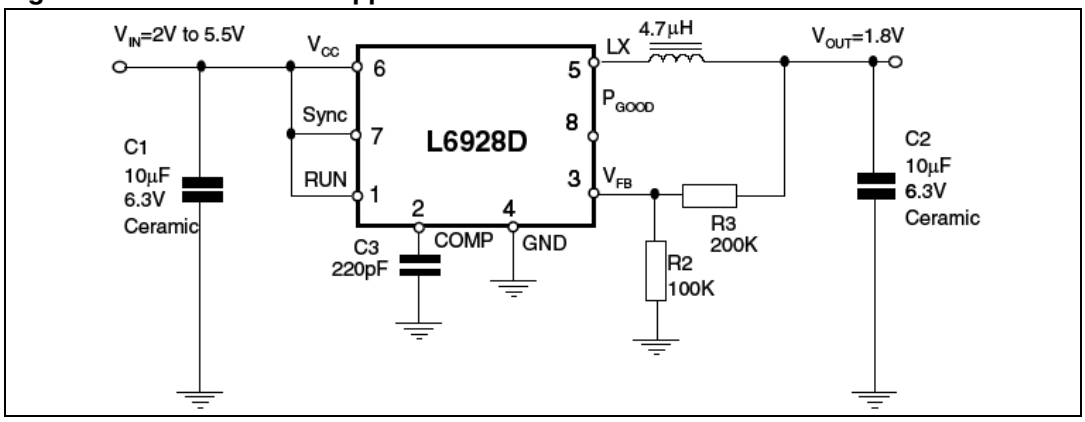


Figure 3. Pin connection

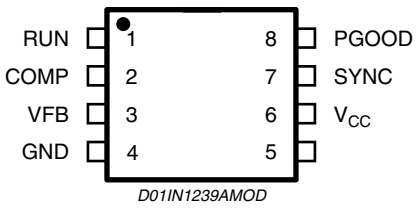
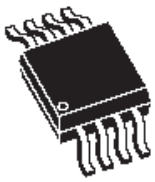


Figure 4. Package



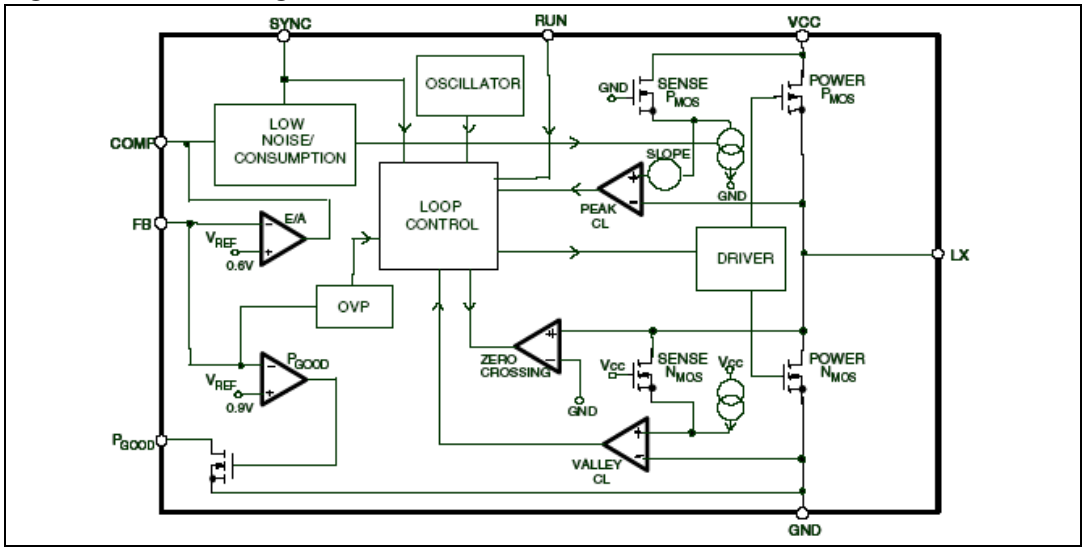
2 Pin function

Table 1. Pin description

N.	Name	Description
1	RUN	Shutdown input. When connected to a low level voltage (less than 0.5 V) the device stops working. When high (above 1.3 V) the device is enabled. This pin must not be left floating.
2	COMP	Error amplifier output. A compensation network must be connected to this pin. Usually a 220 pF capacitor is sufficient to guarantee loop stability (see related section).
3	VFB	Error amplifier inverting input. The output voltage can be adjusted by connecting this pin to an external resistor divider from 0.6 V up to the input voltage.
4	GND	Ground.
5	LX	Switch output node. This pin is internally connected to the drain of the internal switches.
6	VCC	Input voltage. The start-up input voltage is 2.2 V (typ.) while the operating input voltage ranges from 2 V to 5.5 V. An internal UVLO circuit generates a 200 mV (typ.) hysteresis.
7	SYNC	Operating mode selector input. When high (above 1.3 V) Low Consumption Mode is selected. When low (less than 0.5 V), Low Noise Mode is selected. If connected to an appropriate external synchronization signal (from 1 MHz up to 2 MHz) the internal synchronization circuit is activated and the device works at the same switching frequency. This pin must not be left floating.
8	PGOOD	Power good comparator output. It is an open drain output. A pull-up resistor should be connected between PGOOD and V_o (or VCC depending on the requirements). The pin is forced low when the output voltage is lower than 90% of the regulated output voltage, and goes high when the output voltage is greater than 90% of the regulated output voltage. The pin can be left floating if not needed.

3 Block diagram

Figure 5. Block diagram



4 Operation description

The main loop uses a constant frequency peak current mode architecture. Each cycle, the high side MOSFET is turned on, triggered by the oscillator, so that the current flowing through it (which is the same as the inductor current) increases.

When this current reaches the threshold (set by the output of the error amplifier E/A, the peak current limit comparator, PEAK_CL, turns off the high side MOSFET and turns on the low side MOSFET until the next clock cycle begins, or if the current flowing through it decreases to zero (ZERO CROSSING comparator).

In particular, the error amplifier output is dependent on the FB pin voltage. When the output current increases, the output capacitor is discharged and so the FB pin voltage decreases. This produces an increase in the error amplifier output, allowing a higher value for the peak inductor current. For the same reason, when the output current decreases due to a load transient, the error amplifier output goes low, thus reducing the peak inductor current to meet the new load requirements.

The system includes a slope compensation signal, added to the sensed high side ramp current, which provides loop stability even in high duty cycle conditions (see related section).

4.1 Light load modes of operation

Depending on the SYNC pin value, the device can operate in LCM (low consumption mode) or LNM (low noise mode). If the SYNC pin is high (greater than 1.3 V) low consumption mode is selected while low noise mode is selected if the SYNC pin is low (less than 0.5 V).

4.2 Low consumption mode

In this mode of operation, the device operates discontinuously based on the COMP pin voltage in order to maintain very high efficiency even in light load conditions. When the device is not switching, the load discharges the output capacitor and the output voltage decreases. When the feedback voltage goes below the internal reference, the COMP pin voltage increases, and when an internal threshold is reached the device begins to switch. In this condition the peak current limit is set in the range of approximately 200 mA - 400 mA, depending on the slope compensation (see related section).

Once the device starts to switch, the output capacitor is recharged. The feedback pin voltage increases and, when it reaches a value slightly higher than the reference voltage, the output of the error amplifier decreases until a clamp is activated.

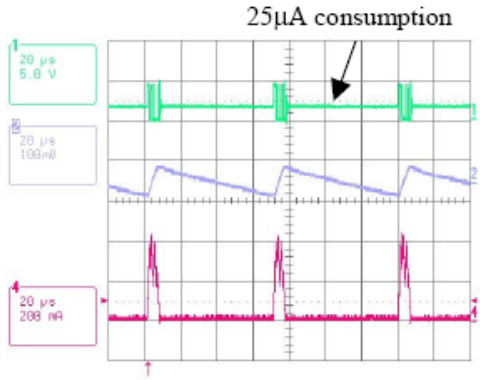
At this point the device stops switching. In this phase, most of the internal circuitry is off, reducing the device's consumption down to a typical value of 25 µA.

4.2.1 Low noise mode

If for noise considerations, the very low frequencies of low consumption mode are undesirable, low noise mode can be selected. In low noise mode, efficiency is slightly lower compared to low consumption mode in very light load conditions, but for medium-high load currents the efficiency values are very similar.

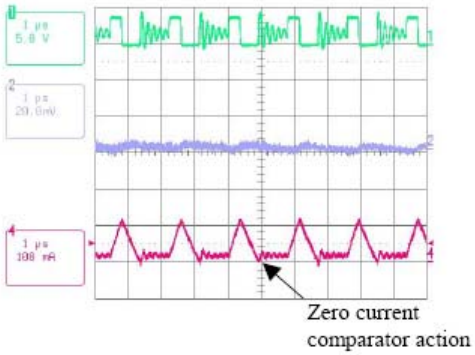
Basically, the device switches with its internal free running frequency of 1.4 MHz. Obviously, in very light load conditions, the device could skip some cycles in order to keep the output voltage regulated. In *Figure 6* and *Figure 7* the LCM and LNM typical waveforms are shown.

Figure 6. Low consumption mode



Red line: inductor current
Blue line: output voltage (AC coupled)
Green line: LX pin

Figure 7. Low noise mode



Red line: inductor current
Blue line: output voltage (AC coupled)
Green line: LX pin

- Measurement conditions:
  - V_{in} = 4.2 V
  - V_{out} = 1.5 V
  - I_{out} = 30 mA
  - L = 3.3 µH
  - C_{IN} = 10 µF
  - C_{OUT} = 10 µF
  - R_C = 20 kΩ
  - C_C = 330 pF

A comparison between the efficiency in low noise mode and low consumption mode is shown in *Figure 19* of this document.

4.3 System stability

Since the device is designed with a current mode architecture, loop stability is rarely a significant issue. For most applications a 220 pF capacitor connected between the COMP pin and ground is sufficient to guarantee stability. If very low ESR capacitors are used for the output filter, such as multilayer ceramic capacitors, the zero introduced by the capacitor itself can shift at very high frequency and the transient loop response could be affected. Adding a series resistor to the 220 pF capacitor may resolve this problem. The appropriate value for the resistor (in the range of 50 kΩ) can be determined by checking the load transient response of the device. Basically, the output voltage should be checked with an oscilloscope after the load steps required by the application.

If there are stability problems, the output voltage could oscillate before reaching the regulated value after a load step. The current mode stability can be observed in two consecutive steps: first, the inner (current) loop is closed, then the second (voltage) loop stability is considered.

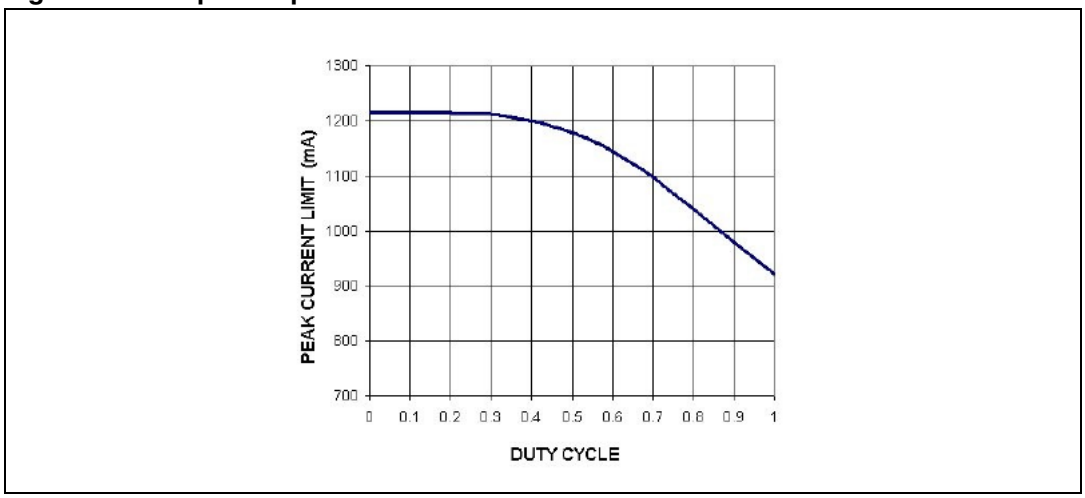
4.3.1 Current loop compensation

The constant frequency, peak current mode control architecture offers numerous advantages: easy compensation with ceramic output capacitors, fast transient response and intrinsic peak current measurement which simplifies the current limit protection.

One drawback, however, is that the current loop becomes unstable when the duty cycle exceeds 50%. This phenomenon is known as "sub-harmonic oscillation" and can be avoided by adding an external ramp to the one coming from the sensed current (or, by subtracting it from the control value, which is the E/A output voltage).

This additional ramp is called "slope compensation". In the L6928D the slope compensation is implemented from a duty cycle of around 25% - 30%, as shown in *Figure 8*.

Figure 8. Slope compensation



The figure above shows that the current limit value will depend on the duty factor, so changing the output voltage will also change the maximum output load.

The amount of slope compensation depends on the inductor current slope during the OFF time. This slope, for a given duty cycle, is inversely proportional to the inductor value.

Since the device can be synchronized at a higher frequency, the inductor value can be adjusted based on this. In fact, for a given current ripple, the required inductor value is inversely proportional to the frequency. Finally, the input voltage affects the OFF time slope as well. This is obvious because, for a given duty cycle, the output voltage (and thus the OFF time inductor current slope) is directly proportional to the input voltage.

In order to better manage these issues, the amount of slope compensation in the L6928D depends both on the switching frequency and input voltage.

Table 2. Minimum inductor value to ensure loop stability

V_{in} [V]	V_{out} [V]	F_{SW} [kHz]	Minimum inductor value [µH]
3.3	1.8	1000	1.0
		2000	1.0
5	3.3	1000	2.2
		2000	2.2

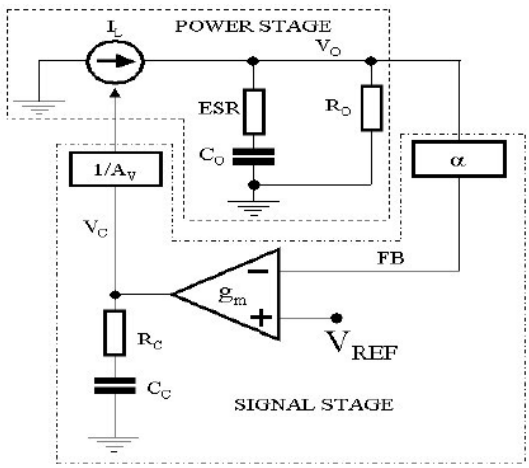
In the table above the minimum inductance values to ensure current loop stability with input voltage of 3.3 V and 5 V are shown. There is also a maximum inductor value, because if the inductor is too high the inductor current ripple will be very low (theoretically down to zero) and will be compared with the slope compensation (a triangular waveform) to generate the duty cycle. This system is similar to the voltage mode control causing stability problems due to the LC double pole (the pole splitting effect will not be present).

4.3.2 Voltage loop compensation

After closing the current loop, the pole splitting effect will separate the complex double pole, due to the inductor and the output capacitor, into 2 separate poles. The pole due to the inductor will shift outside of the system bandwidth (i.e. the inductor ideally acts like a current source), while the pole due to the output capacitor will remain within the bandwidth.

Figure 9 shows the equivalent circuit used to study the voltage loop compensation:

Figure 9. Equivalent circuit for voltage loop analysis



To complete the power stage analysis, the zero due to the output capacitor ESR should be considered.

Equation 1

$$H(s) = \frac{V_o(s)}{I_L(s)} = \frac{(sC_oESR + 1)R_o}{sC_o(ESR + R_o) + 1}$$

In *Equation 1* the power stage transfer function is shown, where RO is the output equivalent resistor load (V_o/I_o). It can be observed that the pole due to the output capacitor shifts in frequency based on the load value.

In order to have zero DC error regulation, the feedback voltage loop is implemented with an integrator stage, the transfer function of which is shown in *Equation 2*.

Equation 2

$$G(s) = \frac{g_m \alpha}{A_V} \bullet \left(\frac{sC_CR_C + 1}{sC_C}\right)$$

where g_m is the integrator transconductance (250 µS). The total gain loop is:

Equation 3

$$G_{LOOP}(s) = \frac{R_o g_m \alpha (1 + sESRC_o)(sC_CR_C + 1)}{A_V sC_C(1 + sC_o(ESR + R_o))}$$

where A_V is the current loop factor (1 Ω typ.) and α is the resistor feedback network partition ($R_2/(R_2+R_3)$). *Equation 3* does not consider the poles due to the sampling effect which are placed at half of the switching frequency.

Once the gain loop is known, the system will be stabilized with the compensation network as shown in the *Section 6.1.4*.

4.4 Short circuit protection

Due to the peak current mode architecture, the peak current flowing through the high side switch is accurately sensed.

When this current reaches the peak current limit threshold, the P-channel MOSFET is turned off. In this way, the ON time of the high side switch, T_{ON}, is reduced and the output voltage decreases. The T_{ON} can decrease down to its minimum value of around 200 nsec (T_{MIN}). In this condition, however, a strong overload or short circuit could result in a further increase in peak current.

Equation 4

$$\Delta I_{ON} = \frac{(V_{in} - V_{out})}{L} \bullet T_{ON} \qquad \text{(Positive slope)}$$

Equation 5

$$\Delta I_{OFF} = \frac{V_{out}}{L} \bullet T_{OFF} \qquad \text{(Negative slope)}$$

It can be observed in the equations above that in short circuit condition the output voltage is zero and thus the negative slope will be zero. Since the positive slope increases with every cycle, the inductor current will likewise increase cycle by cycle.

In order to determine at what point this phenomenon will cease, some real parameters should be considered.

Figure 10. Equivalent buck converter circuit (during ON time)

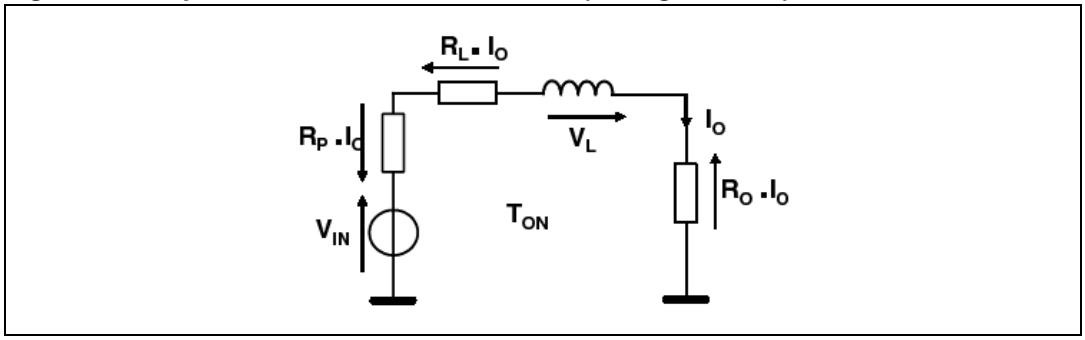
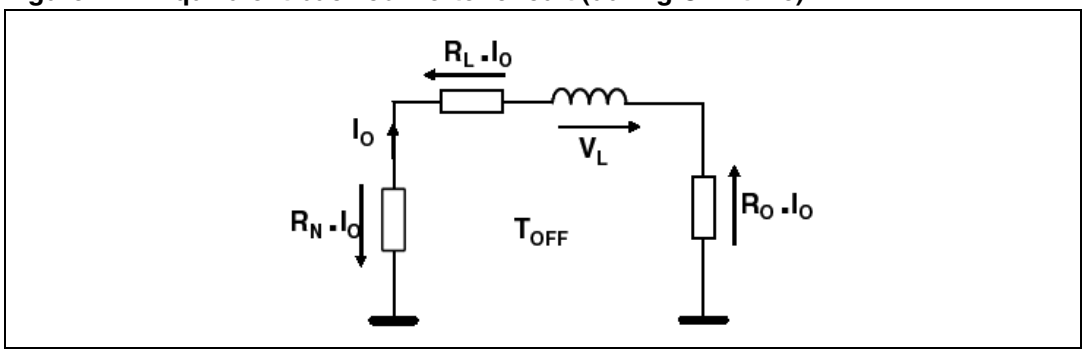


Figure 11. Equivalent buck converter circuit (during OFF time)



Considering the figures above, particularly during OFF time, even though the output voltage is equal to zero, the output current generates the voltage drop necessary to produce a negative slope on the parasitic resistances.

So the higher the output current, the higher the negative slope during OFF time. In this way the inductor current will find a stable find value, which can be derived using the equation below:

Equation 6

$$I_{LIM} = \frac{V_{in} \bullet (T_{MIN} \bullet F_{SW})}{[(R_N + R_L) \bullet (1 - T_{MIN} \bullet F_{SW}) + (R_P + R_L) \bullet (T_{MIN} \bullet F_{SW})]}$$

where T_{MIN} is the minimum ON time, F_{SW} is the switching frequency, R_N and R_P are the ON resistances of the N-channel and P-channel MOSFETs respectively, R_L is the inductor series resistance and R_O is the equivalent output resistance. As can be observed, under these extreme conditions the maximum current value depends on both the application conditions (such as V_{in} and F_{SW}) as well as the inductor parasitic resistor R_L and the MOSFETs' $R_{DS(on)}$, R_N and R_P.

The maximum current value does not depend on the peak current limit at all. In order to limit the output current to a safe value even in extreme short circuit conditions, a current limit has also been introduced on the N-channel MOSFET, which operates as a valley current limit.

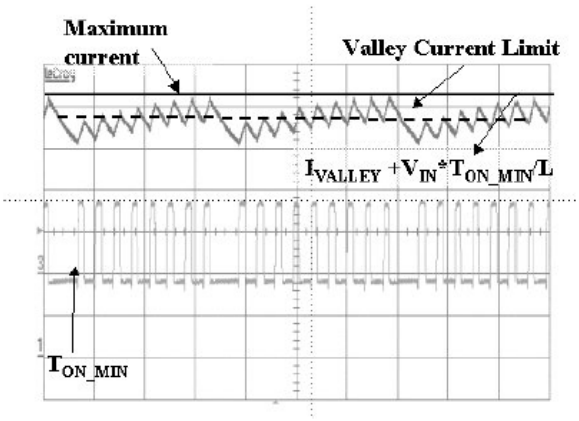
Figure 11 shows its operation. The P-channel MOSFET does not turn on until the inductor current exceeds the valley current limit. This implies that the device skips some cycles depending on the overcurrent conditions, reducing the equivalent switching frequency in

order to limit the output current. With this approach, the maximum peak current is definitively limited to:

Equation 7

$$I_{LIM} = I_{VALLEY} + \frac{V_{in} T_{MIN}}{L}$$

Figure 12. Valley current limit intervention



5 Synchronization

The device can also be synchronized with an external signal from 1 MHz up to 2 MHz through the internal PLL. When the device is locked, the external signal and the high side turn on rising edges are aligned. In this case, low noise mode is automatically selected.

The device could skip some cycles in very light load conditions depending on the input/output conditions. The internal synchronization circuit is inhibited in short circuit and overvoltage conditions in order to keep the protections effective (see relative sections).

The synchronization signal amplitude can range typically from 1 V to V_{CC} and the duty factor can range typically from 20% to 80%. Occasionally, if the synchronization signal duty cycle is very similar to the application duty factor, a jittering can be detected on the LX pin. In this case some practical solutions are listed below:

1. Change the synchronization signal duty factor.
2. Decrease the synchronization signal amplitude.
3. Add a 20 pF capacitor between the COMP pin and ground.

The device switches at 1.4 MHz (typ.) if no synchronization signal is applied.

5.1 Dropout operation

The Li-Ion battery voltage ranges from approximately 3 V to 4.2 V (depending on the anode material). If the regulated output voltage is from 2.5 V and 3.3 V, it is possible for the battery voltage to decrease to the regulated voltage near the end of battery life.

In this case, the device stops switching and works at 100% of duty cycle, minimizing the dropout voltage and the device losses. The minimum input voltage necessary to ensure output regulation can be calculated as:

Equation 8

$$V_{in-MIN} = V_o + I_o \bullet (R_{DS(on)-HS-MAX} + R_L)$$

Where $R_{DS(on)\_HS\_MAX}$ is the maximum high side resistance and RL is the series inductor resistance.

5.2 PGOOD (Power good output)

The device also features a power good output signal. The VFB pin is internally connected to a comparator with a threshold set at 90% of the reference voltage (0.6 V). Since the output voltage is connected to the VFB pin by a resistor divider, when the output voltage goes lower than the regulated value, the VFB pin voltage goes lower than 90% of the internal reference value. The internal comparator is triggered and the PGOOD pin is pulled down. The pin is an open drain output, so it should be connected to a pull up resistor. If the feature is not required, the pin can be left floating.

5.3 Adjustable output voltage

The output voltage can be adjusted by an external resistor divider from a minimum value of 0.6 V up to the input voltage. The output voltage value is given by:

Equation 9

$$V_{out} = 0.6 \bullet \left(1 + \frac{R_3}{R_2}\right)$$

Thanks to the very low FB leakage current (25 nA), high R_3 and R_2 values can be chosen (hundreds of kΩ) which increase system efficiency at very low load.

5.4 OVP (overvoltage protection)

The device is equipped with an internal overvoltage protection circuit to protect the load. If the voltage at the feedback pin goes higher than an internal threshold set at 10% (typ.) higher than the reference voltage, the low side MOSFET is turned on until the feedback voltage goes lower than the reference voltage. During overvoltage circuit intervention, the zero crossing comparator is disabled so that the device is also able to sink current.

5.5 Thermal shutdown

The device also has thermal shutdown protection, which is activated when the junction temperature reaches 155 °C. In this case both the high and low side MOSFETs are turned off.

Once the junction temperature goes back below 95 °C, the device resumes normal operation.

6 Application information

6.1 External component selection

6.1.1 Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current. Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current.

The RMS input current (flowing through the input capacitor) is:

Equation 10

$$I_{RMS} = I_o \bullet \sqrt{D - \frac{2 \bullet D^2}{\eta} + \frac{D^2}{\eta^2}}$$

Where η is the expected system efficiency, D is the duty cycle and I_o is the output DC current. Assuming $\eta = 1$, this function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to $I_o/2$. The maximum and minimum duty cycles are:

Equation 11

$$D_{MAX} = \frac{V_o}{V_{inMIN}}$$

Equation 12

$$D_{MIN} = \frac{V_o}{V_{inMAX}}$$

Depending on the output voltage value, the worst case could occur when the input battery is nearly discharged. Usually the best choice for the input capacitor is the MLCC (multi layer ceramic capacitor) thanks to its very small size and very low ESR. *Table 3* provides a list of some MLCC manufacturers.

Table 3. Recommended input capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR@1.4 MHz (mΩ)
Panasonic	ECJ	10 to 22	6.3	10
Taiyo Yuden	JMK	10 to 22	6.3	10
Murata	GRM	10 to 22	6.3	5 to 10

6.1.2 Output capacitor

The output capacitor is very important for satisfying the output voltage ripple requirement. Very small inductor values reduce the size and cost of the application but increase the current ripple.

This ripple, multiplied by the ESR of the output capacitor, is the output voltage ripple. Tantalum and ceramic capacitors are usually good for this purpose. Ceramic capacitors

have the minimum ESR for a given size, so for very compact applications they are the best choice.

POSCAP capacitors from Sanyo are also a good choice for the output filter. The list below provides some capacitor manufacturers.

Table 4. Recommended output capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
Panasonic	ECJ	10 to 47	6.3	10
Panasonic	EEF	22 to 47	6.3	60 to 90
Taiyo Yuden	JMK	10 to 47	6.3	10
Sanyo POSCAP	TPA	47 to 100	6.3	80 to 100
Murata	GRM	10 to 22	6.3	5 to 10

6.1.3 Inductor

The inductor value establishes the ripple current flowing through the output capacitor. The ripple current is usually fixed at 20% - 40% of the output current, an approximation of which is obtained with the following formula:

Equation 13

$$L = \frac{(V_{in} - V_{out})}{\Delta I} \bullet T_{ON}$$

For example, with V_{out} = 3.3 V, V_{in} = 4.2 V (Li-Ion battery fully charged), F_{SW} = 1.4 MHz, I_O = 600 mA and ΔI = 200 mA, the inductor value is about 3.3 µH. The peak current through the inductor is given by:

Equation 14

$$I_{PK} = I_o + \frac{\Delta I}{2}$$

Note that if the inductor value decreases, the peak current (which must be lower than the current limit of the device) increases. This peak current must be lower than the saturation current of the choke.

This is particularly important when using ferrite cores because they can saturate severely. The inductance value decreases abruptly when the saturation threshold is exceeded, thus causing an abrupt increase in the current flowing through it.

The inductor should be selected with system stability taken into consideration (see the paragraph regarding slope compensation).

Parasitic resistance should also be considered when selecting the inductor, as too high a value can decrease efficiency. In the following table some inductor manufacturers are listed.

Table 5. Recommended inductors

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	DO1607C	6.8 to 15	0.72 to 0.96
	DT1608C	6.8 to 15	0.6 to 1
	LPO1704	6.8 to 10	0.8 to 0.9
	CH4192-A	4.7	1.3
	DO1606T	6.8 to 10	1 to 1.1
Panasonic	ELL6RH	6.2 to 22	0.7 to 1.4
	ELL6GM	6.8 to 10	0.93 to 1.1
Toko	D62CB	10 to 22	0.71 to 1.07
	D62C	10 to 22	0.63 to 0.99
Coiltronics	SD10	3.3 to 6.2	0.92 to 1.31
	SD12	3.3 to 6.2	1.08 to 1.42

6.1.4 Compensation network (R_1 C_3)

As shown in *Section 4.3* the system stability can be studied using the loop transfer function given by *Equation 3*. If the output capacitor is of the ceramic type, the zero due to the ESR will generally be outside of the system bandwidth. Thus, the stability of the system will be ensured by the cancellation between the pole due to the output capacitor, the equivalent load and the R_1C_3 zero. *Equation 15* represents a simplified gain loop expression, applicable around the transition frequency f_T:

Equation 15

$$G_{LOOP}(s) = \frac{g_m R_1 \alpha}{sC_2}$$

Assuming that C_2 = 10 uF, the transition frequency at 0 dB = 30 kHz (f_T is equal to the system bandwidth), and the output voltage = 1.8 V, the value of R1 can be calculated as:

Equation 16

$$R_1 = \frac{2\pi f_T C_2}{g_m \alpha} = 24k\Omega$$

The nearest standard E12 series value is R_1 = 24 kΩ.

The higher the bandwidth, the faster the transient response will be, but the bandwidth (and so the R_1 value) must be lower than f_{SW}/10 to avoid being influenced by the sampling effect poles as mentioned in *Section 4.3*. The zero due to the compensation network must be at the least 5 times before the frequency transition, so the value of C3 will be:

Equation 17

$$C_3 = \frac{5}{2\pi f_T R_1} = 220pF$$

The nearest standard value is C_3 = 220 pF

If the output capacitors are of the tantalum type, the ESR zero is within the system bandwidth and it can be used to stabilize the system so that the zero due to the compensation network will be rendered unnecessary.

6.2 Application losses and efficiency

There are many losses affecting the efficiency of the application. Some of these losses are related to the device and others are related to the external components. The most important losses are described below.

6.2.1 Conduction losses

These losses are basically due to the significant resistances of the internal switches and the external inductor. Usually the current ripple across the inductor is negligible and so to estimate the conduction losses of the inductor, the average output current can be considered.

The conduction losses of the switches depend also on the duty cycle of the application.

The RMS current flowing through the high side MOSFET is $(I_o)^2D$, while the RMS current flowing through the low side MOSFET is $(I_o)^2$ (1-D). So, the total conduction losses of the application are:

Equation 18

$$P_{MOS} = I_o^2 \bullet (R_{ON-HS} \bullet (D) + R_{ON-LS} \bullet (1-D) + R_L)$$

Where R_{ON-HS} and R_{ON-LS} are the series resistances of the high side and low side MOSFETs respectively, and R_L is the series resistance of the inductor. The conduction losses due to the ESR of the input and output capacitors are usually negligible, particularly when using ceramic caps (very low ESR). In any case, when the ESR values for these caps are high, their conduction losses are:

Equation 19

$$P_{CIN,COUT} = I_o^2 \bullet (D \bullet (1-D)) \bullet ESR_{CIN} + \frac{\Delta I^2}{12} \bullet ESR_{COUT}$$

Where ΔI is the current ripple flowing through the choke and D the duty cycle of the application. The conduction losses are particularly important at high current cause they depend on its squared value.

6.2.2 Switching losses

The switching losses are due to the turning on and off of the internal high side MOSFET.

Equation 20

$$P_{SWITCHING} = V_{in} \bullet I_o \bullet F_{SW} \bullet \frac{(T_{ON} + T_{OFF})}{2}$$

where T_{ON} and T_{OFF} are the turn on and turn off times of the internal high side switch. These are approximately in the range of 15 ns to 20 ns.This loss is important at high frequency.

6.2.3 Gate charge losses

The gate charge losses derive from switching the gate capacitance of the internal MOSFETs. The gate capacitances (C_H for the high side MOSFETs and C_L for the low side MOSFETs) are charged and discharged with the input voltage at the switching frequency.

Equation 21

$$P_{GATE-CHANGE} = V_{in}^2 \bullet (C_H + C_L) \bullet F_{SW}$$

These losses are also directly proportional to the switching frequency and input voltage but are usually negligible compared with the conduction and switching losses.

6.2.4 Thermal consideration

Depending on the application conditions (input voltage, switching frequency, output current) and ambient temperature, the heat produced by device losses could increase the junction temperature to over its absolute maximum rating. The following equation can estimate the junction temperature of the device:

Equation 22

$$T_j = T_A + R_{TH-JA} \bullet P_{tot}$$

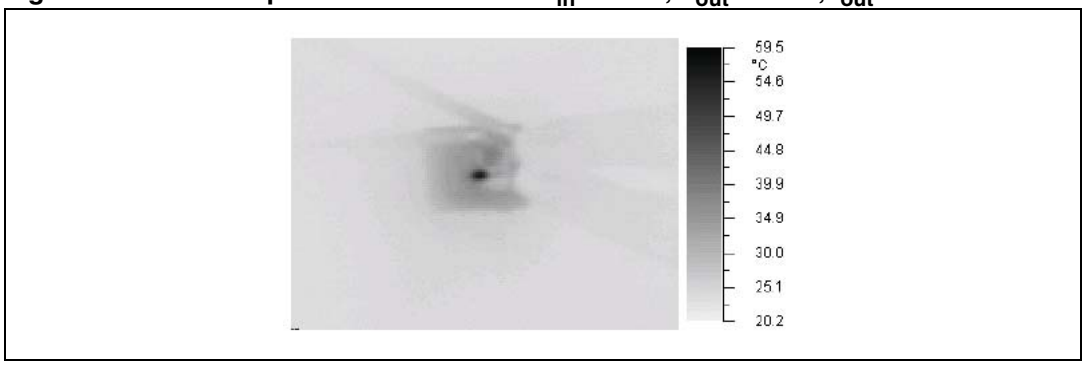
where T_A is the ambient temperature of the application, R_{TH_JA} is the thermal resistance junction to ambient of the package and P_{tot} is the overall power dissipated by the device.

R_{TH_JA} depends to some degree on the application board but it can considered approximately equal to 180 °C/W. P_{tot} given by:

Equation 23

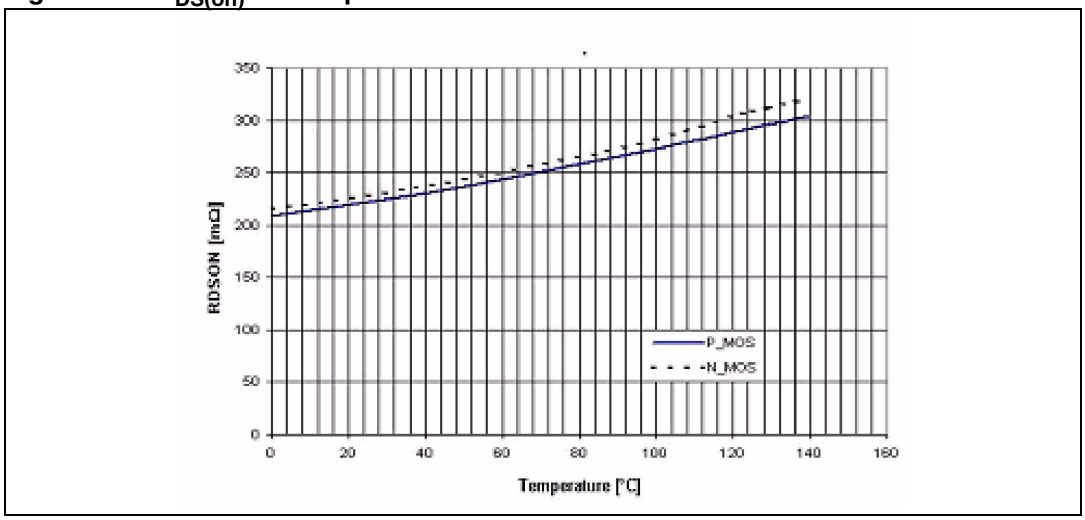
$$P_{tot} = P_{MOS} + P_{SWITCHING} + P_{GATE-CHARGE}$$

Figure 13. Thermal performance results: V_{in} = 3.7 V, V_{out} = 1.8 V, I_{out} = 800 mA



The figure above shows the thermal performance of the device mounted on the application board, which is described in the following paragraph.

Figure 14. $R_{DS(on)}$ vs. temperature



To more accurately estimate the power dissipated, it may be useful to observe the variation with the temperature of the MOSFET's $R_{DS(on)}$, as shown in the *Figure 14*.

7 Application board

7.0.1 Demoboard layout

The illustrations below show the layout of the demoboard.

Figure 15. Component placement

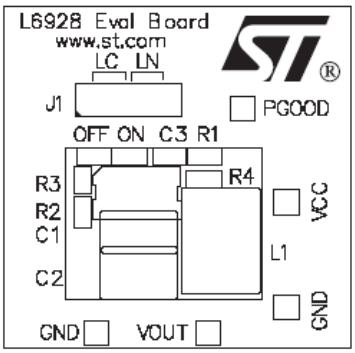


Figure 16. Top side view

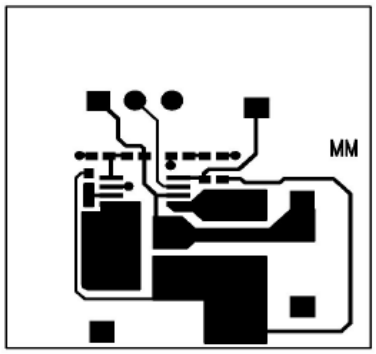
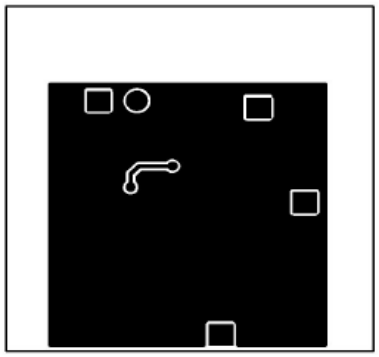


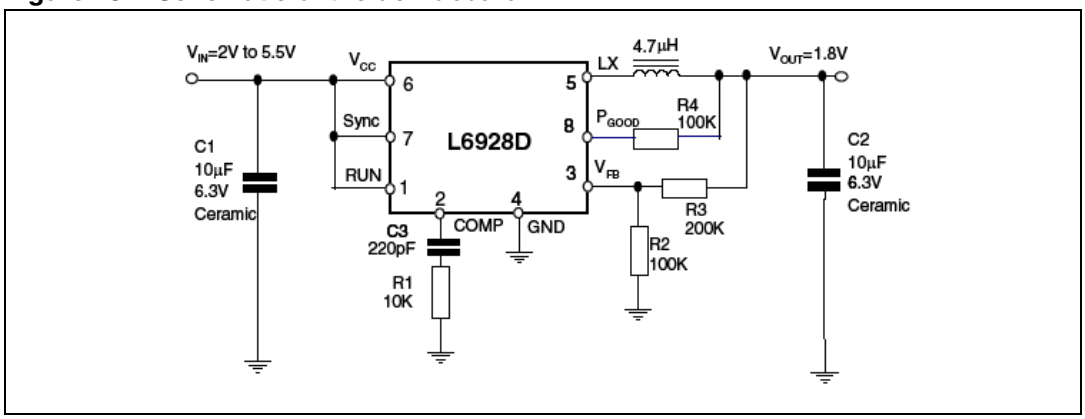
Figure 17. Bottom side view



8 Demoboard schematic

The very small package and high switching frequency allow for a very compact application. The demoboard circuit is shown in *Figure 18*:

Figure 18. Schematic of the demoboard



The external component parts list is shown below:

Table 6. Demoboard parts list

Reference	Part number	Description	Manufacturer
C1	GRM21BR60J106KE19	10 µF 6.3 V	Murata
C2	GRM21BR60J106KE19	10 µF 6.3 V	Murata
C3	C0406C221J5GAC	220 pF, 5% 50 V	Kemet
R1		10 kΩ 1% 0402	Neohm
R2		100 kΩ 1% 0402	Neohm
R3		200 kΩ 1% 0402	Neohm
R4		100 kΩ 1% 0402	Neohm
L1	CH4194-A	4.7 µH	Coilcraft

9 Efficiency results

Some efficiency results are shown in the figures below.

Figure 19. Low noise vs. low consumption efficiency

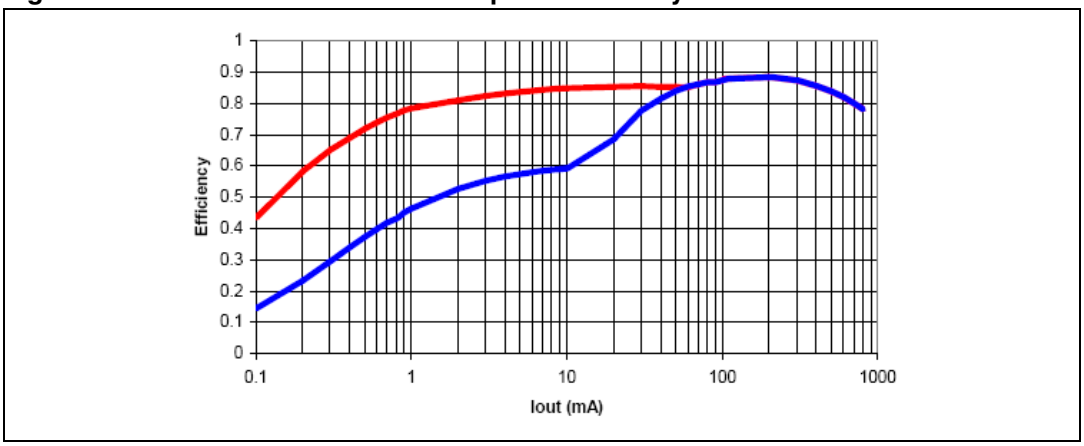


Figure 20. Efficiency vs. output current

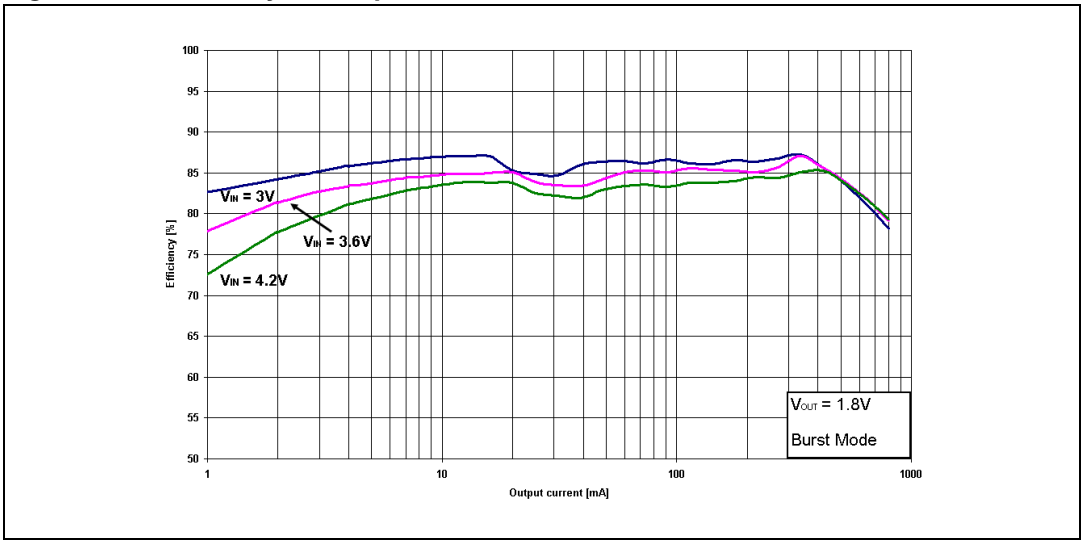


Figure 21. Efficiency vs. output current

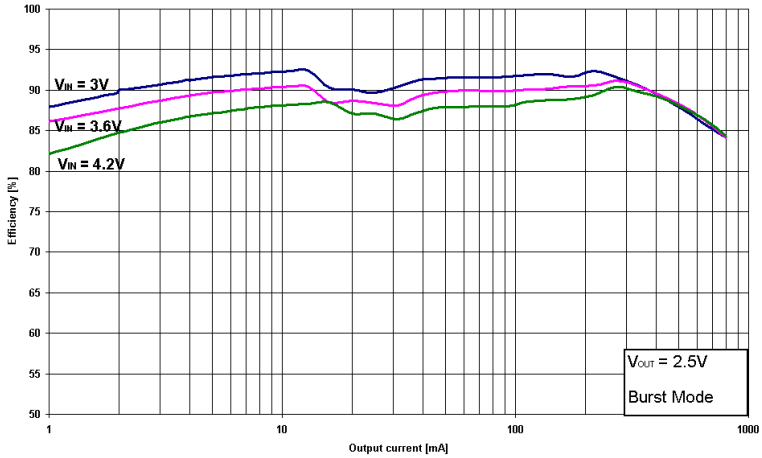
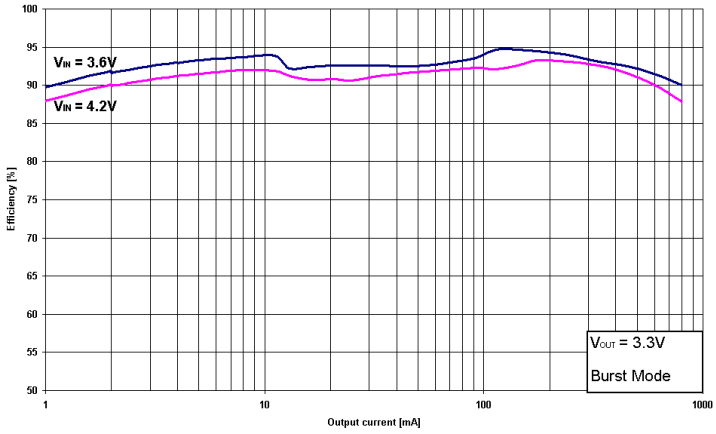


Figure 22. Efficiency vs. output current



10 Application ideas

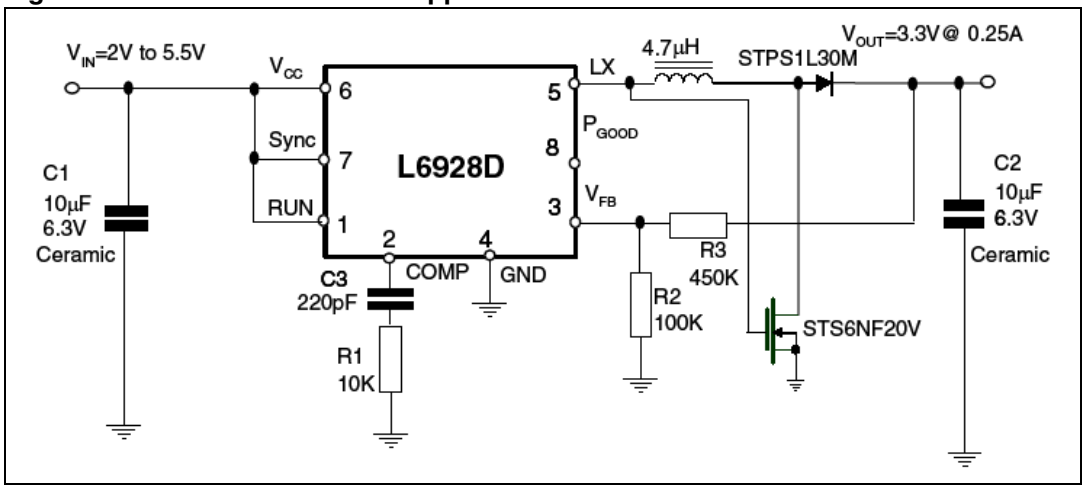
10.1 Buck boost topology

In portable applications, the input voltage changes significantly due to the battery discharge profile, which often depends on parameters like temperature, discharge rate, battery ageing, etc. Moreover, in certain applications the output voltage requirements can also change.

This could imply that is not possible to provide the desired regulated output voltage using a simple buck topology. This problem is often present, for example, in systems using a single Li-Ion cell, whose voltage profile changes from 4.2 V down to 2.7 V or less. In fact, in these systems, a 3.3 V output is normally required to power the processor I/O, memory and logic. Adopting the buck topology, the 3.3 V output can be regulated until the battery voltage is approximately 3.4 V, depending also on the minimum dropout of the regulator. Depending on the battery type and conditions, this would leave unused some 20 - 40% of its capacity. Another even more critical application is the power management of 3G phones, where 3.7 V or more can be required to power the RF power amplifier (PA).

In order to use the full battery capacity in these applications, a positive buck boost topology can be used. *Figure 23* shows how to implement this topology using the L6928D. This topology may be more suitable than a standard buck, depending on the battery discharge profile and the load conditions. In fact, the efficiency loss of the buck boost topology can be translated into an equivalent loss in battery capacity. This can then be compared with the gain in battery capacity due to the fact that it is used over the full voltage range.

Figure 23. Positive buck boost application. 1 Li-Ion cell to 3.3 V@0.25 A



10.2 White LEDs

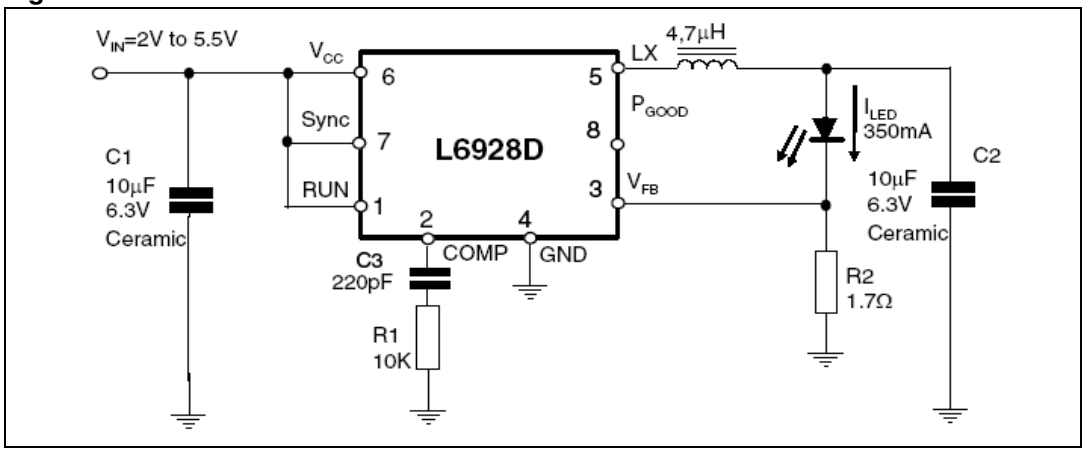
White LEDs are now widely used both for LCD backlighting and for illumination. Since their brightness is proportional to the current flowing through them, a current control loop must be implemented rather than a voltage control loop. The L6928D can be used in a current control architecture by simply inserting a sense resistor between the FB and GND pins and connecting the LED in series with it. The loop will set 0.6 V across the sense resistor and thus a constant current flow through the LED. The current, and therefore the brightness, can be adjusted by changing the resistor value or the voltage across it (by partitioning the FB pin

voltage). The forward voltage across a white LED is approximately 3.6 V and so, depending on the input source, appropriate topologies must be used.

10.2.1 Driving white LEDs: buck topology

The simple buck topology can be used when the input voltage source is higher than approximately 4.5 V, which is the case, for example, with a USB bus.

Figure 24. Buck LED

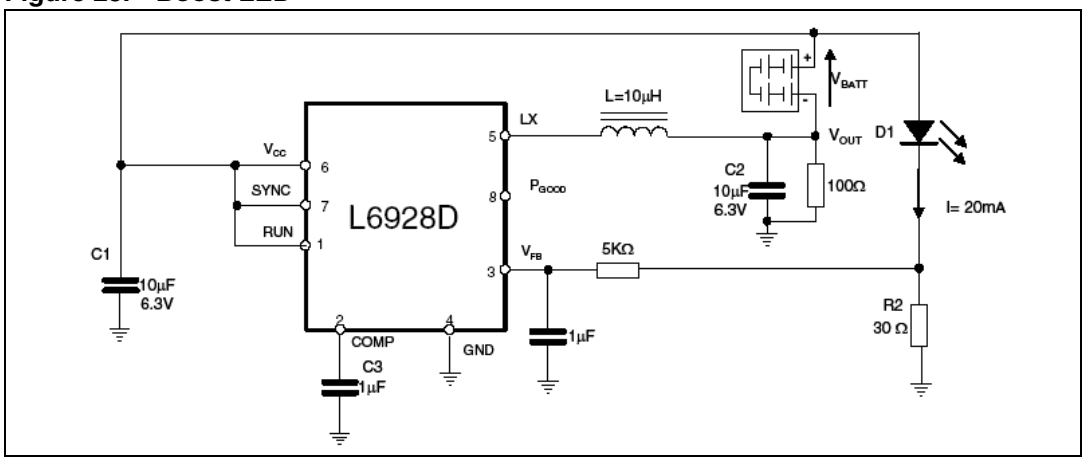


In this case, the maximum device current (800 mA, continuous) can be delivered to the LED. Moreover, in this topology the efficiency is maximized.

10.2.2 Driving white LEDs: boost topology

When the input voltage source is always lower than 3 V (which is the case, for example, of 2 NiMH battery cells) a boost topology must be implemented, as shown in *Figure 25*.

Figure 25. Boost LED



In this case, according to the boost topology, the maximum current that can be delivered depends on the duty cycle. The relation between the output current and the internal switch current (assuming a negligible current ripple and 100% efficiency) is given in *Equation 24*:

Equation 24

$$I_{OUT} = I_{SWITCH}(1 - D)$$

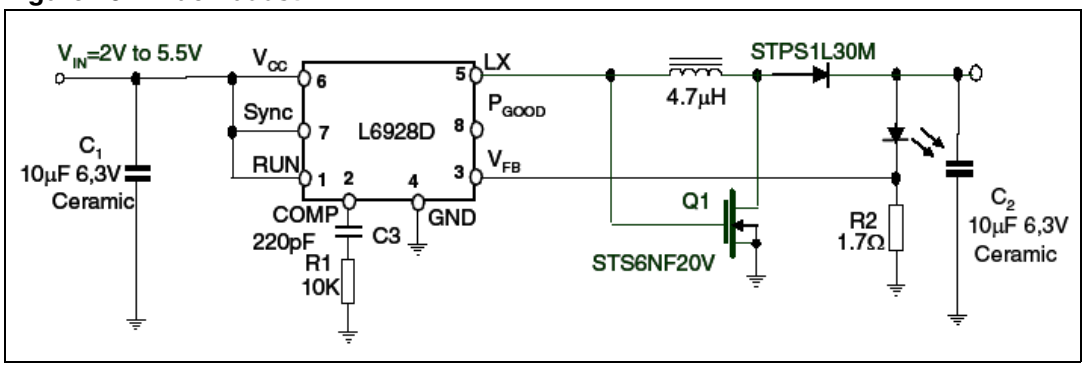
This topology is possible only because the input source is a battery, and so it must not be referred to ground. A drawback of this approach, which is intrinsic in the boost topology, is that a path between the input and output is always present.

This does not allow effective short circuit protection and can generate a battery discharge even when the device is turned off.

10.2.3 Driving white LEDs: buck boost topology

When a single Li-Ion cell is used at the input, a buck boost topology can be employed, as shown in *Figure 26*.

Figure 26. Buck boost LED



The relationship between the output current and the switch current is the same as in the boost topology. An advantage of this topology compared with the boost topology, however, is that when the device is turned off there is no current path between the input and the output.

This allows effective short circuit protection and minimizes the current drawn from the battery when the device is turned off. A dimming control can be developed by turning the device on and off with a frequency of around 100 - 200 Hz in order to avoid LED flickering (*Figure 27*). Another way to implement LED dimming is by changing the voltage of the dimming resistor (*Figure 28*).

Figure 27. LED dimming control using PWM

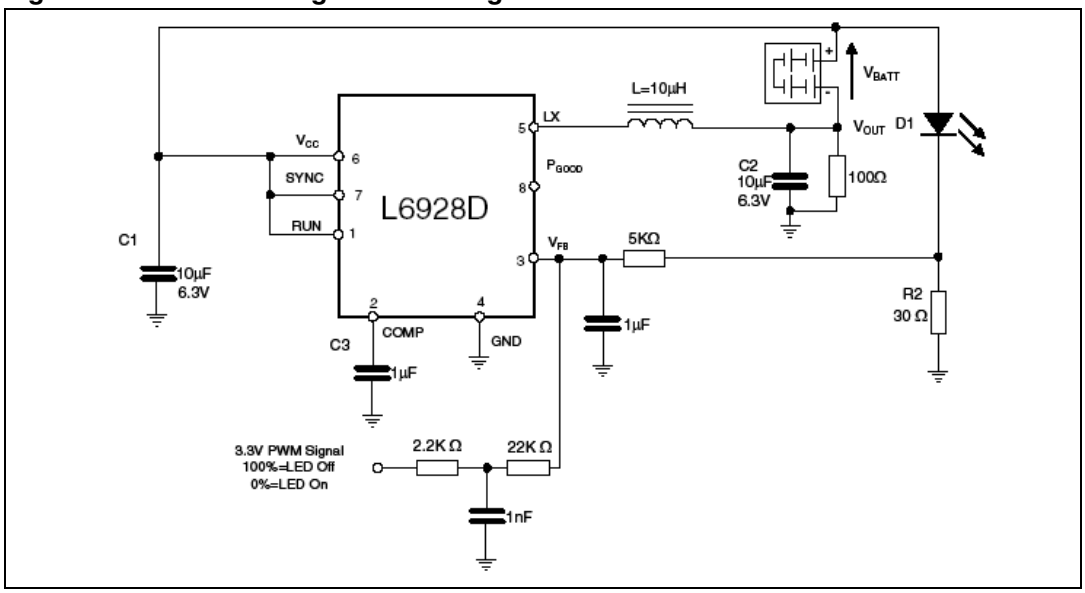
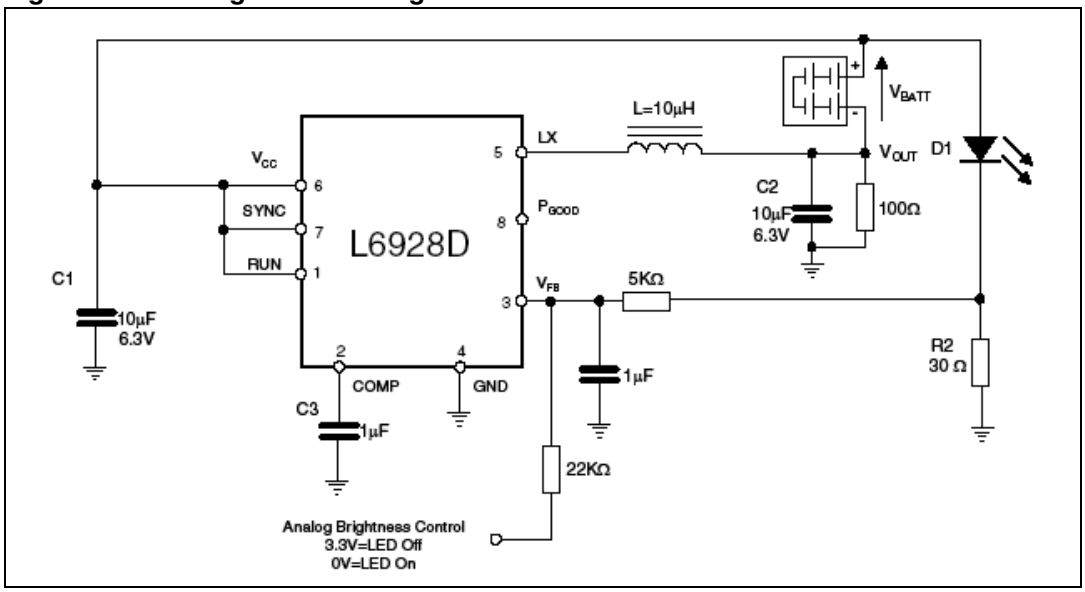


Figure 28. Analog LED dimming control



Both solutions change the output current by changing the FB voltage. In *Figure 28* a DC voltage is used. In *Figure 27* the average voltage coming from the PWM signal is utilized.

11 Revision history

Table 7. Document revision history

Date	Revision	Changes
Jan-2005	1	First issue
06-Aug-2007	2	– Document reformatted – Added *List of figures* – Minor text changes
28-Nov-2007	3	Changed *Figure 14*
26-Feb-2009	4	– Modified: *Section 6.1.1* – Modified: *Table 6* (reference 3)

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