

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Max t_{pd} of 3.6 ns at 3.3 V
- ±24-mA Output Drive at 3.3 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

DESCRIPTION/ORDERING INFORMATION

This 16-bit transparent D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. This device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the busines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. \overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

DGG OR DL PACKAGE
(TOP VIEW)

\overline{OE}	1	48	1LE
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	4	45	GND
1Q3	5	44	1D3
1Q4	6	43	1D4
V_{CC}	7	42	V_{CC}
1Q5	8	41	1D5
1Q6	9	40	1D6
GND	10	39	GND
1Q7	11	38	1D7
1Q8	12	37	1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	16	33	2D3
2Q4	17	32	2D4
V_{CC}	18	31	V_{CC}
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	GND
2Q7	22	27	2D7
2Q8	23	26	2D8
\overline{OE}	24	25	2LE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

SN74ALVCH16373
16-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

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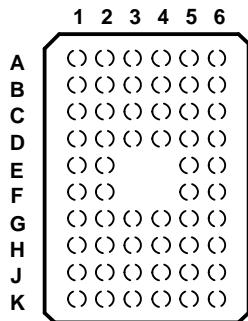
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ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	FBGA – GRD	Tape and reel	SN74ALVCH16373GRDR	VH373
	FBGA – ZRD (Pb-free)		SN74ALVCH16373ZRDR	
	SSOP – DL	Tube	SN74ALVCH16373DL	ALVCH16373
		Tape and reel	SN74ALVCH16373DLR	
			74ALVCH16373DLG4	
			74ALVCH16373DLRG4	
	TSSOP – DGG	Tape and reel	SN74ALVCH16373DGGR	ALVCH16373
			74ALVCH16373DGGE4	
			74ALVCH16373DGGRG4	
	VFBGA – GQL	Tape and reel	SN74ALVCH16373KR	VH373
	VFBGA – ZQL (Pb-free)		74ALVCH16373ZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**GQL OR ZQL PACKAGE
(TOP VIEW)**

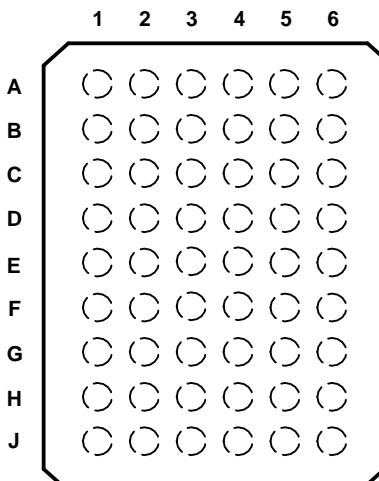


**TERMINAL ASSIGNMENTS⁽¹⁾
(56-Ball GQL/ZQL Package)**

	1	2	3	4	5	6
A	1 \overline{OE}	NC	NC	NC	NC	1LE
B	1Q2	1Q1	GND	GND	1D1	1D2
C	1Q4	1Q3	V _{CC}	V _{CC}	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
H	2Q5	2Q6	V _{CC}	V _{CC}	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	2 \overline{OE}	NC	NC	NC	NC	2LE

(1) NC – No internal connection

**GRD OR ZRD PACKAGE
(TOP VIEW)**



**TERMINAL ASSIGNMENTS⁽¹⁾
(54-Ball GRD/ZRD Package)**

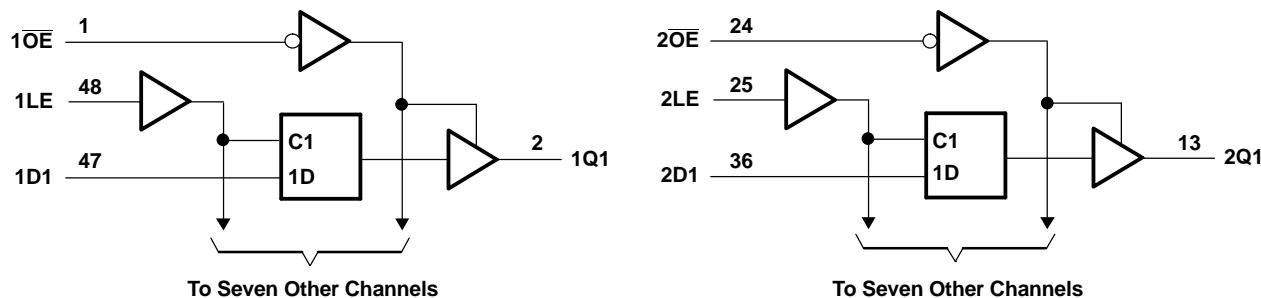
	1	2	3	4	5	6
A	1Q1	NC	1 \overline{OE}	1LE	NC	1D1
B	1Q3	1Q2	NC	NC	1D2	1D3
C	1Q5	1Q4	V _{CC}	V _{CC}	1D4	1D5
D	1Q7	1Q6	GND	GND	1D6	1D7
E	2Q1	1Q8	GND	GND	1D8	2D1
F	2Q3	2Q2	GND	GND	2D2	2D3
G	2Q5	2Q4	V _{CC}	V _{CC}	2D4	2D5
H	2Q7	2Q6	NC	NC	2D6	2D7
J	2Q8	NC	2 \overline{OE}	2LE	NC	2D8

(1) NC – No internal connection

FUNCTION TABLE
(EACH 8-BIT SECTION)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG and DL packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
V_O	Output voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		± 50	mA
	Continuous current through each V_{CC} or GND		± 100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package	70	°C/W
		DL package	63	
		GQL/ZQL package	42	
		GRD/ZRD package	36	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

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Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.65	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	
V_{IL}	Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0.8	
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65 \text{ V}$	-4	mA
		$V_{CC} = 2.3 \text{ V}$	-12	
		$V_{CC} = 2.7 \text{ V}$	-12	
		$V_{CC} = 3 \text{ V}$	-24	
I_{OL}	Low-level output current	$V_{CC} = 1.65 \text{ V}$	4	mA
		$V_{CC} = 2.3 \text{ V}$	12	
		$V_{CC} = 2.7 \text{ V}$	12	
		$V_{CC} = 3 \text{ V}$	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
T_A	Operating free-air temperature	-40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OH} = -100 µA	1.65 V to 3.6 V	V _{CC} - 0.2			V
	I _{OH} = -4 mA	1.65 V		1.2		
	I _{OH} = -6 mA	2.3 V		2		
		2.3 V		1.7		
	I _{OH} = -12 mA	2.7 V		2.2		
		3 V		2.4		
	I _{OH} = -24 mA	3 V		2		
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V		0.2		V
	I _{OL} = 4 mA	1.65 V		0.45		
	I _{OL} = 6 mA	2.3 V		0.4		
		2.3 V		0.7		
	I _{OL} = 12 mA	2.7 V		0.4		
	I _{OL} = 24 mA	3 V		0.55		
I _I	V _I = V _{CC} or GND	3.6 V		±5	µA	
I _{I(hold)}	V _I = 0.58 V	1.65 V		25		µA
	V _I = 1.07 V	1.65 V		-25		
	V _I = 0.7 V	2.3 V		45		
	V _I = 1.7 V	2.3 V		-45		
	V _I = 0.8 V	3 V		75		
	V _I = 2 V	3 V		-75		
	V _I = 0 to 3.6 V ⁽²⁾	3.6 V		±500		
I _{OZ}	V _O = V _{CC} or GND	3.6 V		±10	µA	
I _{CC}	V _I = V _{CC} or GND I _O = 0	3.6 V		40	µA	
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		750	µA	
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	3		pF
	Data inputs			6		
C _o	Outputs	V _O = V _{CC} or GND	3.3 V	7	pF	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 1.8 V	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high or low	(1)		3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE↓	(1)		1		1		1.1		ns
t _h	Hold time, data after LE↓	(1)		1.5		1.7		1.4		ns

(1) This information was not available at the time of publication.

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SCES020I—JULY 1995—REVISED NOVEMBER 2005

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Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	(1)	1	4.5	4.3	1.1	3.6		ns
	LE		(1)	1	4.9	4.6	1	3.9		
t_{en}	\overline{OE}	Q	(1)	1	6	5.7	1	4.7	ns	
t_{dis}	\overline{OE}	Q	(1)	1.2	5.1	4.5	1.4	4.1	ns	

(1) This information was not available at the time of publication.

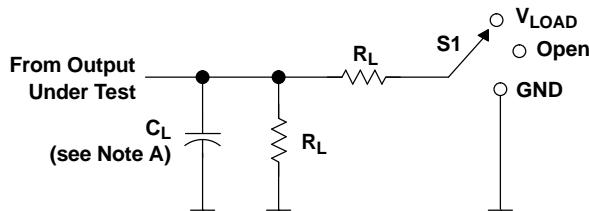
Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
		TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	Outputs enabled	(1)	19	22	pF
	Outputs disabled	(1)	4	5	

(1) This information was not available at the time of publication.

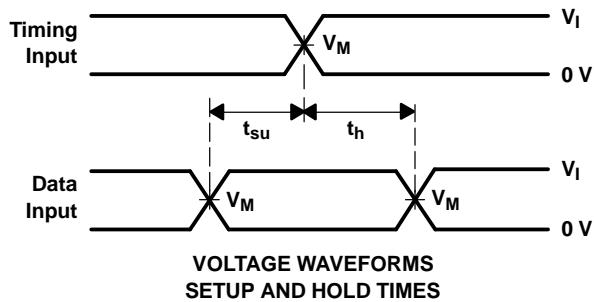
PARAMETER MEASUREMENT INFORMATION



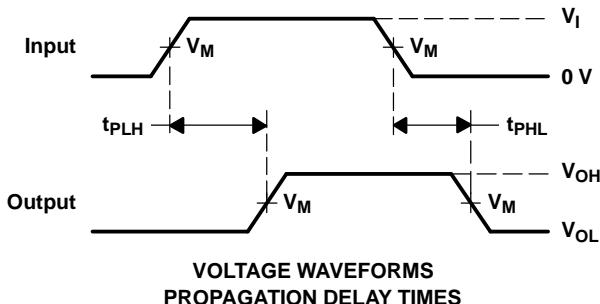
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

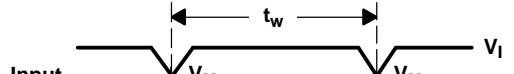
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 V \pm 0.2$ V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3 V \pm 0.3$ V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



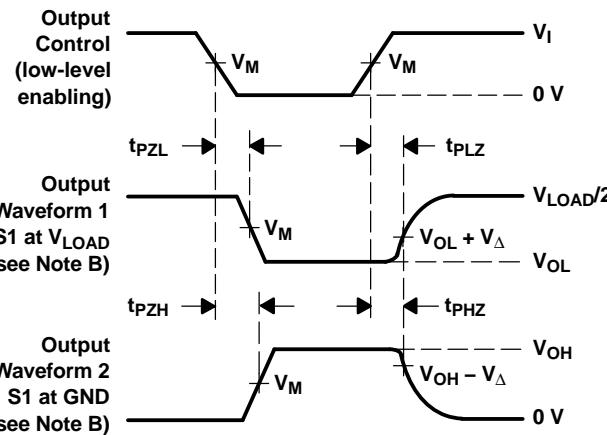
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50$ Ω .
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74ALVCH16373DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16373	Samples
74ALVCH16373DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16373	Samples
74ALVCH16373DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16373	Samples
74ALVCH16373GRDR	OBsolete	BGA MICROSTAR JUNIOR	GRD	54		TBD	Call TI	Call TI	-40 to 85	VH373	
74ALVCH16373GRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16373	Samples
74ALVCH16373ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	VH373	Samples
74ALVCH16373ZRDR	ACTIVE	BGA MICROSTAR JUNIOR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	VH373	Samples
SN74ALVCH16373DGG	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16373	Samples
SN74ALVCH16373DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16373	Samples
SN74ALVCH16373DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16373	Samples
SN74ALVCH16373KR	OBsolete	BGA MICROSTAR JUNIOR	GQL	56		TBD	Call TI	Call TI	-40 to 85	VH373	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

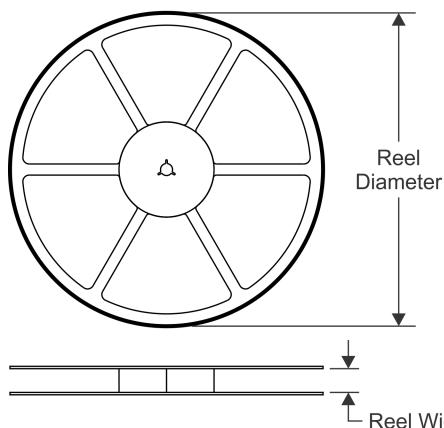
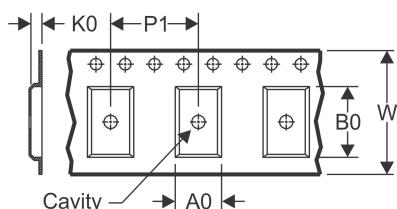
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

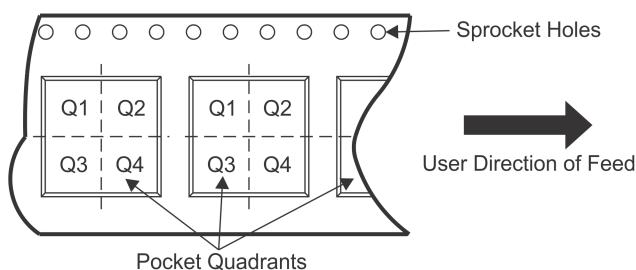
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ALVCH16373ZQLR	BGA MI CROSTA R JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
74ALVCH16373ZRDR	BGA MI CROSTA R JUNIOR	ZRD	54	1000	330.0	16.4	5.8	8.3	1.55	8.0	16.0	Q1
SN74ALVCH16373DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74ALVCH16373DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

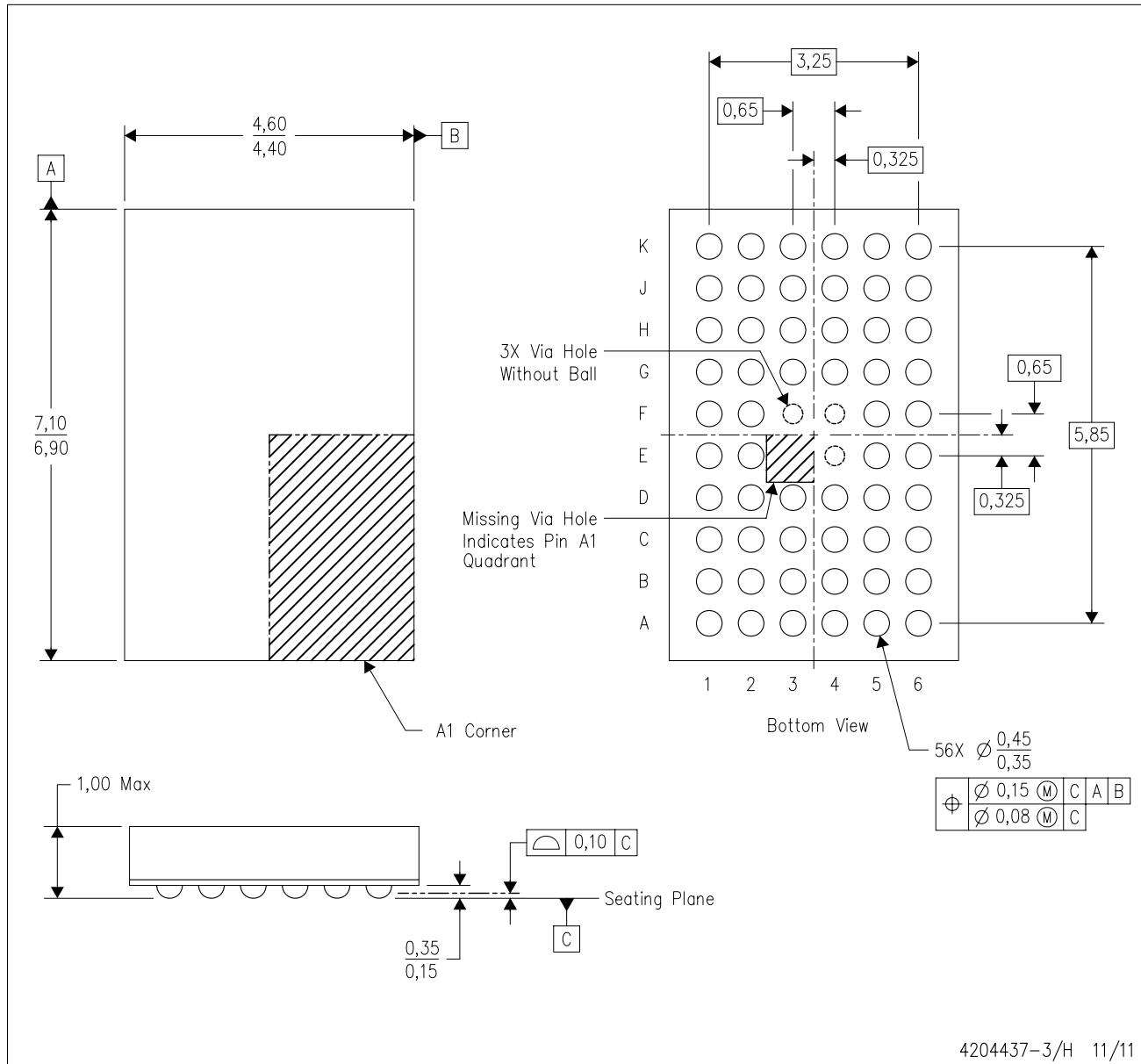
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ALVCH16373ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	333.2	345.9	28.6
74ALVCH16373ZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	333.2	345.9	28.6
SN74ALVCH16373DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ALVCH16373DLR	SSOP	DL	48	1000	367.0	367.0	55.0

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



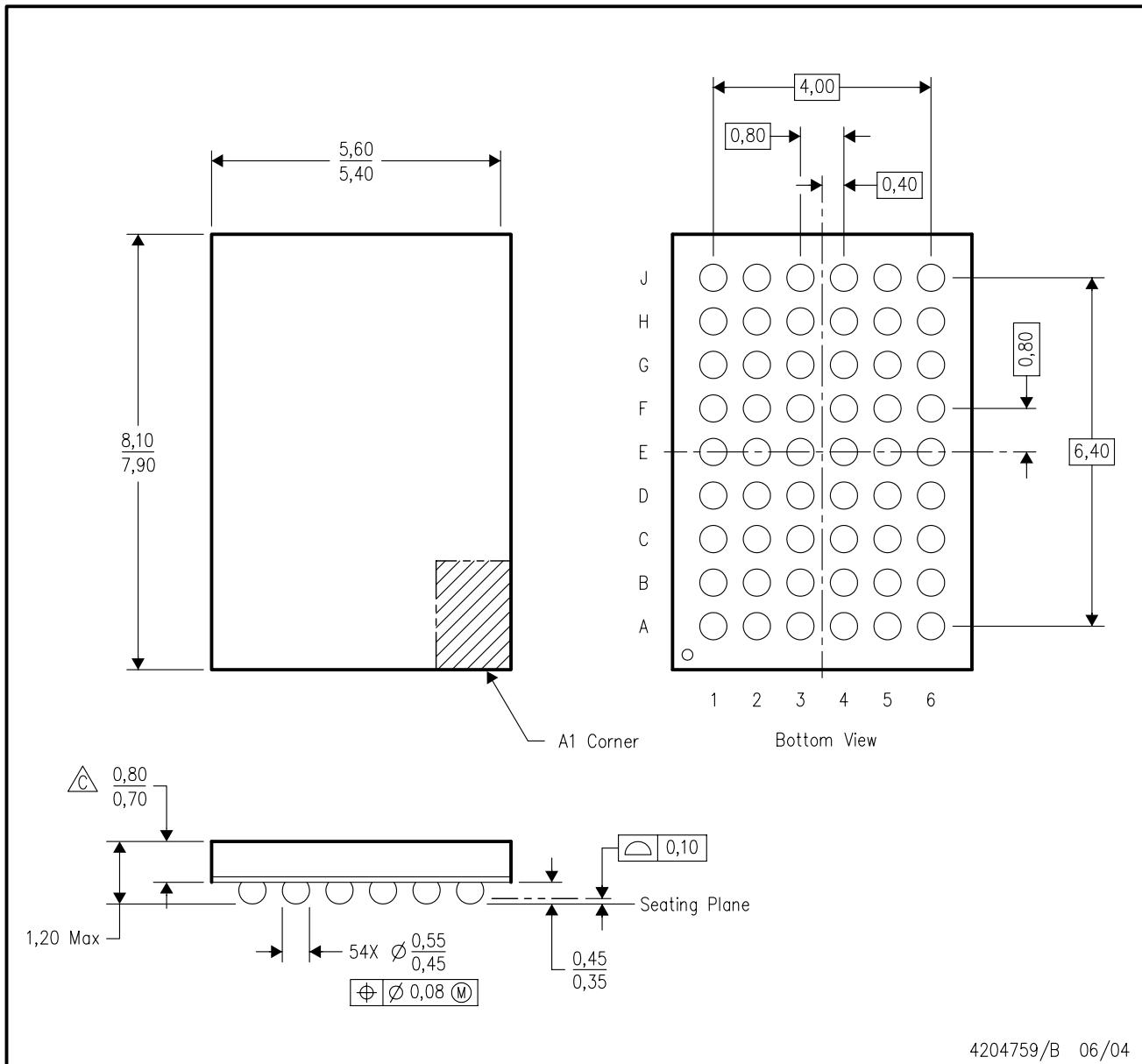
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MO-285 variation BA-2.
 - This package is Pb-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

4204437-3/H 11/11

MicroStar Junior is a trademark of Texas Instruments

GRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY



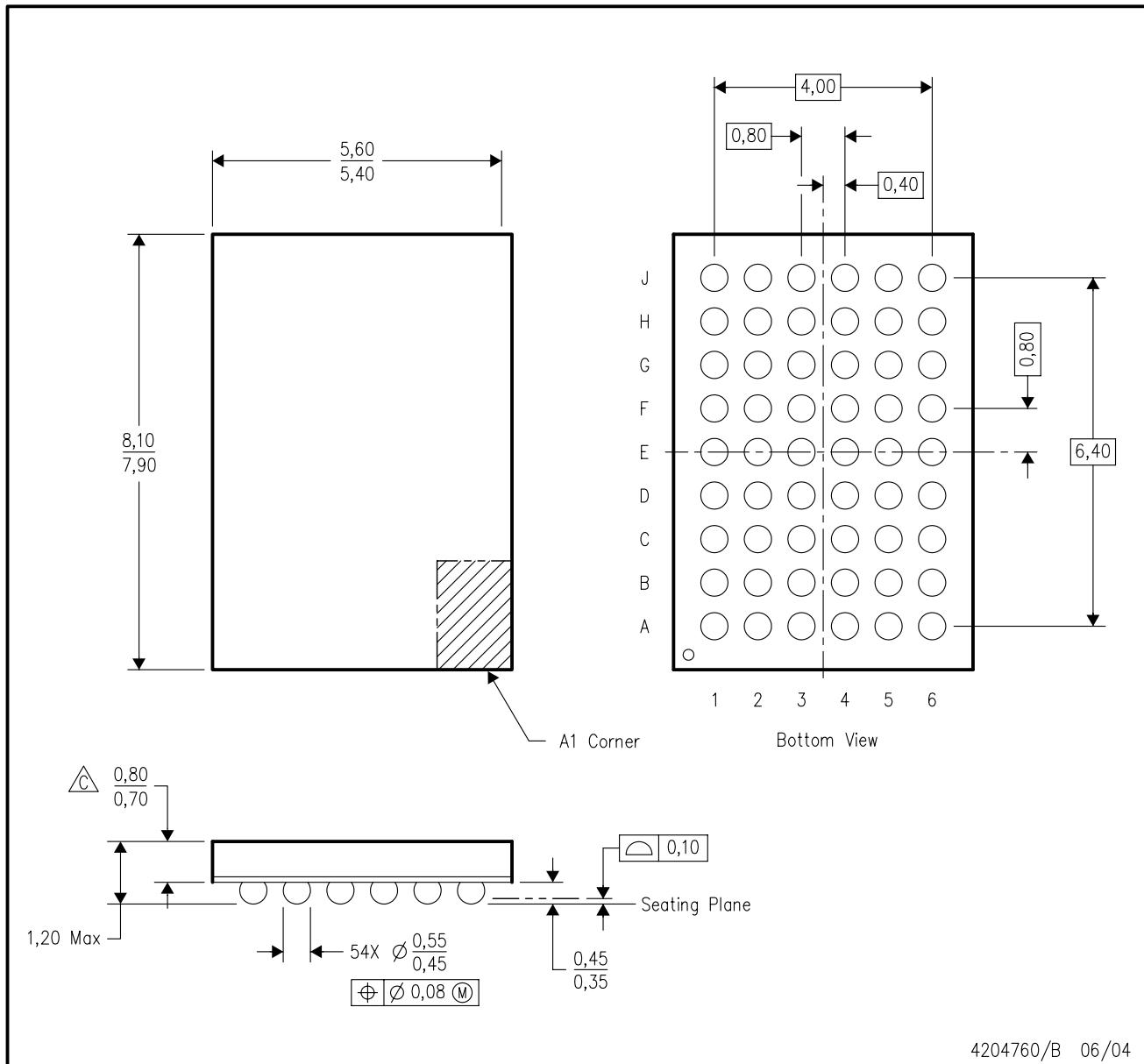
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

Falls within JEDEC MO-205 variation DD.

D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

ZRD (R-PBGA-N54)

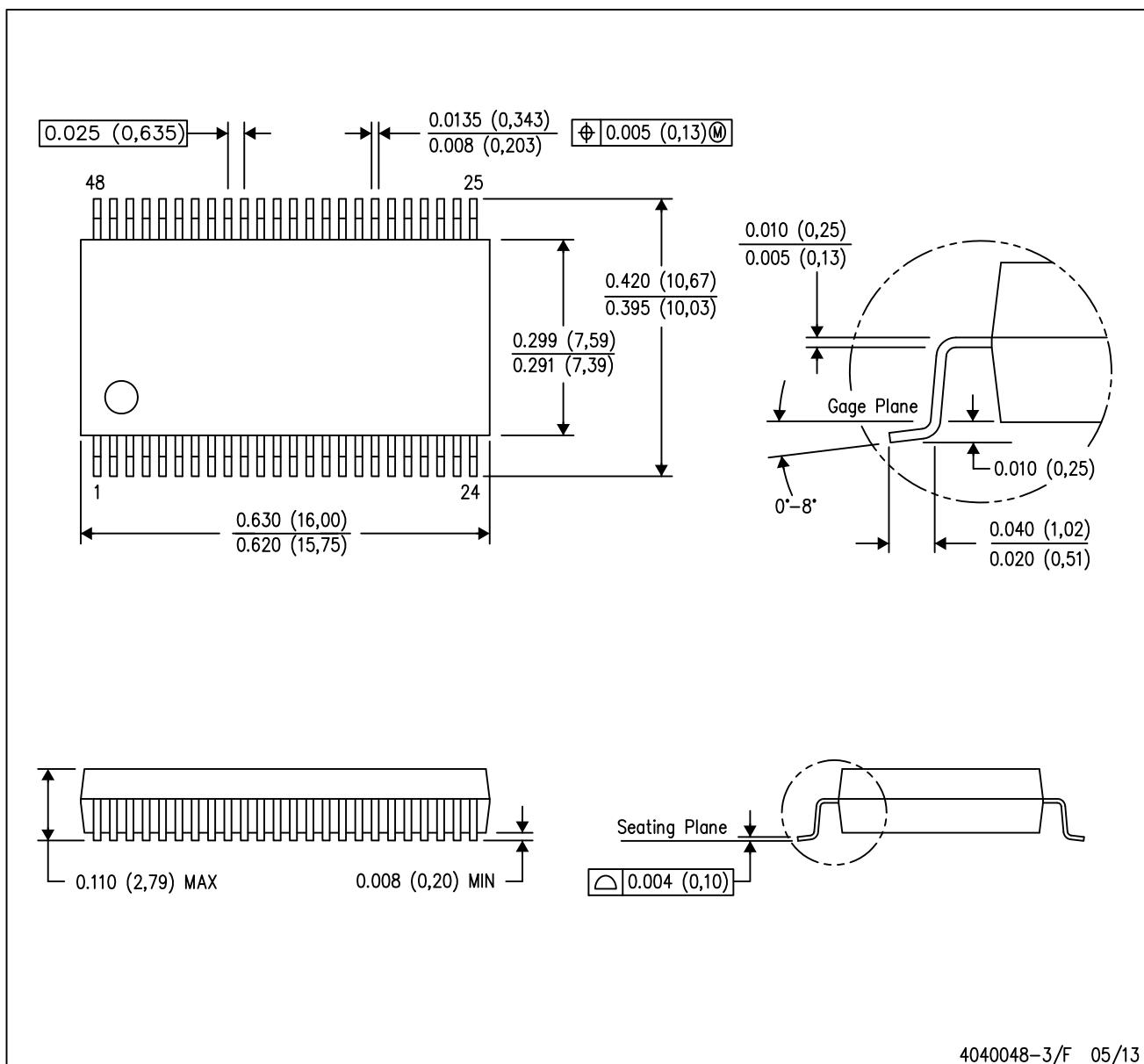
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation DD.
 - D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



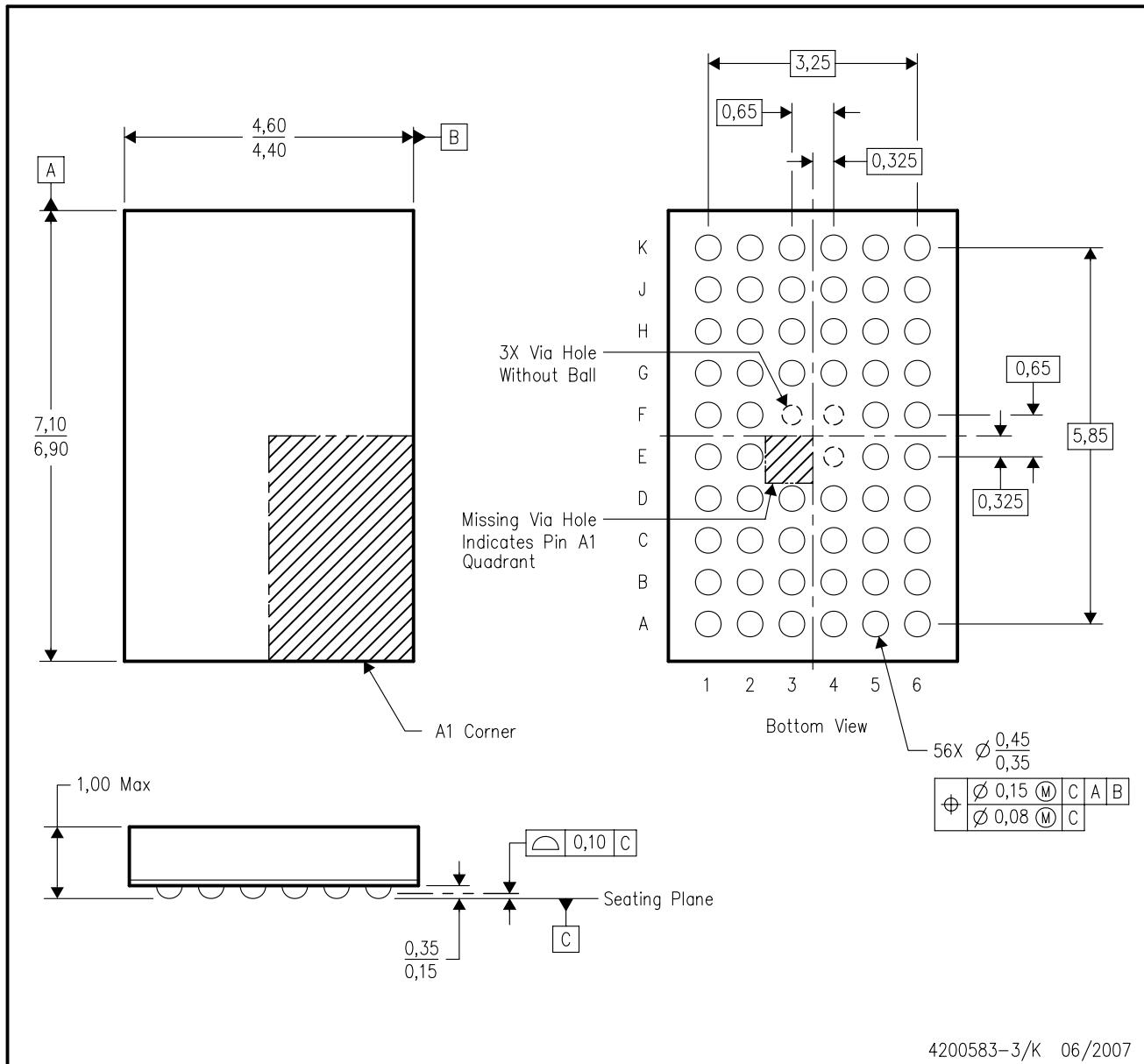
4040048-3/F 05/13

- NOTES:
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 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

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GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



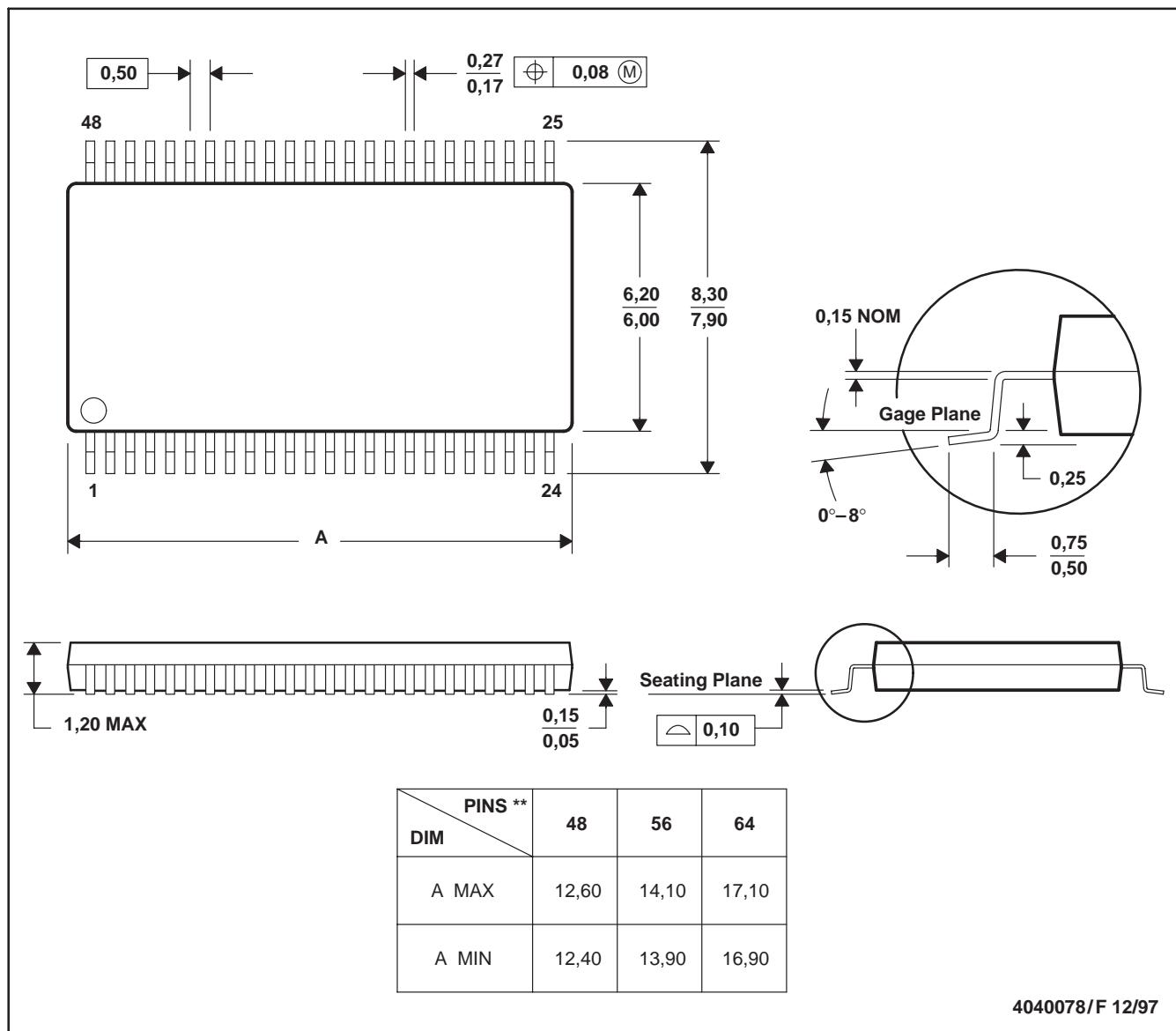
4200583-3/K 06/2007

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MO-285 variation BA-2.
 - This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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